ECE 238L Digital Computers and Number Systems Lecture lab 4

September 25, 2006

– Typeset by $\ensuremath{\mathsf{FoilT}}_E\!X$ –

Do any engineering students need a job?

Date: Mon, 25 Sep 2006 10:02:58 -0600
From: Joseph L. Sanchez <josanchez@lanl.gov>
Subject: engineering student

Justin,

I have a job opening for an engineering student which will last about two and a half months with a possible extension. The job would be available immediately. The task the student will be working on is assisting me to model a facility electrical power system for one of the facilities here at the laboratory. The job will be a minimum of 20 hrs per week with the option to work more. If you have any students that are interested in applying, please have them give me a call, or email.

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Problem – There must be an easier way to build repetious circuits...

label: for variable in range generate -- label required block declarative items -- optional begin concurrent statements -- using variable end generate [label]; Label: if boolean_expression generate -- conditional [declarative region] -- optional begin {concurrent statement} -- use variable or not. end generate [label];

Example – Muxes

Example – Complex

```
G1 : For N in 7 downto 0 generate
begin
 G2: if (n = 7) generate
  begin
     or1 : or_gate
       port map(A => S1(N), B => S2(N), C => S3(N));
  end generate g2;
  G3 : if (N < 7) generate
  begin
     and_array : and_gate
        port map(X => S1(N), Y => S2(N), Z => S3(N));
  end generate G3;
end generate g1;
```

Example – Complex

```
L : For i in 0 to 7 generate
  begin
     RO : if ( i = 0 ) generate
       begin
         U1:component DFF
           port map ( CLK => clock, DATA => din, Q=>dout(i));
       end generate RO;
     RI : if ( i /= 0 ) generate
       begin
         U1:component DFF
           port map (CLK=>clock, DATA=>dout(i-1), Q=>dout(i));
       end generate R1;
end generate L;
```