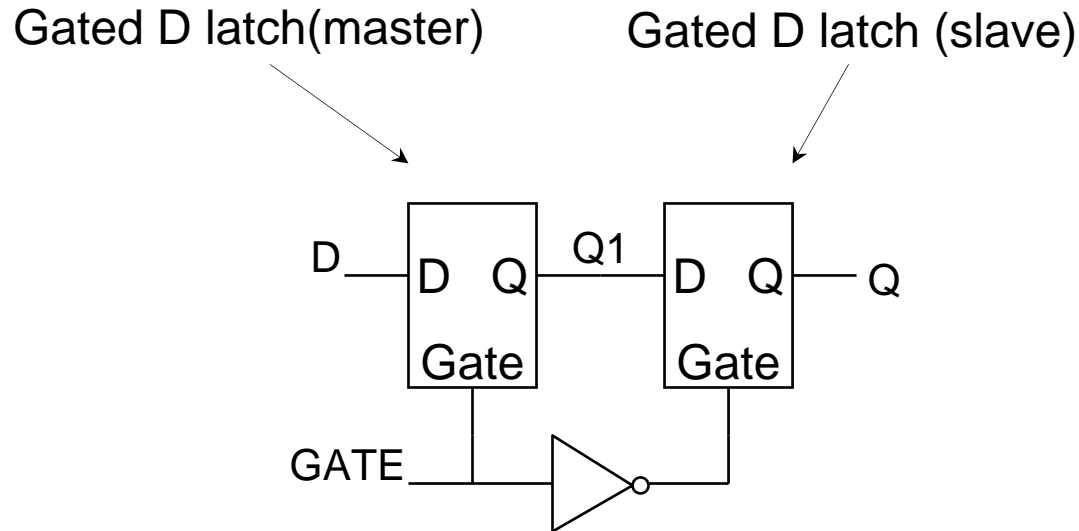


MSFF

Master/Slave Flip Flops

A Master/Slave Flip Flop (D Type)



Either:

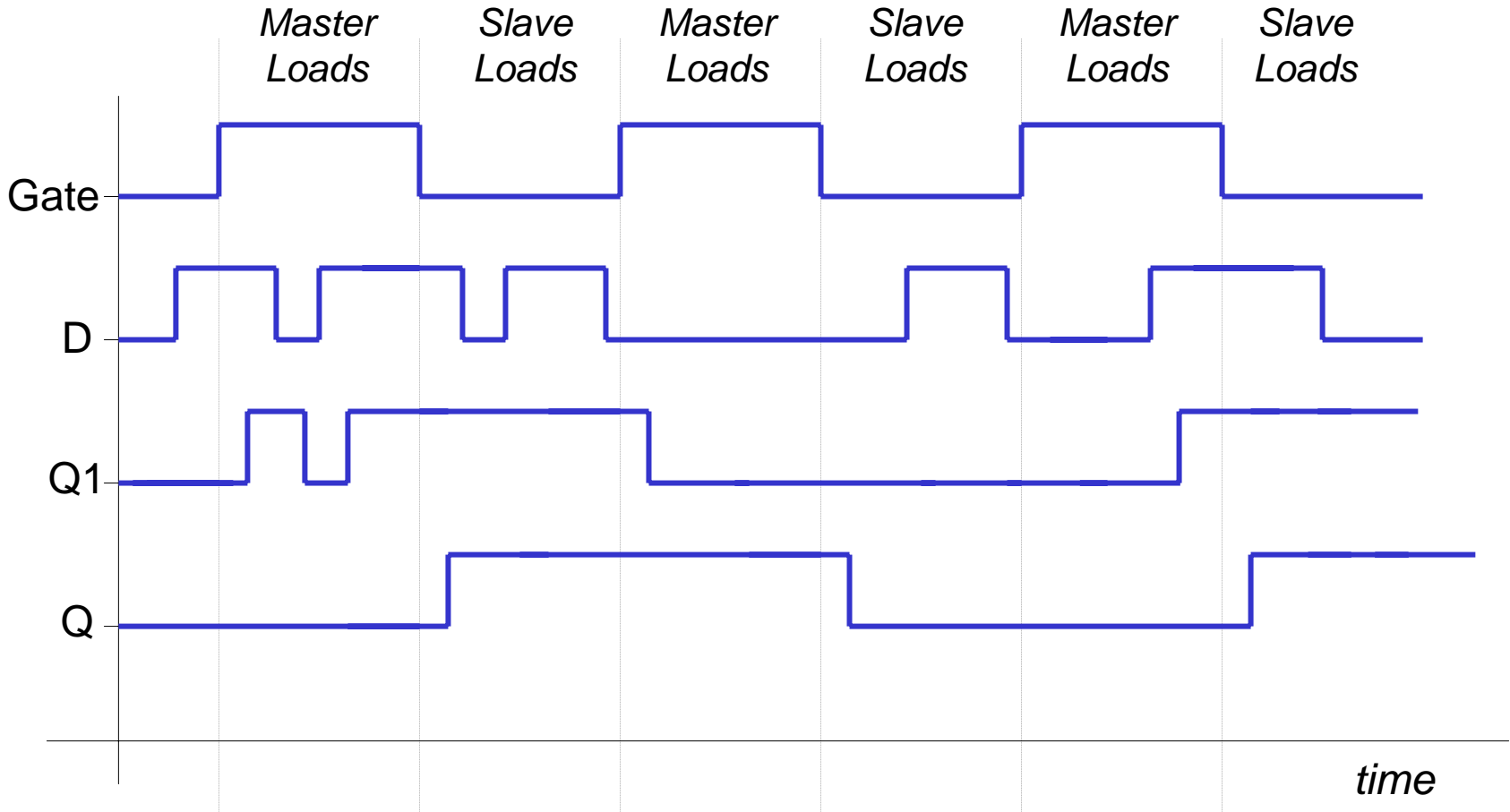
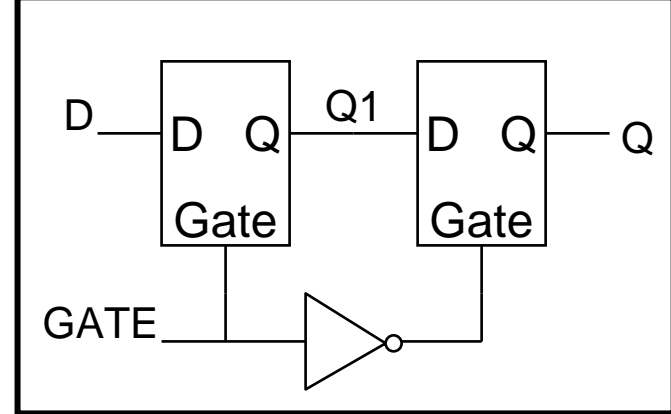
The master is loading (the master is *on*)

or

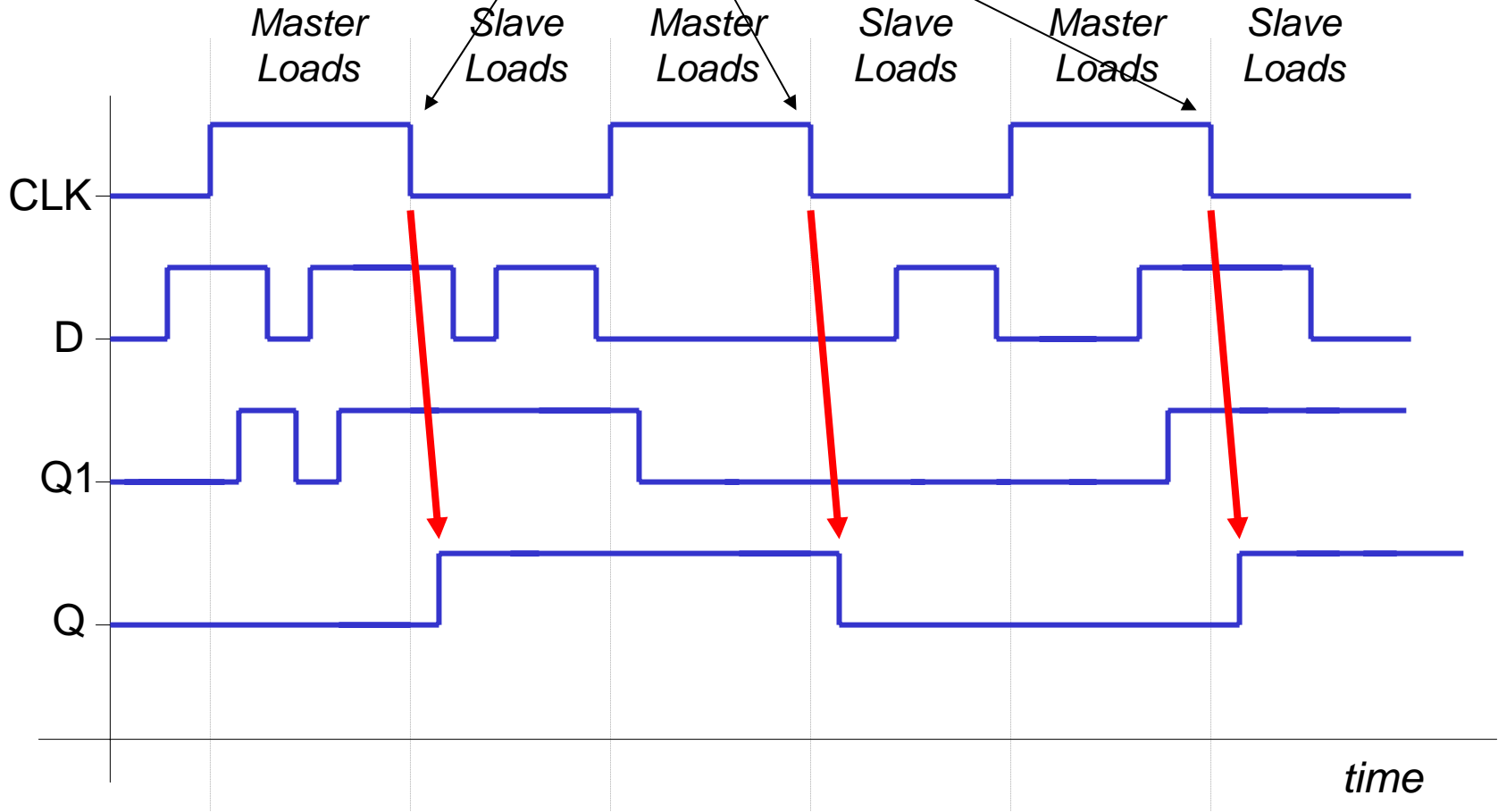
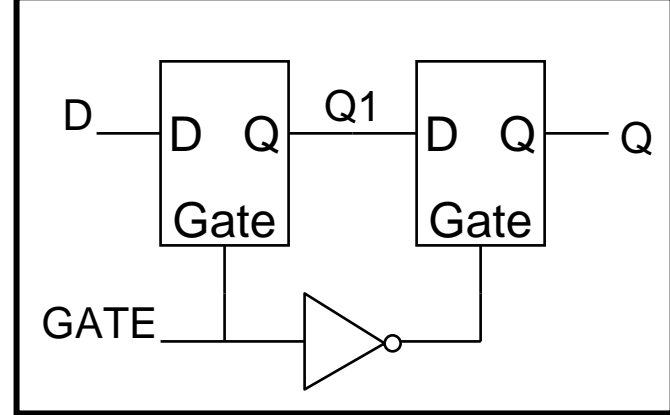
The slave is loading (the slave is *on*)

But never both at the same time...

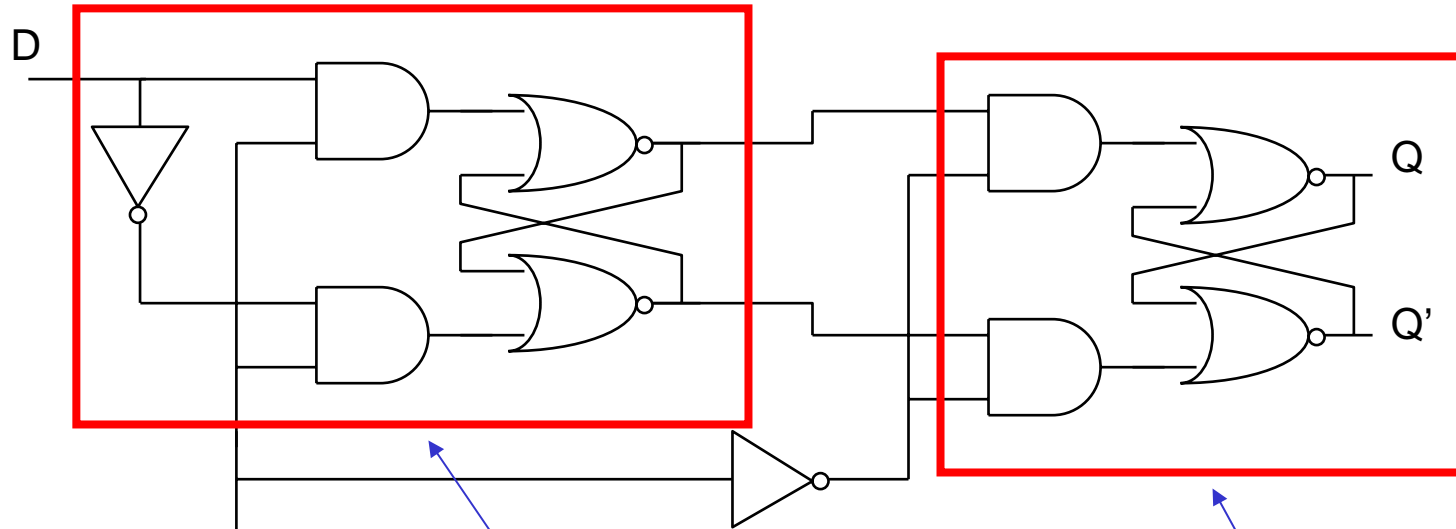
DFF Timing



Output Changes in Response to Falling Clock



DFF Detailed Schematic



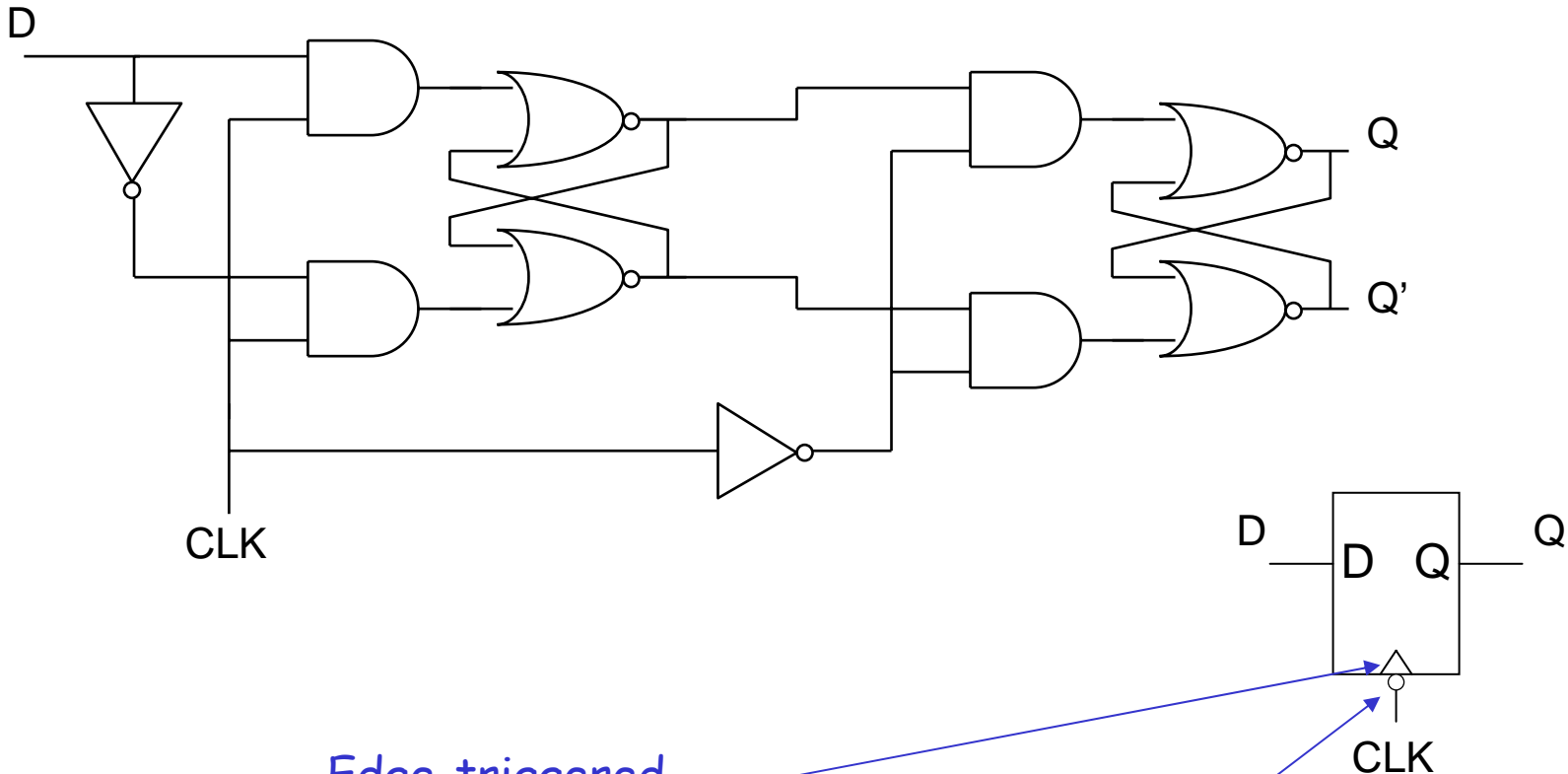
CLK

Master latch (D)

Usually call the gate "CLK"

Slave latch (SR)

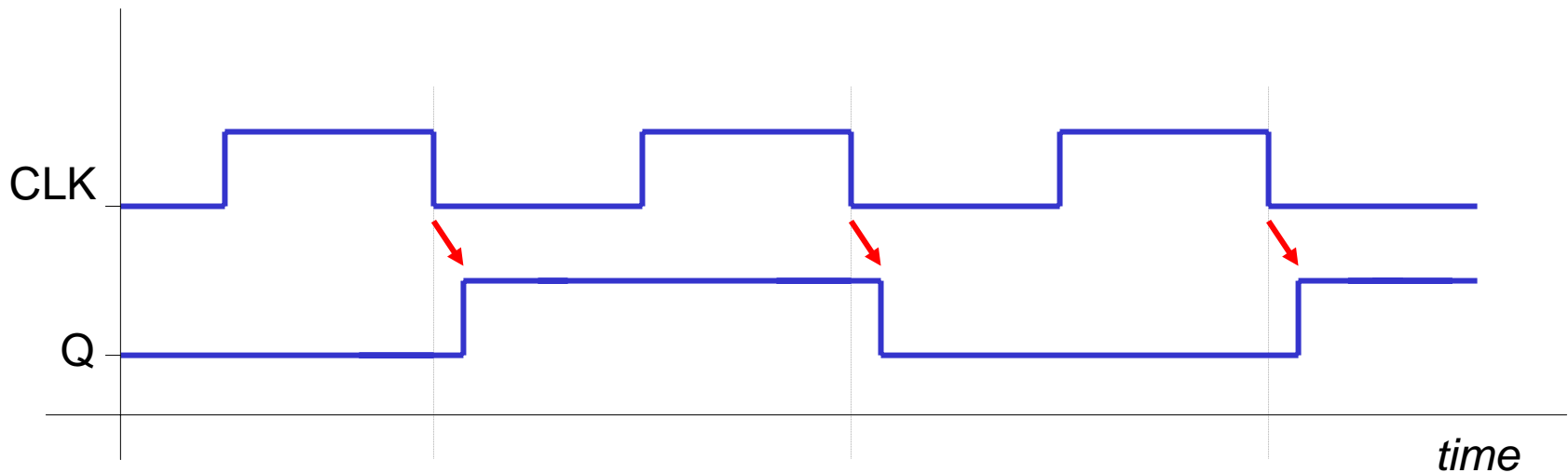
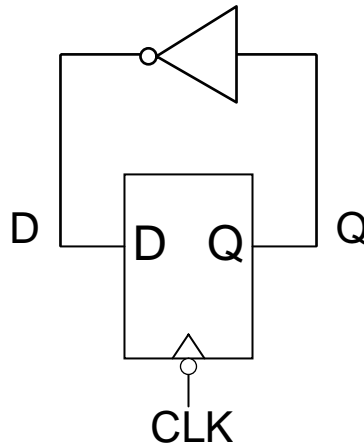
A Falling Edge Triggered DFF



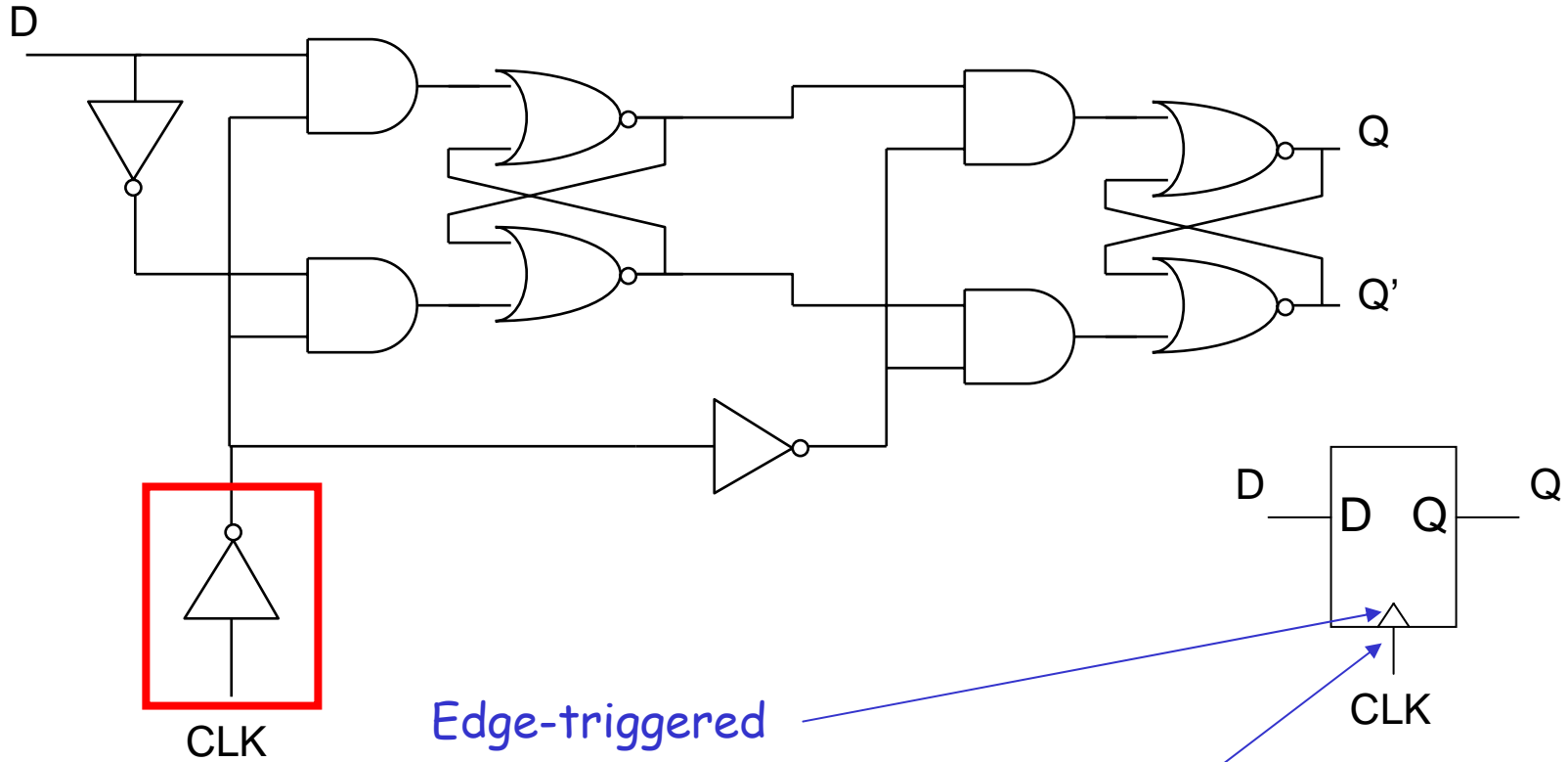
Edge-triggered

Falling edge triggered

Oscillator (Toggle Circuit) Operation



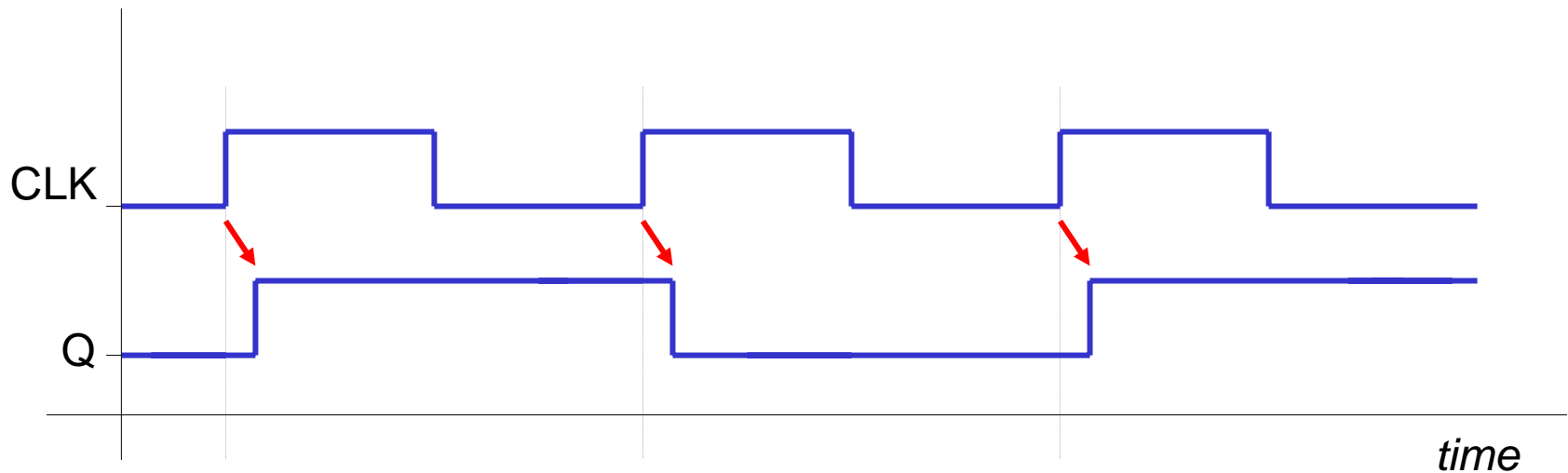
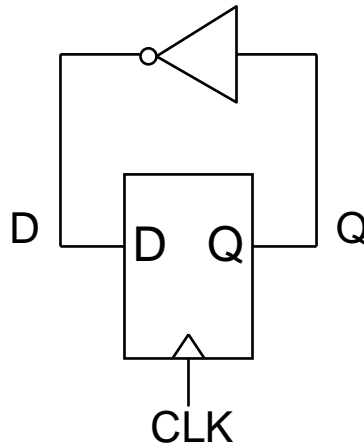
Rising Edge Triggered DFF Schematic



Edge-triggered

Rising edge triggered

Oscillator (Toggle Circuit) Operation



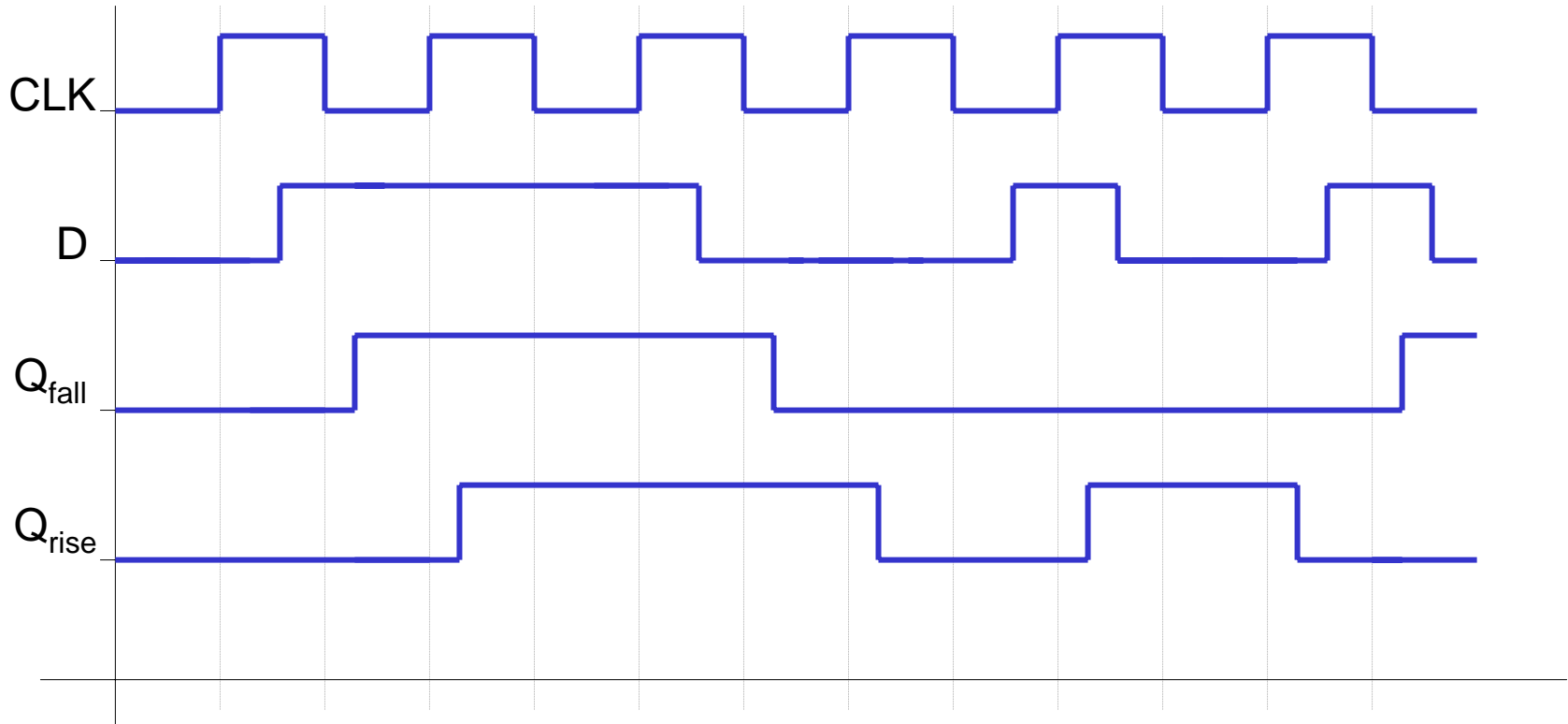
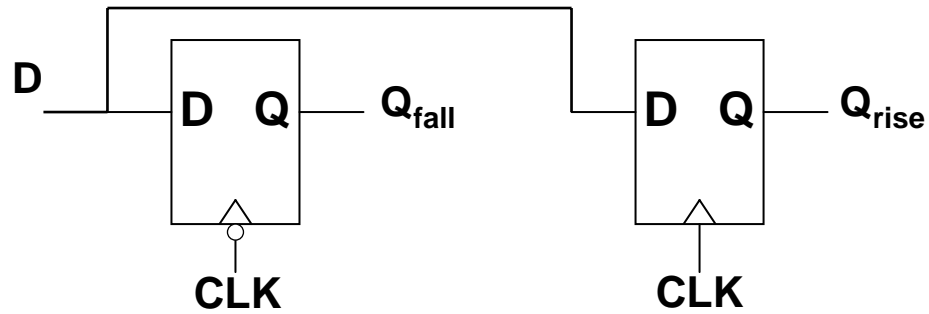
D Flip Flop Transition Table

D	Q	Q+
0	0	0
0	1	0
1	0	1
1	1	1

$Q_+ = D$

No clock shown since it is edge triggered (assumed)

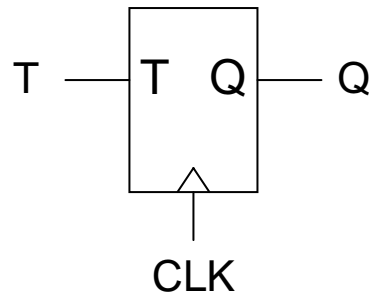
Falling vs. Rising Edge Triggered



Alternative Flip Flops

T
JK

Toggle Flip Flop

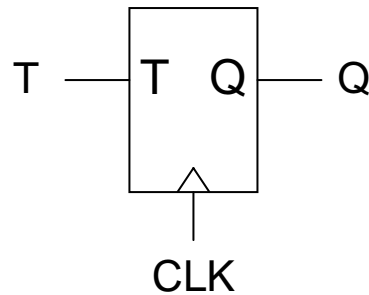


T	Q	Q+	
0	0	0	No
0	1	1	Action
1	0	1	Toggle
1	1	0	

$$Q_+ = T' \cdot Q + T \cdot Q' = T \oplus Q$$

Clock edge is assumed
in this transition table...

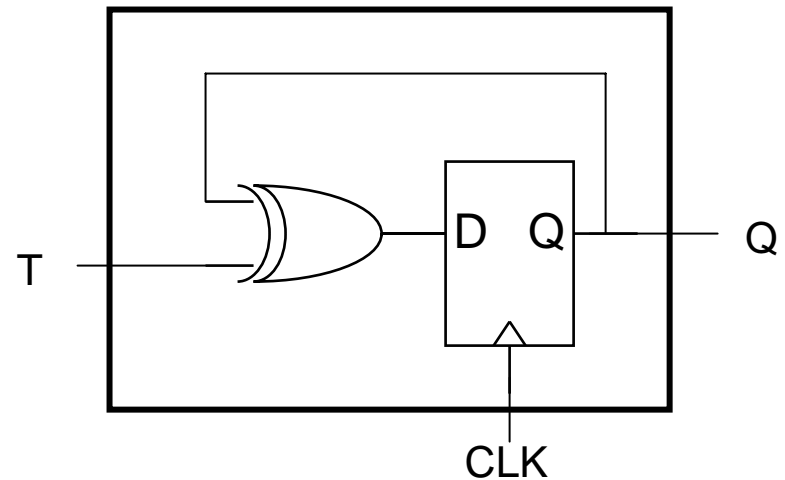
Toggle Flip Flop



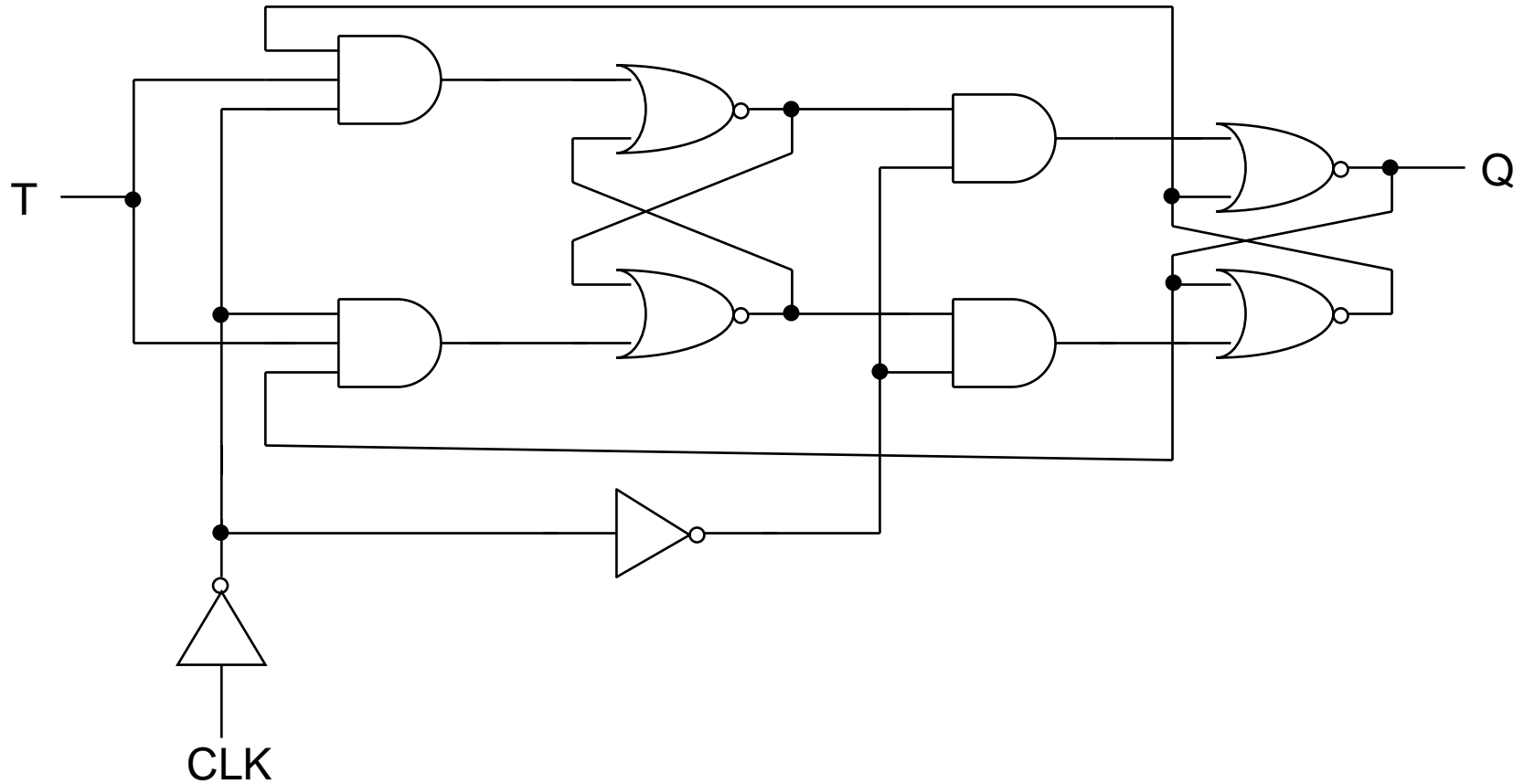
T	Q	Q+	
0	0	0	No
0	1	1	Action
1	0	1	Toggle
1	1	0	

$$Q_+ = T' \cdot Q + T \cdot Q' = T \oplus Q$$

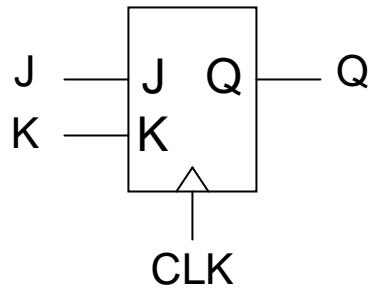
An oscillator with an enable input (T)



Toggle Flip Flop



JK Flip Flop

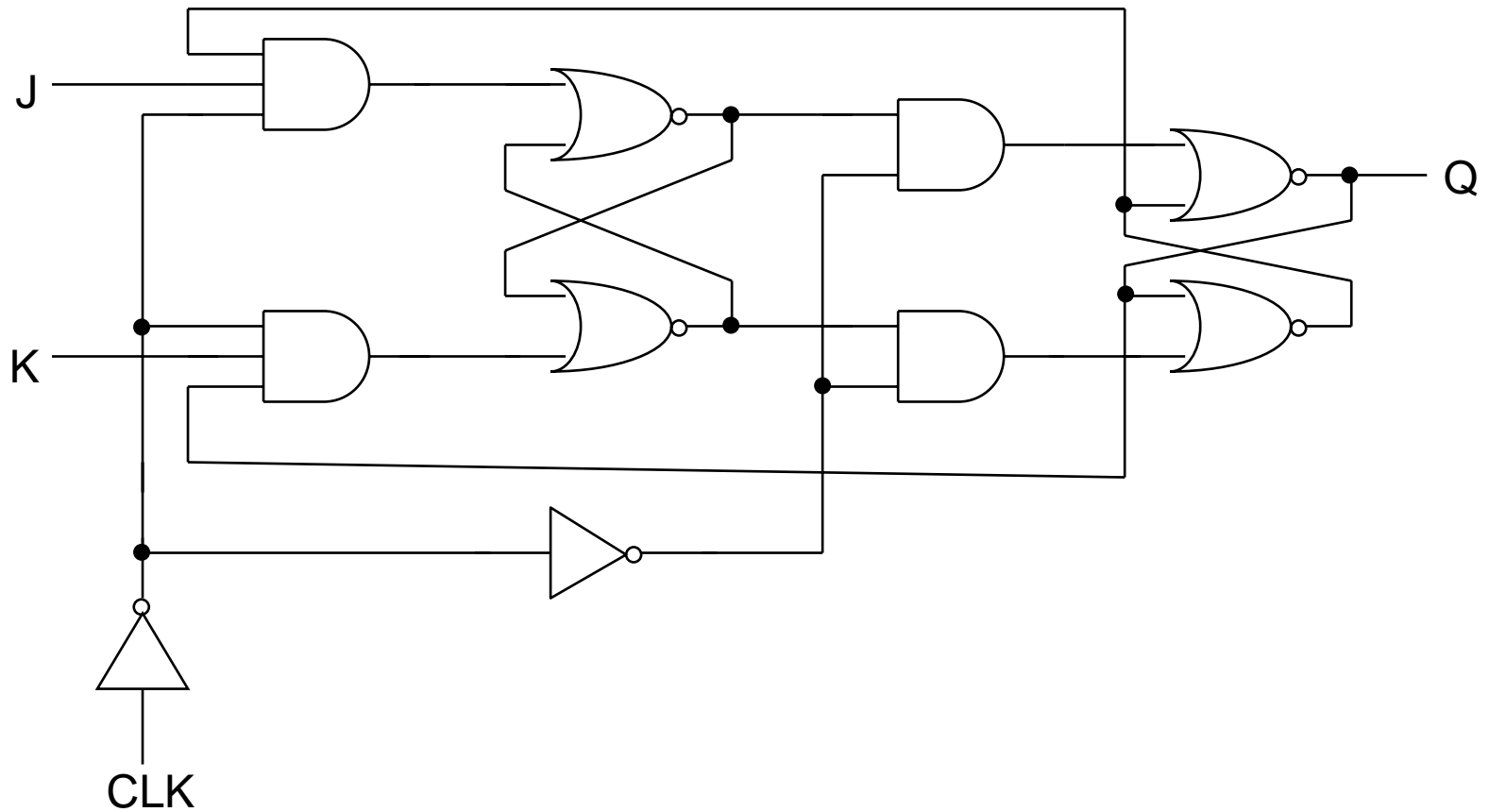


J	K	Q	Q+	
0	0	0	0	No Change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

Kind of a cross between
a SR FF and a T FF

$$Q+ = K' \cdot Q + J \cdot Q'$$

JK Flip Flop

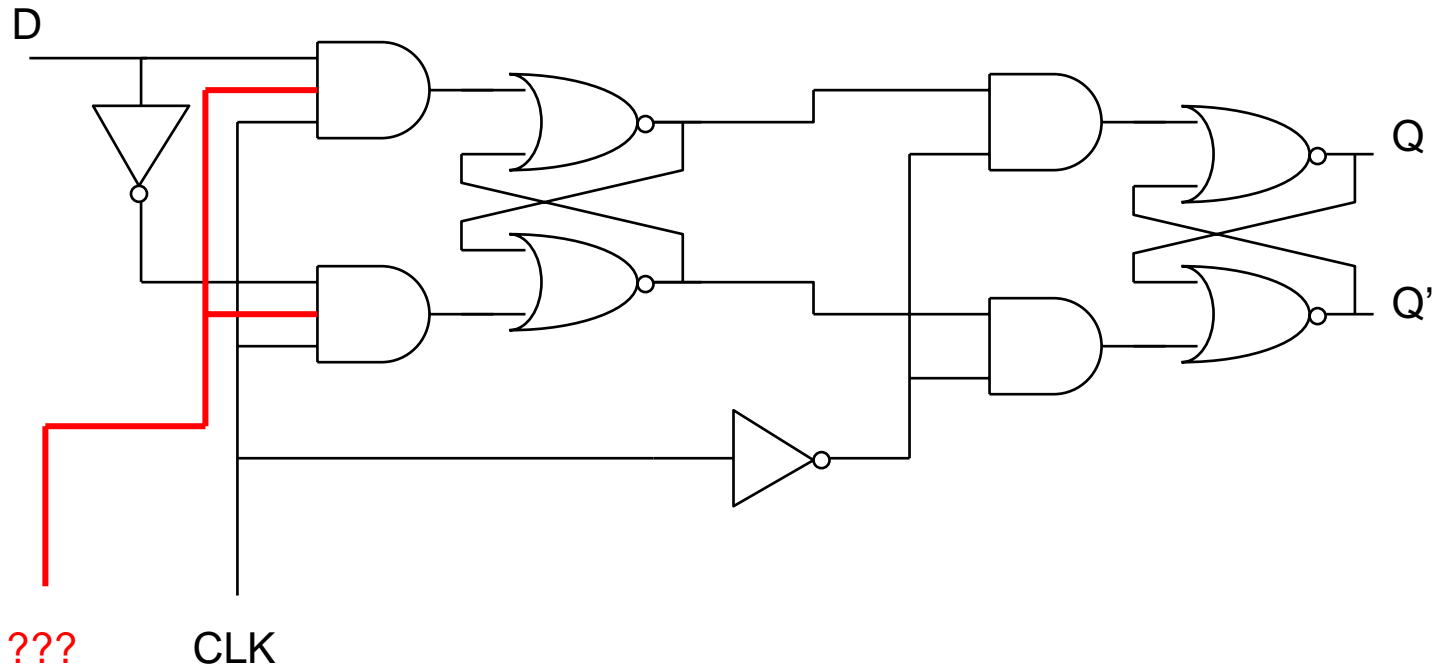


Why Alternative FF's?

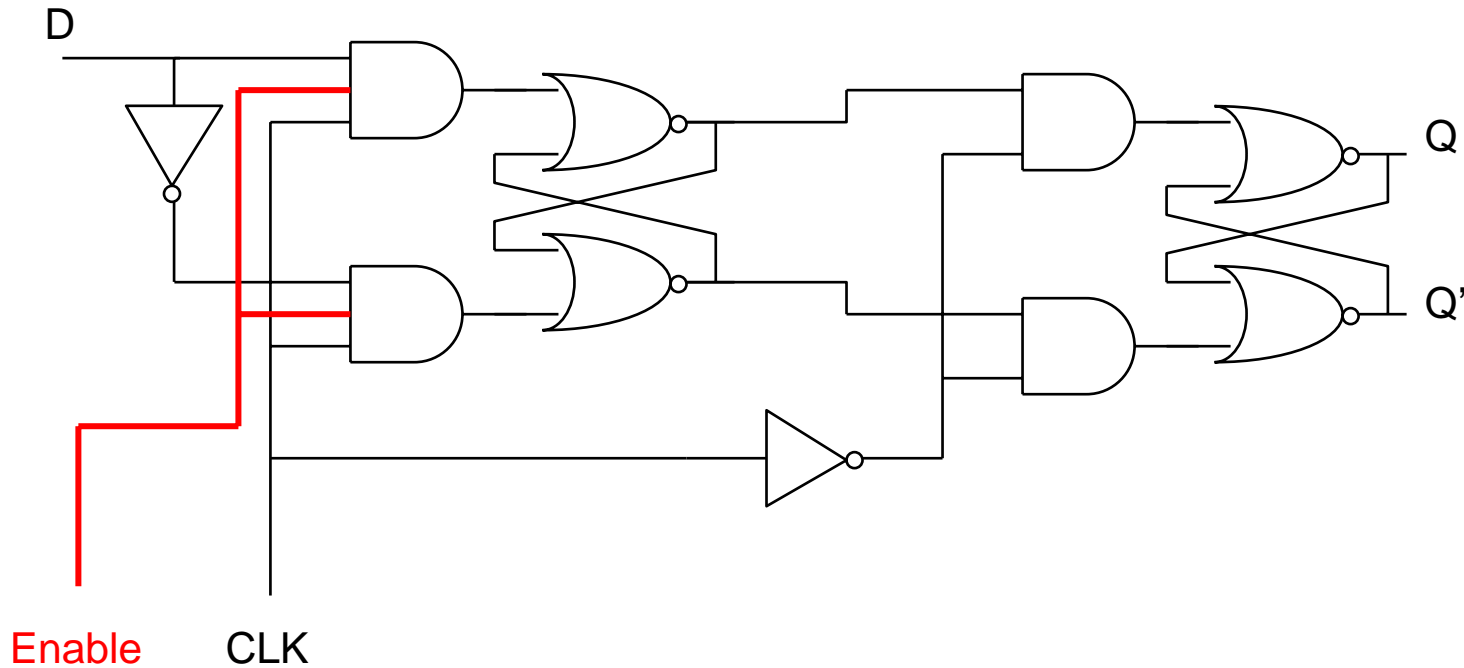
- With discrete parts (TTL family)
 - JK or T FF's could reduce gate count for the input forming logic
 - Extensively used
- With VLSI IC's and FPGA's
 - JK or T FF's must be built from DFF+gates
 - Larger, slower than a DFF
 - Not used

Flip Flops With Additional Control Inputs

What is this?



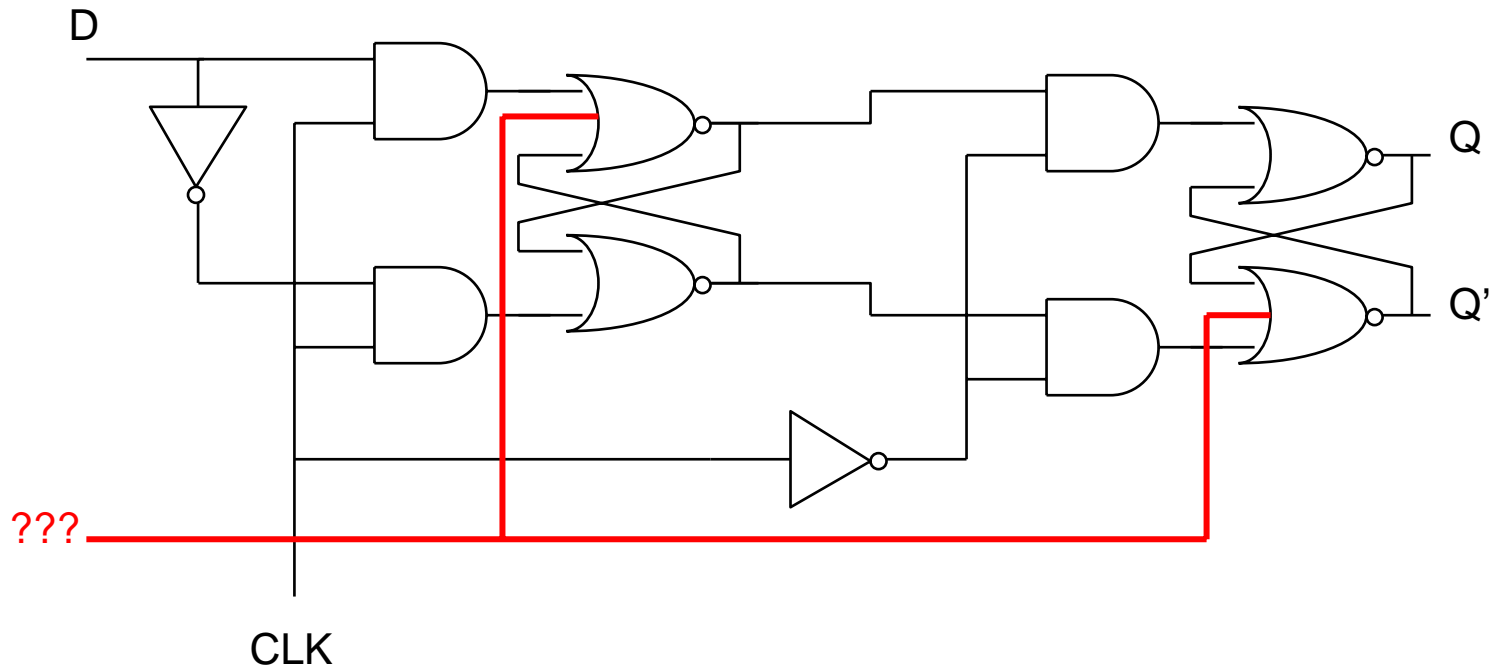
What is this?



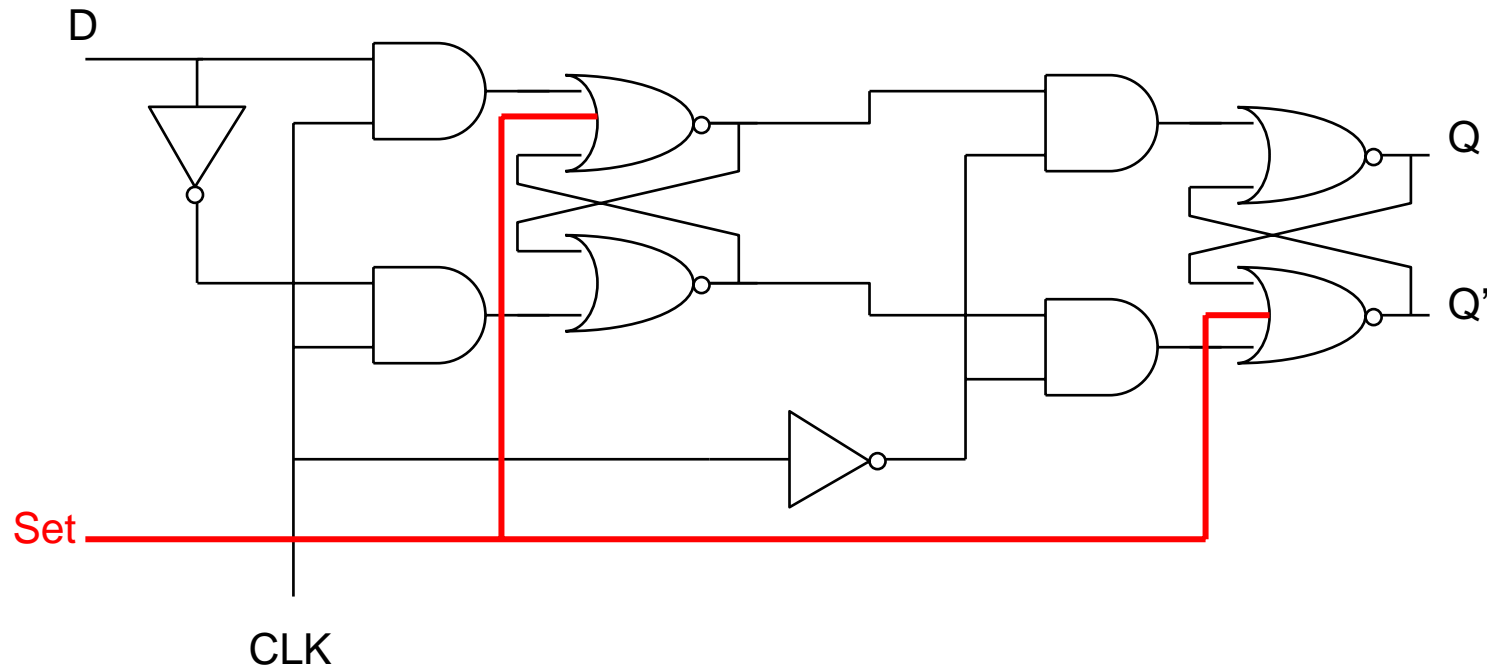
A falling edge triggered, D-type FF with enable

Master only loads when $CLK=Enable='1'$

What is this?



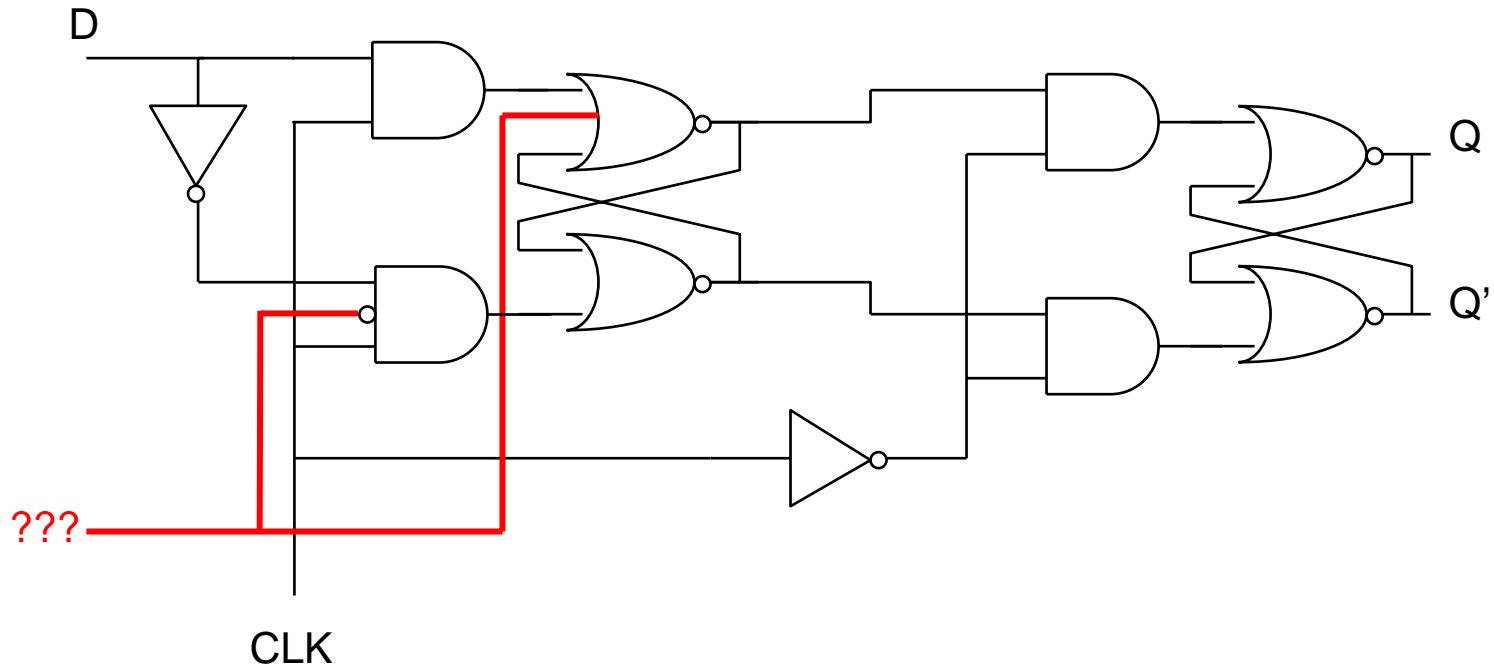
What is this?



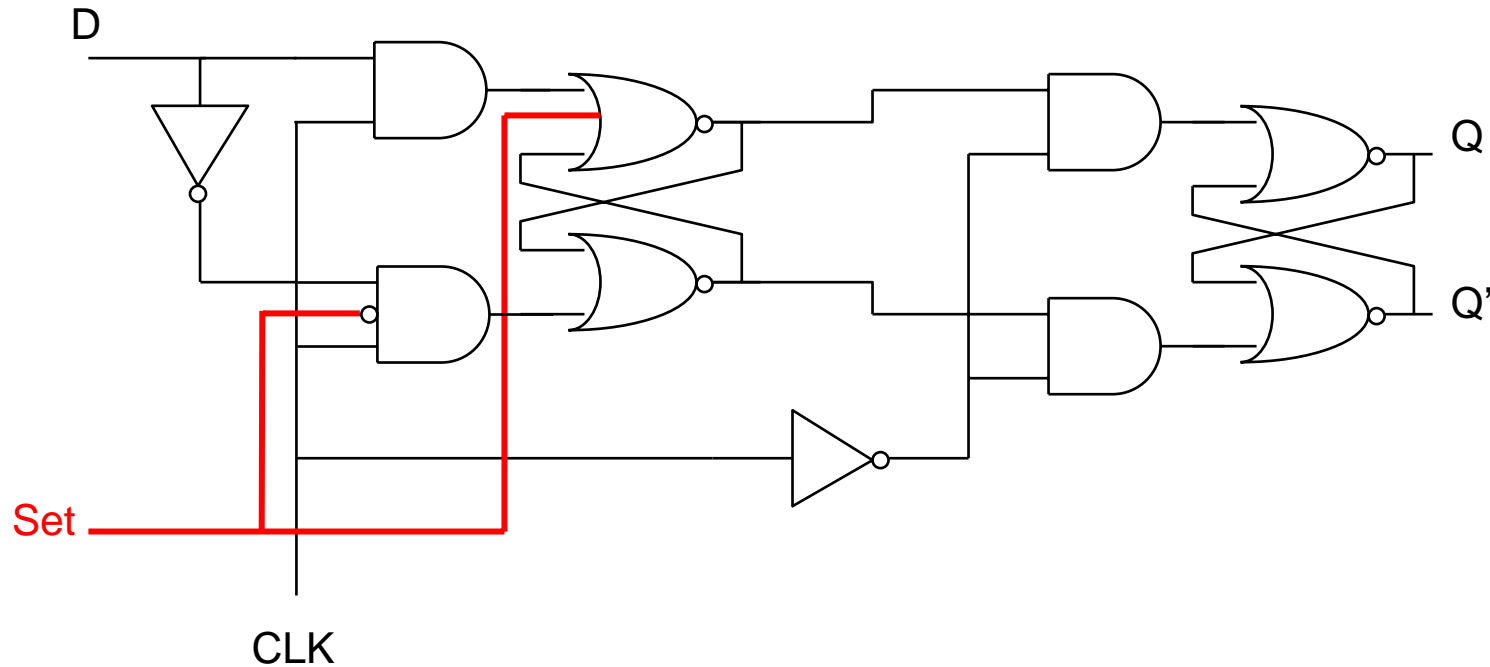
A falling edge triggered, D-type FF with an asynchronous set

If Set=1 then $Q \Rightarrow 1$, regardless of CLK or D

What is this?



What is this?



A falling edge triggered, D-type FF with a synchronous set

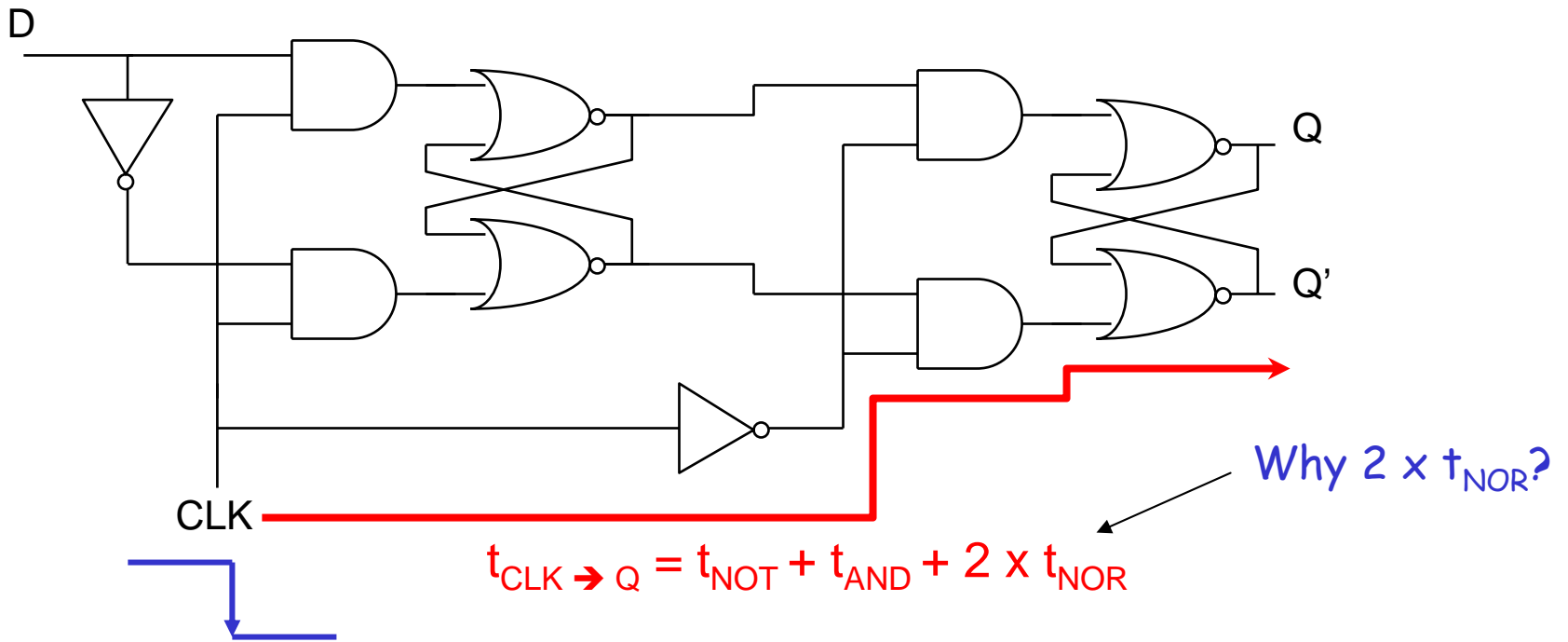
If Set=1 then $Q \Rightarrow 1$ on the next falling edge of the clock, regardless of D

Flip Flops With Additional Control Inputs

- A variety of FF's have been made over the years
- They contain combinations of these inputs:
 - Enable
 - Set
 - Reset
- The Set and Reset can be either:
 - Asynchronous (independent of CLK)
 - Synchronous (work only on CLK edge)

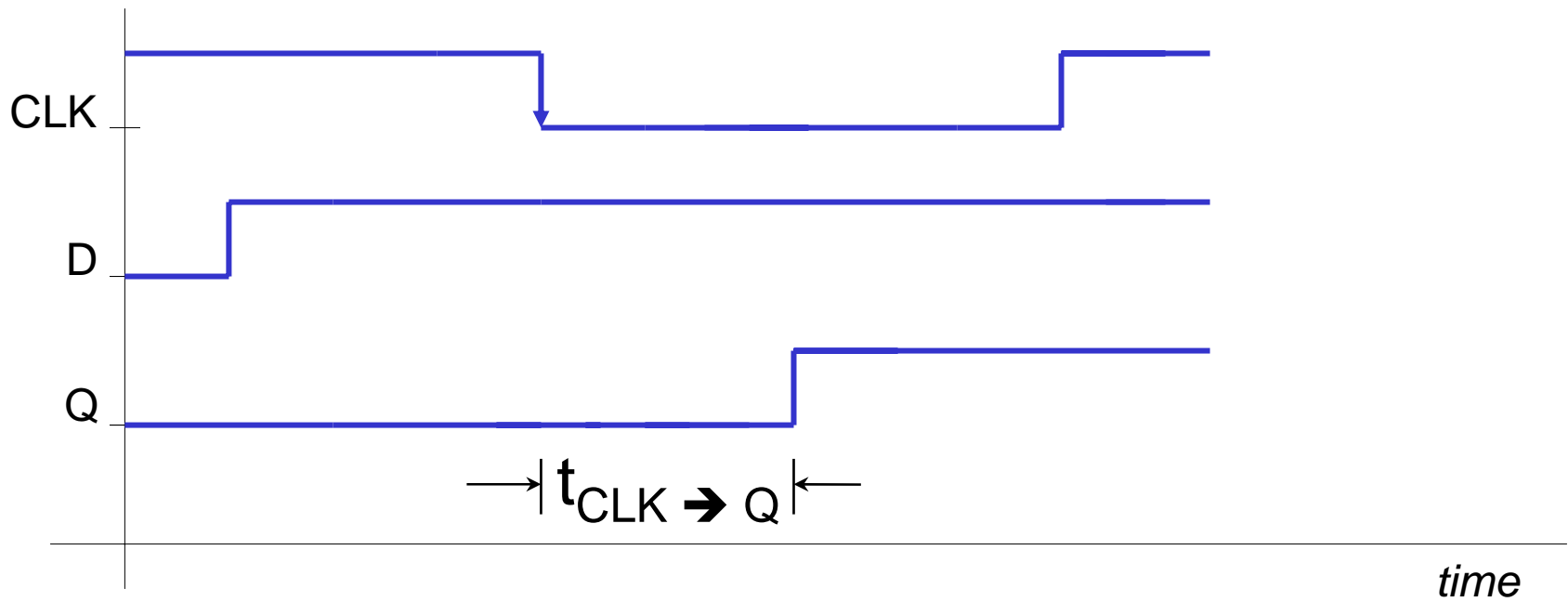
Flip Flop Timing Characteristics

Clock-to-Q Time ($t_{\text{CLK} \rightarrow \text{Q}}$)

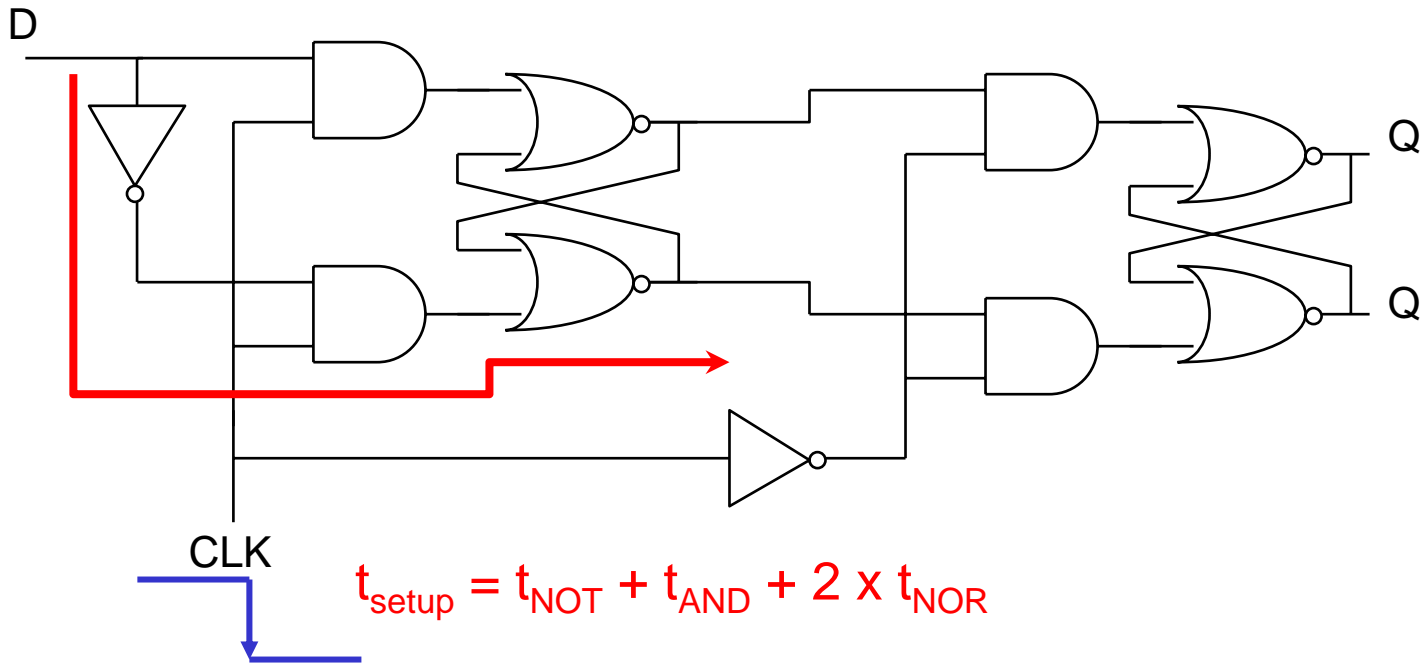


The output does not change instantaneously...

$t_{\text{CLK} \rightarrow \text{Q}}$

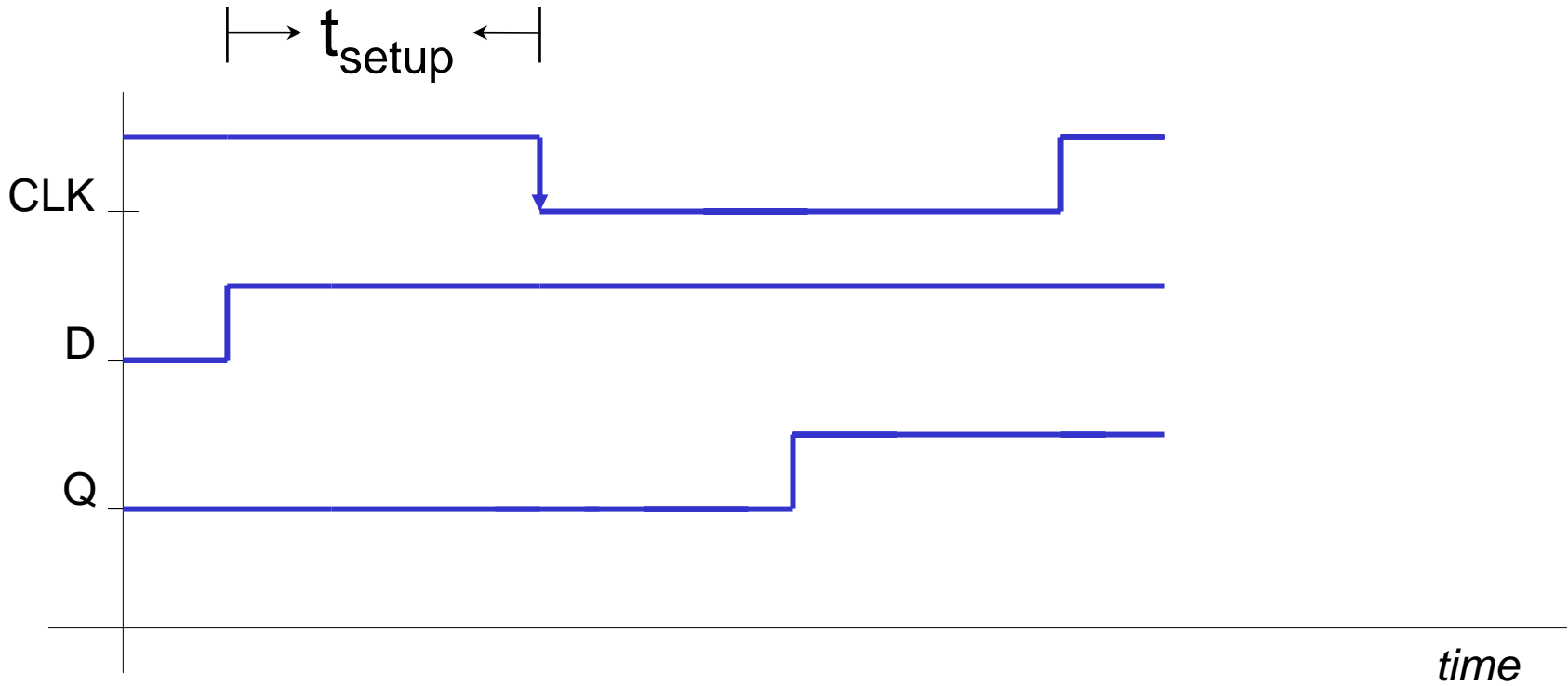


Setup Time (t_{setup})

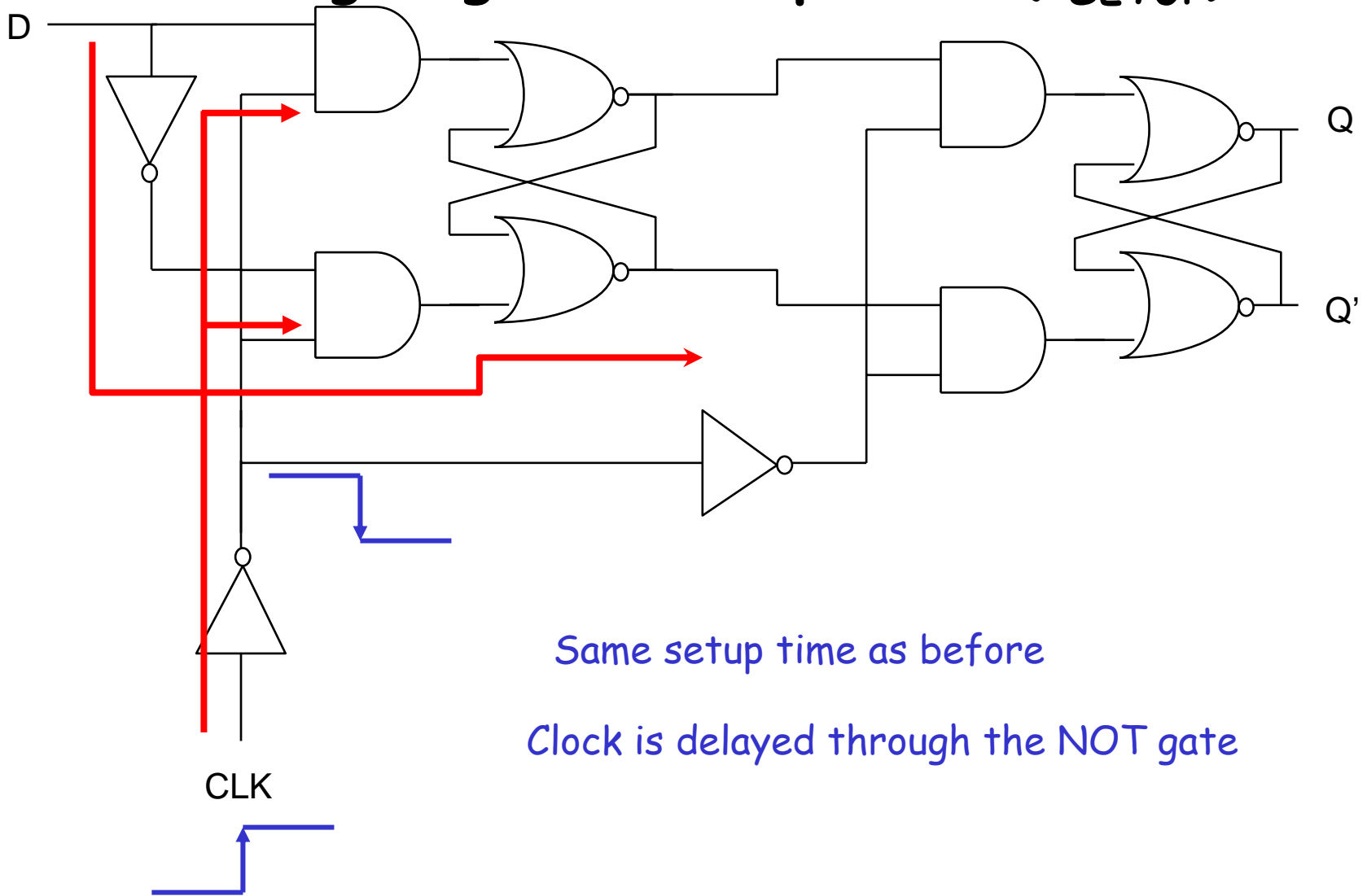


The input has to get there early enough to set the master latch before the clock turns off...

t_{setup}

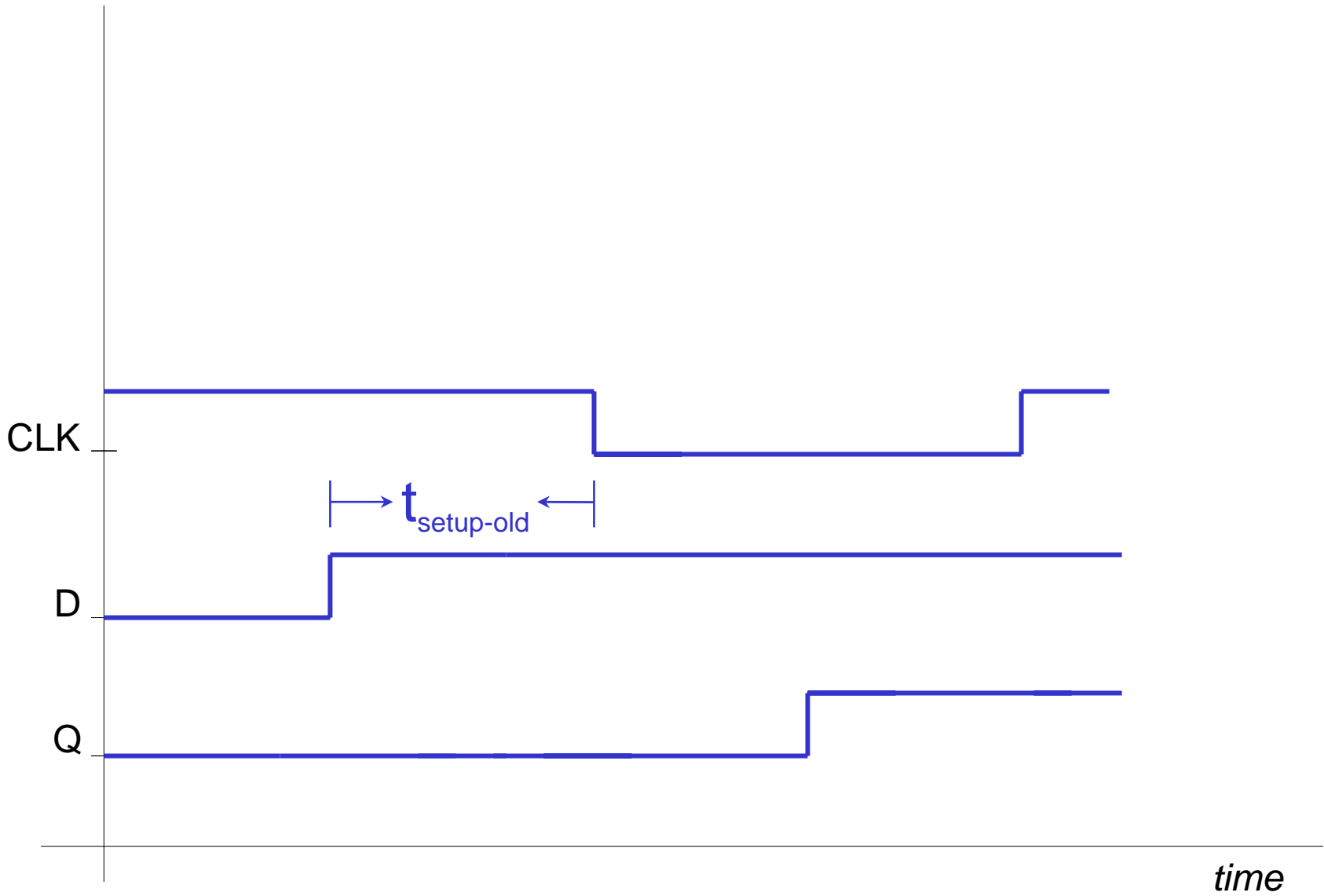


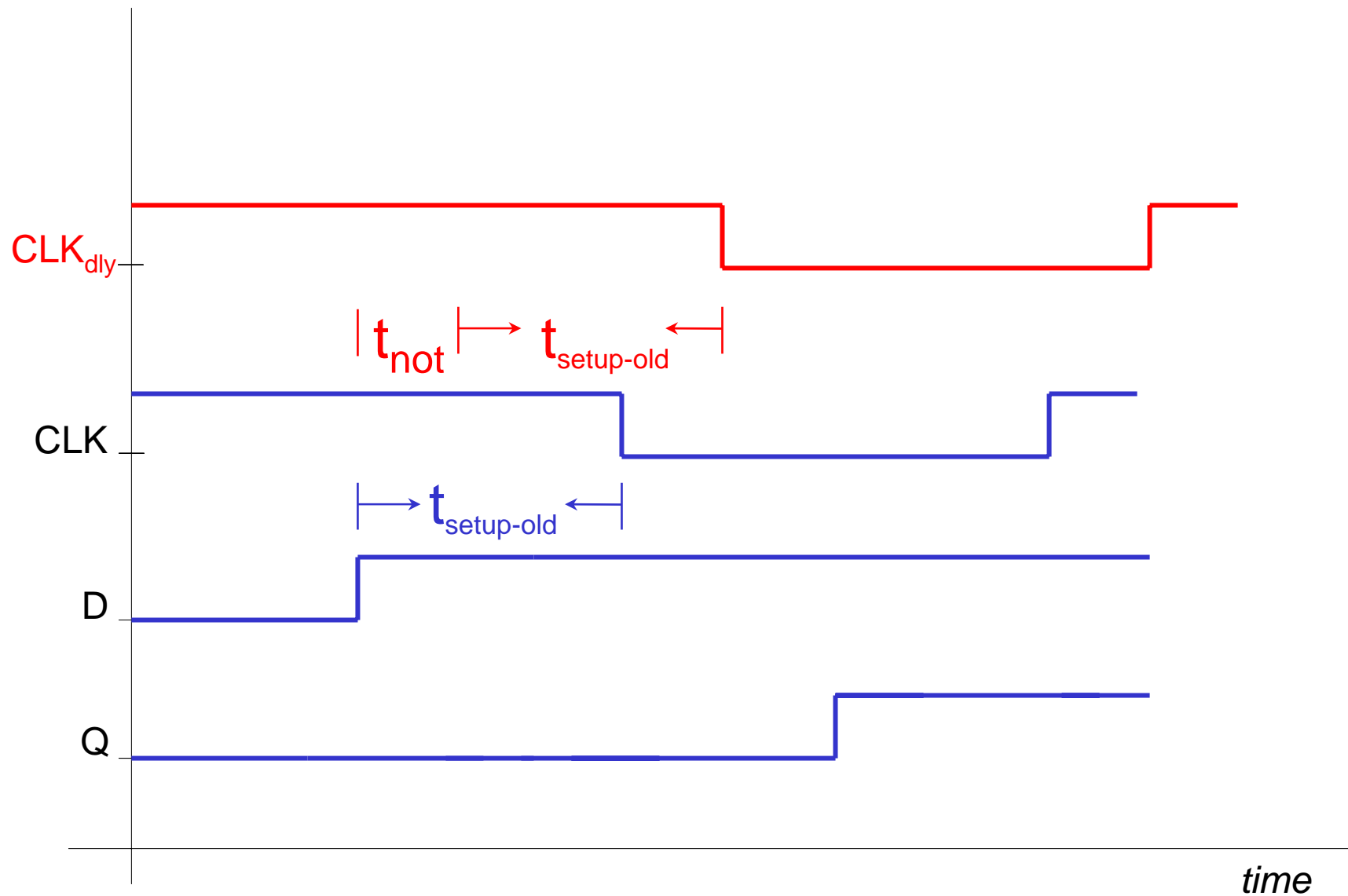
Rising Edge FF Setup Time (t_{SETUP})

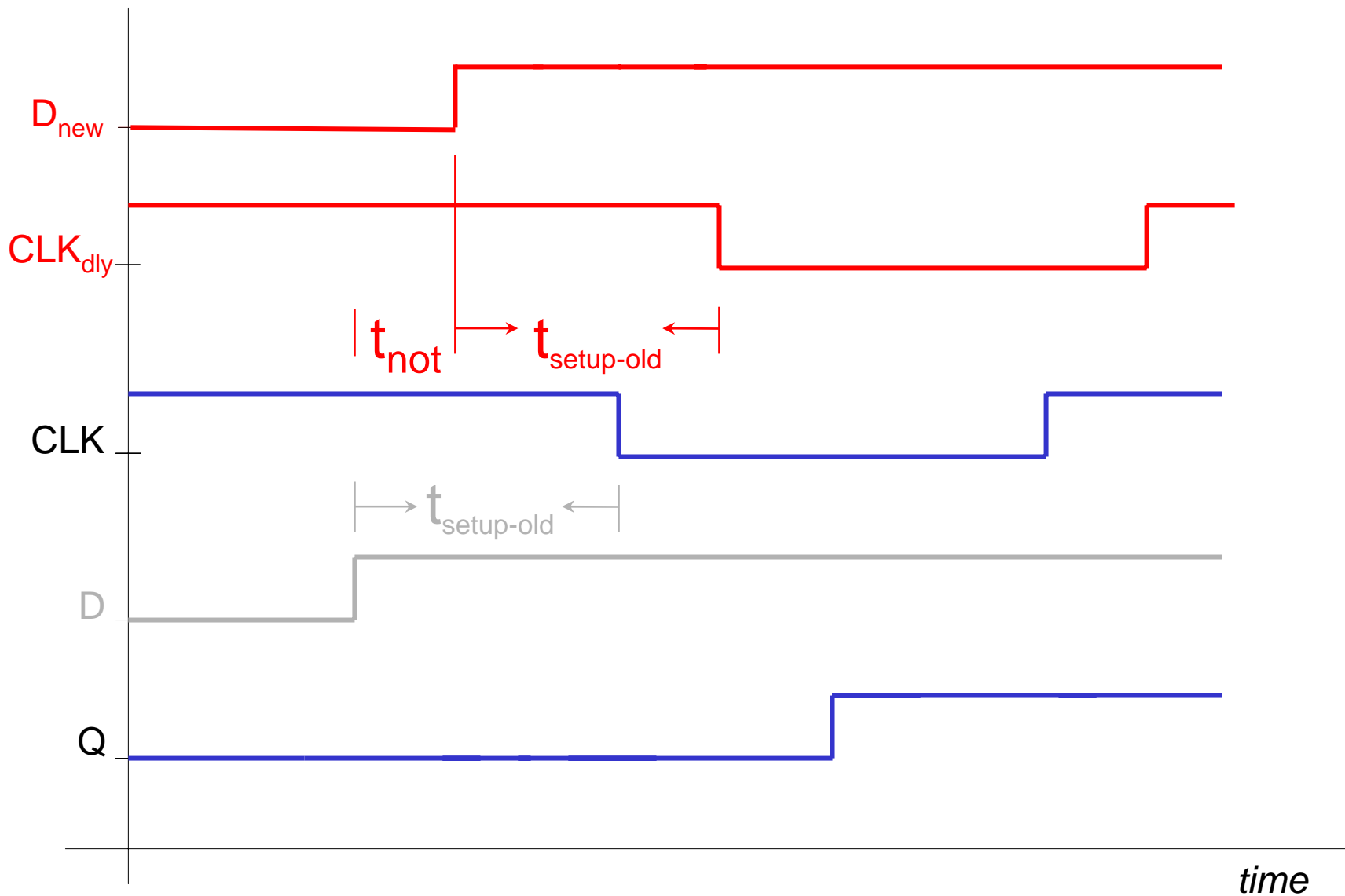


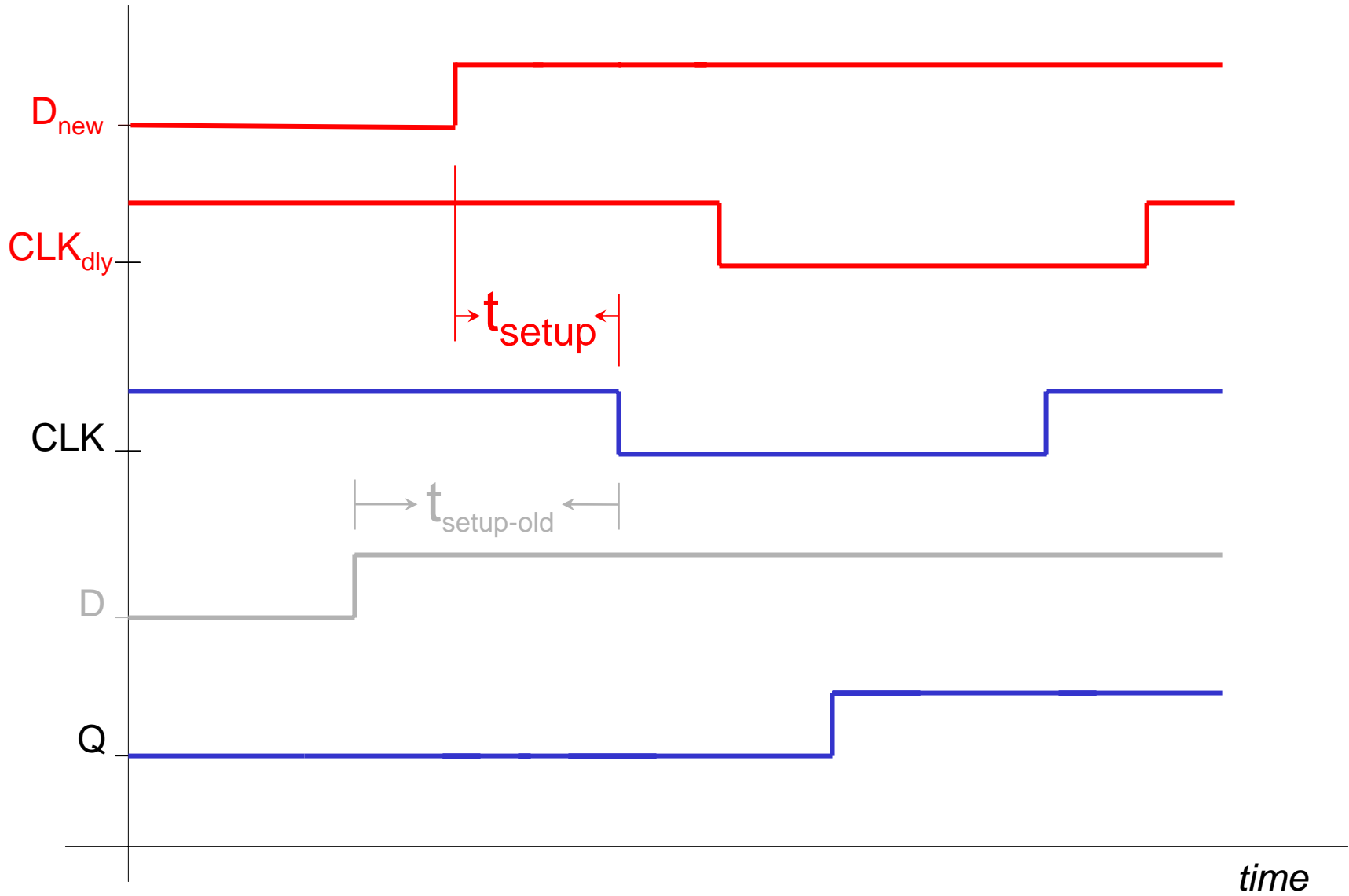
Same setup time as before

Clock is delayed through the NOT gate

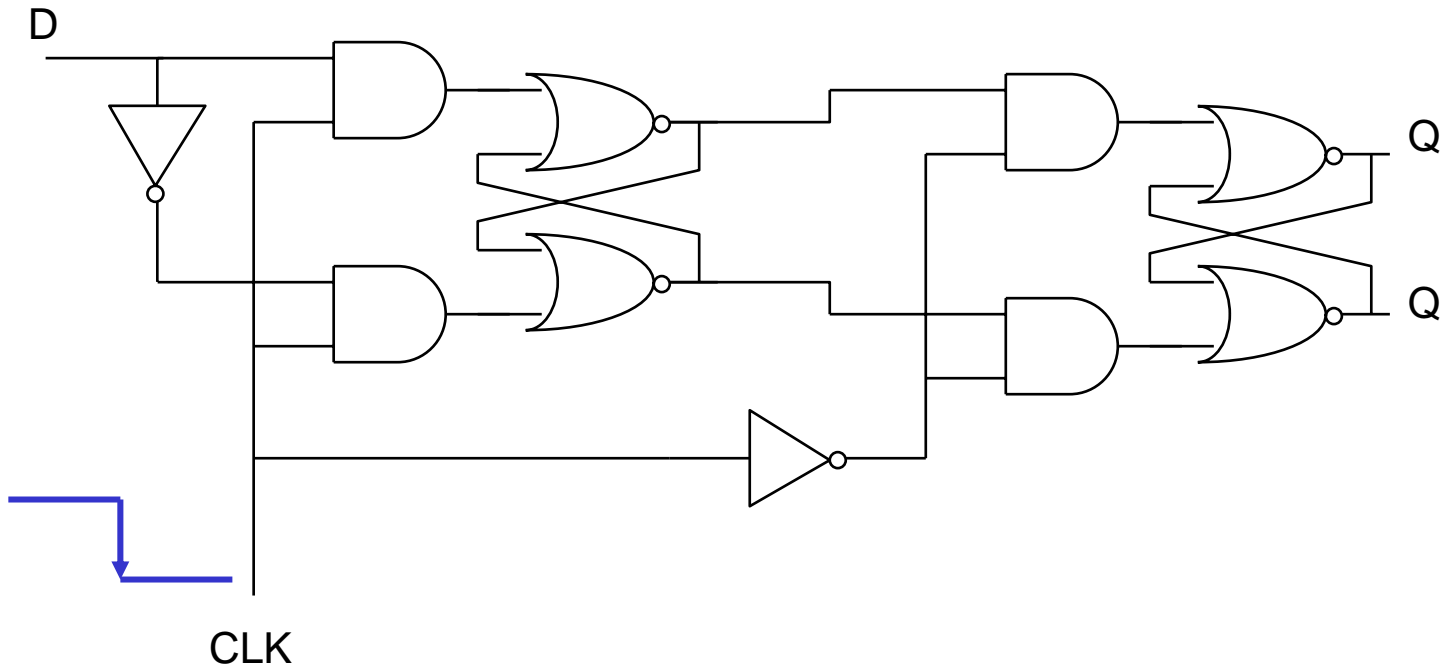








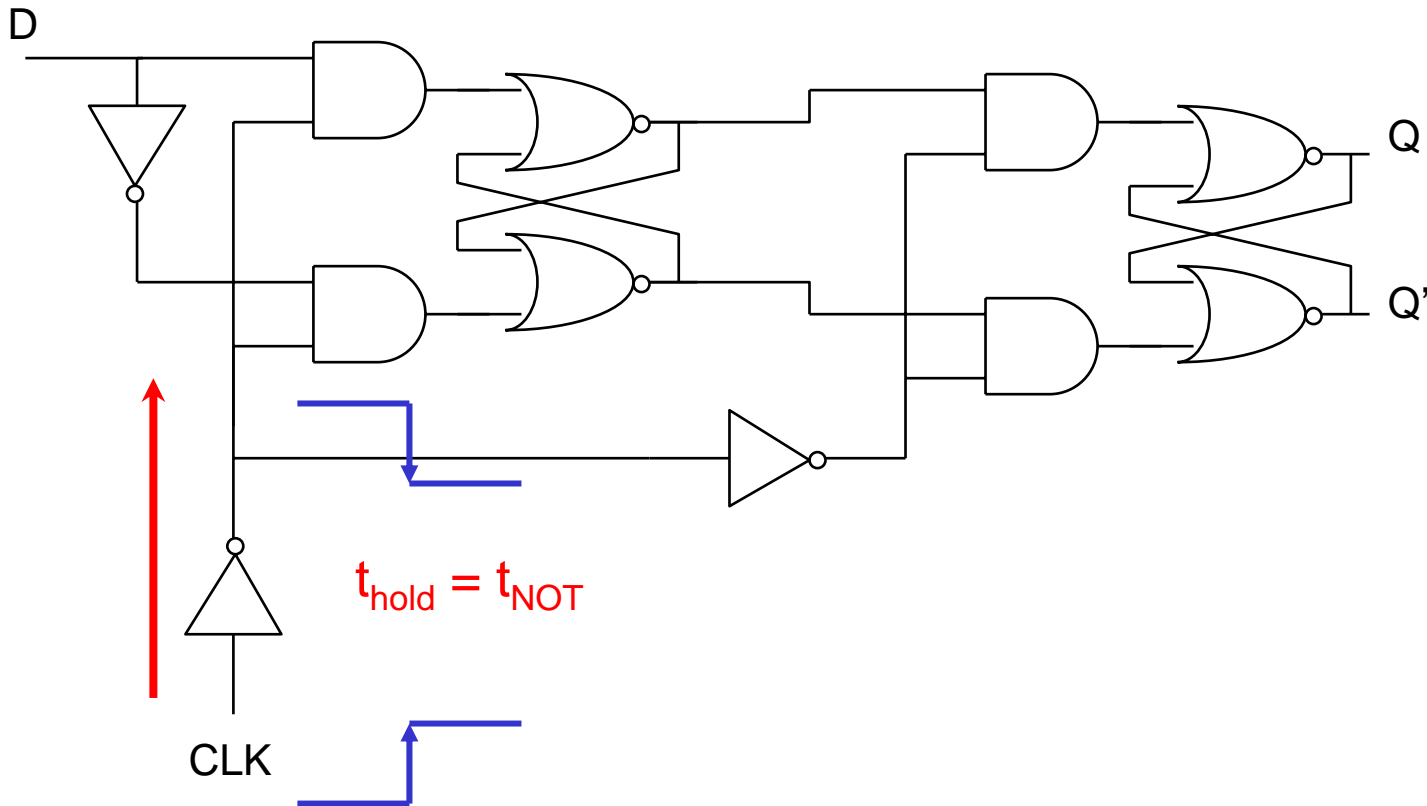
Falling Edge Hold Time (t_{hold})



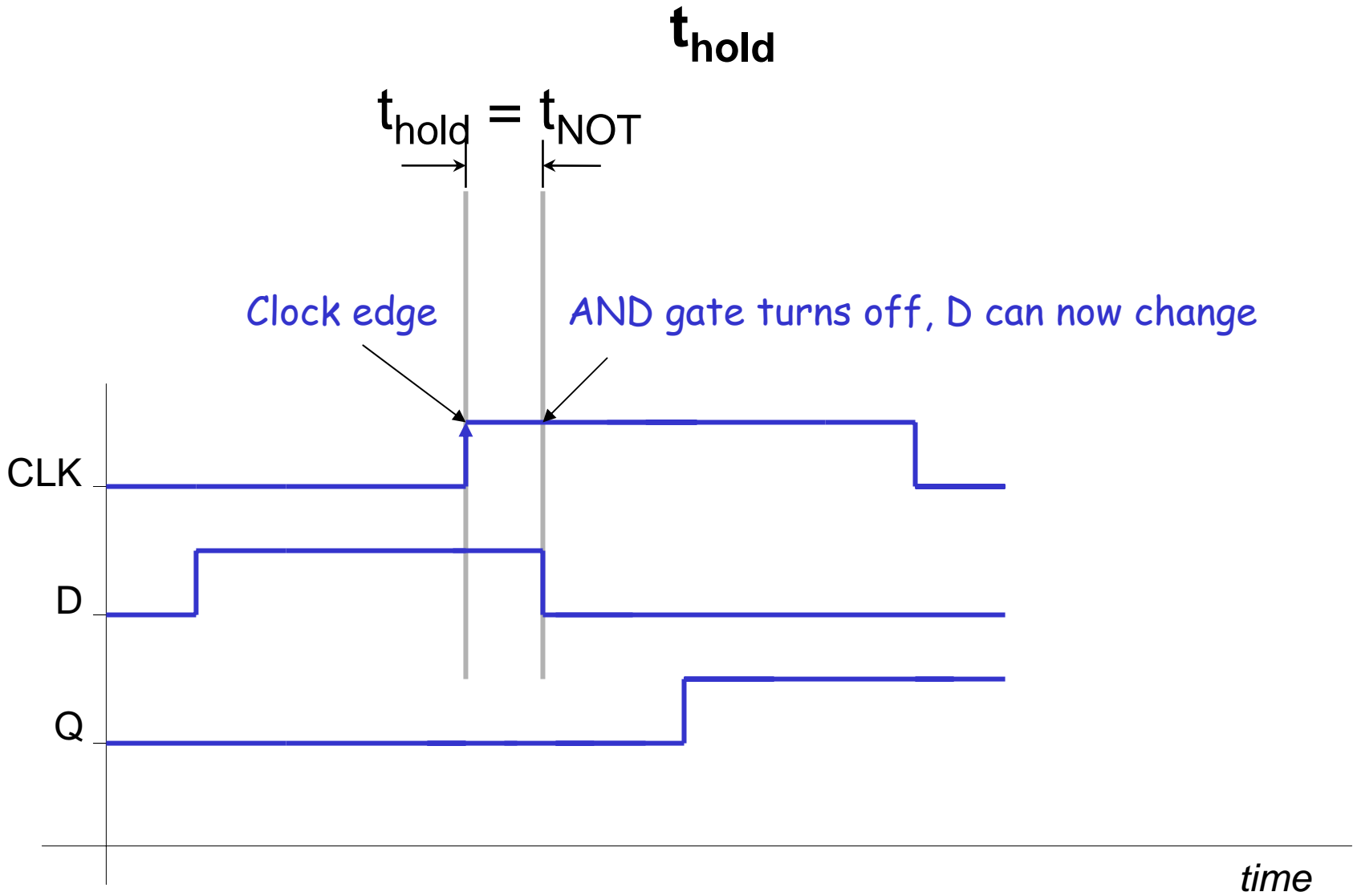
$t_{\text{hold}} = 0\text{ns}$ (AND gates turn off immediately)

You have to keep the old D value there until the AND gates are shut off... (but no longer)

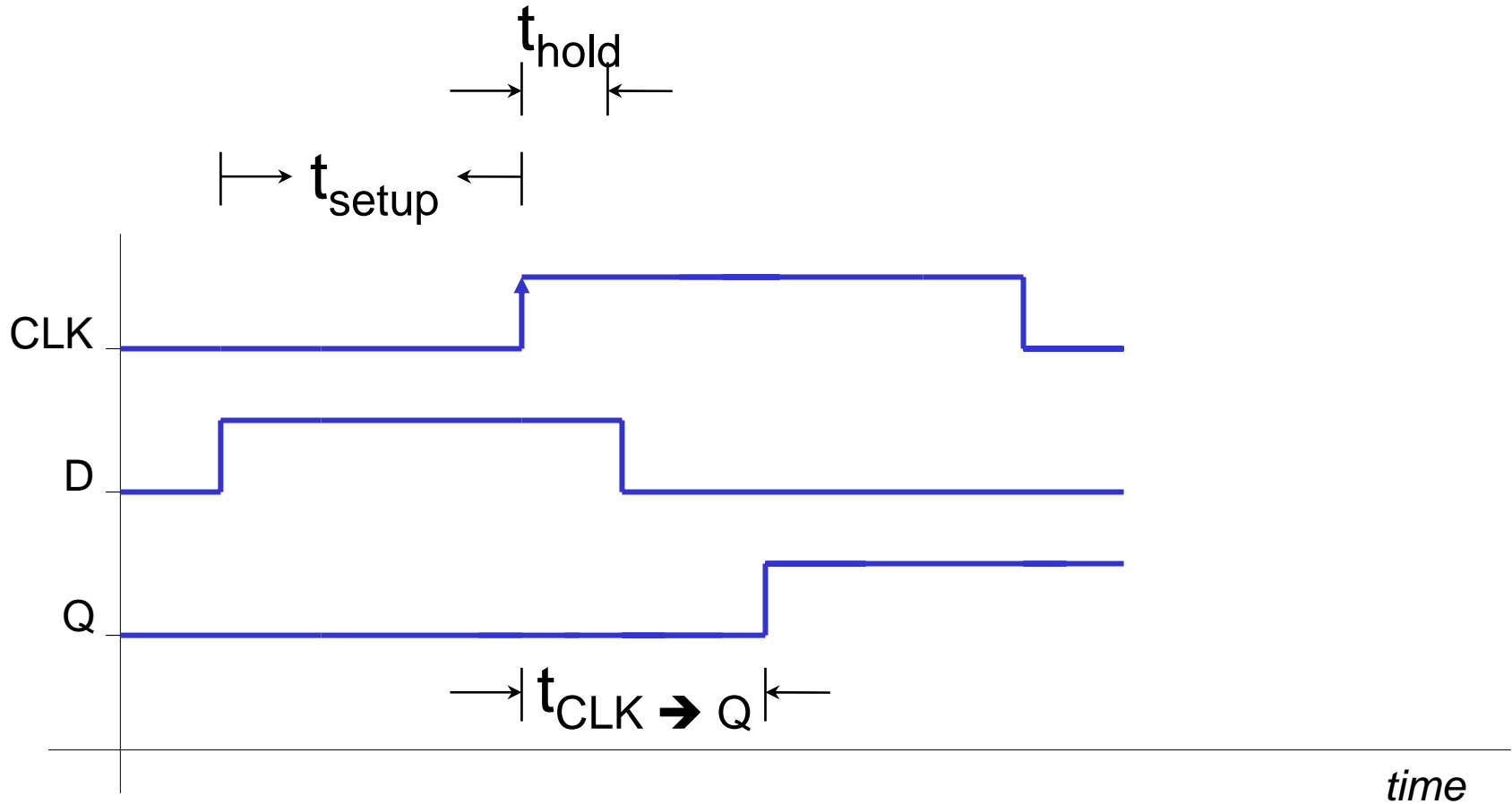
Rising Edge Hold Time (t_{hold})



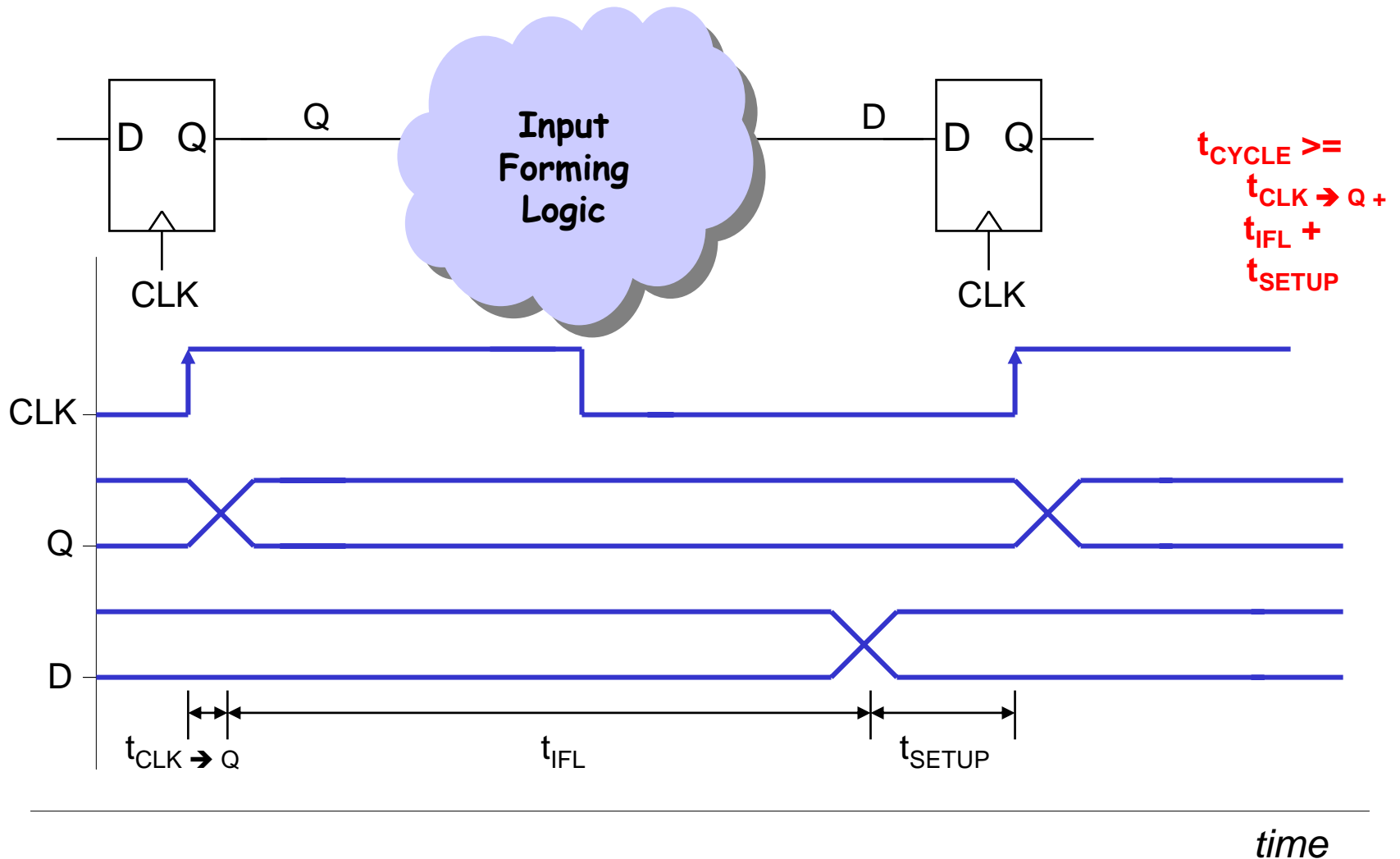
You have to keep the old D value there until the AND gates are shut off...



Flip Flop Timing



Timing of a Synchronous System



Example of a Synchronous System

