

**ECE 238L**  
**Digital Computers and Number Systems**  
**Lecture lab 3**

September 14, 2006

## Problem 2.3a

$$\begin{aligned}AB + BC'D' + A'BC + C'D &= B + C'D \\B(A + A'C) + C'(D + BD') &= \\B(A + AC + A'C) + C'(D + BD + BD') &= \\B(A + C) + C'(D + B) &= \\AB + BC + C'D + B'C &= \\B(C + C' + A) + C'D &= \\B(1 + A) + C'D &= \\B + C'D &= \end{aligned}$$

## Problem 2.3b

$$\begin{aligned}wy + w'yz' + wxz + w'xy' &= wy + w'xz' + x'yz' + xy'z \\&= wy + wxyz + w'xyz' + w'xy'z' + \\&\quad wx'yz' + w'x'yz' + wxy'z + w'xy'z \\&= wy + w'xyz' + w'x'yz' + wxyz + \\&\quad wxy'z + w'xy'z + w'xy'z' + wx'yz' \\&= wy + wx'yz' + w'yz'(x + x') + wxz(y + y') \\&\quad + w'xy'(z + z') \\&= wy(1 + x'z') + w'yz' + wxz + w'xy' \\&= wy + w'yz' + wxz + w'xy'\end{aligned}$$

## Problem 2.3b

$$\begin{aligned} AC' + A'B + B'C + D' &= (A' + B' + C' + D')(A + B + C + D') \\ &= AA' + AB' + AC' + AD' + \\ &\quad A'B + BB' + BC' + BD' + \\ &\quad A'C + B'C' + CC' + CD' + \\ &\quad A'D' + B'D' + C'D' + D'D' \\ &= AB' + AC' + A'B + BC' + A'C \\ &\quad + B'C + D' + AB'C' \\ &= AB'C + AB'C' + AC' + A'B + ABC' + A'BC' + \\ &\quad A'BC + A'B'C + B'C + D' \end{aligned}$$

## Problem 2.3b

$$\begin{aligned} AC' + A'B + B'C + D' &= \\ &= AC' + AB'C' + A'BC' + \\ &\quad A'B + A'BC + A'BC' + \\ &\quad B'C + AB'C + A'B'C + D' \\ &= AC'(1 + B' + B) + A'B(1 + C' + C) + \\ &\quad B'C(1 + A + A') + D' \\ &= AC' + A'B + B'C + D' \end{aligned}$$

# Problem Statement

Design a circuit which selects between two inputs (A and B) and pass the selected input to the output Q.

The desired circuit is called a multiplexer or mux.

# Multiplexers

| A | B | S | F |
|---|---|---|---|
| 0 | 0 | 0 |   |
| 0 | 0 | 1 |   |
| 0 | 1 | 0 |   |
| 0 | 1 | 1 |   |
| 1 | 0 | 0 |   |
| 1 | 0 | 1 |   |
| 1 | 1 | 0 |   |
| 1 | 1 | 1 |   |

# Multiplexers

| A | B | S | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

# Multiplexers

| A | B | S | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

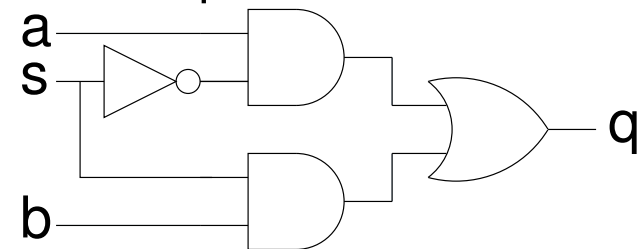
|   |   | ab |    |    |    |
|---|---|----|----|----|----|
|   |   | 00 | 01 | 11 | 10 |
| s | 0 | 0  | 0  | 1  | 1  |
|   | 1 | 0  | 1  | 1  | 0  |

# Multiplexers

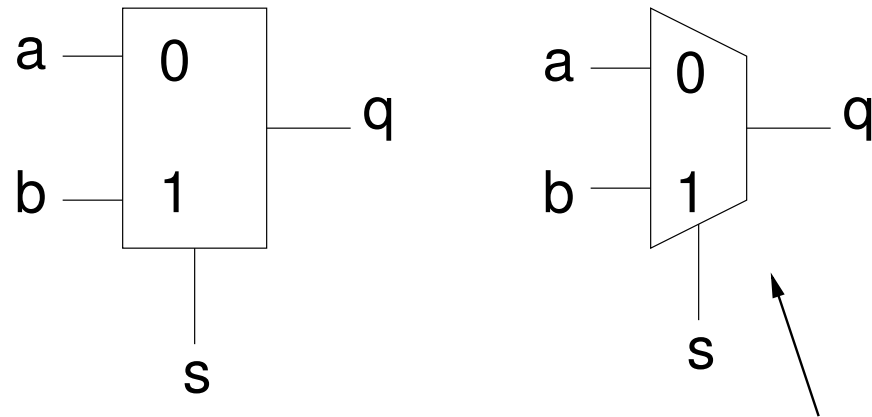
| A | B | S | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

| s \ ab | ab |    |    |    |
|--------|----|----|----|----|
|        | 00 | 01 | 11 | 10 |
| 0      | 0  | 0  | 1  | 1  |
| 1      | 0  | 1  | 1  | 0  |

$$q = s'a + sb$$

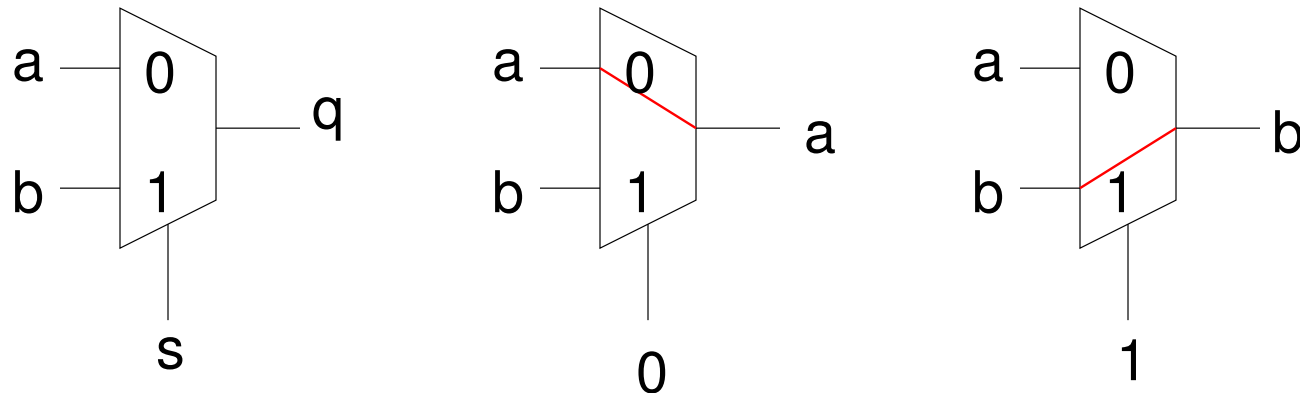


# Multiplexer Symbols



This is the preferred symbol.

# Data Steering



Key idea: The select input wire selects one of the inputs and passes it out to the output.