MSFF

Master/Slave Flip Flops
A Master/Slave Flip Flop (D Type)

Gated D latch (master)       Gated D latch (slave)

D   Q         D   Q
Gate  Gate

Q1

GATE

Either:

The master is loading (the master is on)
or
The slave is loading (the slave is on)

But never both at the same time...
DFF Timing

Master Loads  Slave Loads  Master Loads  Slave Loads  Master Loads  Slave Loads

Gate

D

Q1

Q

time

ECE 238L
Output Changes in Response to Falling Clock

D   Q
Gate

D   Q
Gate

GATE

Master Loads
Slave Loads
Master Loads
Slave Loads
Master Loads
Slave Loads

CLK
D
Q1
Q
DFF Detailed Schematic

Master latch (D)

Slave latch (SR)

Usually call the gate "CLK"
A Falling Edge Triggered DFF

Edge-triggered

Falling edge triggered

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Oscillator (Toggle Circuit) Operation

CLK → D → Q

CLK
Q

time
Rising Edge Triggered DFF Schematic

Edge-triggered

Rising edge triggered
Oscillator (Toggle Circuit) Operation

D

Q

CLK

CLK

Q

Q

time
D Flip Flop Transition Table

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<tr>
<th>D</th>
<th>Q</th>
<th>Q+</th>
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Q+ = D

No clock shown since it is edge triggered (assumed)
Falling vs. Rising Edge Triggered

\[ D \quad Q \quad Q_{\text{fall}} \]
\[ D \quad Q \quad Q_{\text{rise}} \]

CLK

CLK

D

Q_{\text{fall}}

Q_{\text{rise}}
Alternative Flip Flops

T

JK
Toggle Flip Flop

\[ Q^+ = T' \cdot Q + T \cdot Q' = T \oplus Q \]

Clock edge is assumed in this transition table...
Toggle Flip Flop

Q+ = T′•Q + T•Q′ = T ⊕ Q

An oscillator with an enable input (T)
Toggle Flip Flop

T

CLK

Q
JK Flip Flop

Kind of a cross between a SR FF and a T FF

<table>
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<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q+</th>
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\[ Q^+ = K' \cdot Q + J \cdot Q' \]
JK Flip Flop
Why Alternative FF’s?

• With discrete parts (TTL family)
  - JK or T FF’s could reduce gate count for the input forming logic
  - Extensively used

• With VLSI IC’s and FPGA’s
  - JK or T FF’s must be built from DFF+gates
  - Larger, slower than a DFF
  - Not used
Flip Flops With Additional Control Inputs
What is this?
What is this?

A falling edge triggered, D-type FF with enable

Master only loads when CLK=Enable='1'
What is this?
What is this?

A falling edge triggered, D-type FF with an *asynchronous* set

If Set=1 then Q=1, regardless of CLK or D
What is this?

[Diagram of a circuit with inputs D and CLK, and outputs Q and Q']
What is this?

A falling edge triggered, D-type FF with a synchronous set

If Set=1 then Q=>1 on the next falling edge of the clock, regardless of D
Flip Flops With Additional Control Inputs

• A variety of FF’s have been made over the years
• They contain combinations of these inputs:
  - Enable
  - Set
  - Reset
• The Set and Reset can be either:
  - Asynchronous (independent of CLK)
  - Synchronous (work only on CLK edge)
Flip Flop Timing Characteristics
Clock-to-Q Time ($t_{CLK\rightarrow Q}$)

The output does not change instantaneously...

Why $2 \times t_{NOR}$?
$t_{CLK} \rightarrow Q$
Setup Time \( (t_{\text{setup}}) \)

\[
t_{\text{setup}} = t_{\text{NOT}} + t_{\text{AND}} + 2 \times t_{\text{NOR}}
\]

The input has to get there early enough to set the master latch before the clock turns off...
$t_{\text{setup}}$
Rising Edge FF Setup Time ($t_{\text{SETUP}}$)

Same setup time as before

Clock is delayed through the NOT gate
The diagram shows the timing diagram for a digital circuit, specifically a JK flip-flop. The horizontal axis represents time, and the vertical axis represents the values of the signals CLK, D, and Q. The signal CLK is a clock signal, and D is the data input signal. Q is the output of the flip-flop.

The notation $t_{\text{setup-old}}$ indicates the old setup time, which is the time interval required for the data input (D) to be stable before the clock (CLK) edge to avoid setup violations. The diagram illustrates how the data input (D) and the clock (CLK) signals interact in the time domain, with $t_{\text{setup-old}}$ being the critical timing parameter for proper operation.
Falling Edge Hold Time ($t_{\text{hold}}$)

$t_{\text{hold}} = 0\text{ns}$  (AND gates turn off immediately)

You have to keep the old D value there until the AND gates are shut off... (but no longer)
Rising Edge Hold Time \((t_{\text{hold}})\)

\[ t_{\text{hold}} = t_{\text{NOT}} \]

You have to keep the old D value there until the AND gates are shut off...
\[ t_{\text{hold}} = t_{\text{NOT}} \]

Clock edge

AND gate turns off, D can now change
Flip Flop Timing

\[ t_{\text{hold}} \]

\[ t_{\text{setup}} \]

\[ t_{\text{CLK} \rightarrow Q} \]
Timing of a Synchronous System

\[ t_{\text{CYCLE}} \geq t_{\text{CLK}} \rightarrow Q + t_{\text{IFL}} + t_{\text{SETUP}} \]
Example of a Synchronous System

One transition per clock edge...