University of New Mexico

Department of Electrical and Computer Engineering

ECE 321 – Electronics I (Fall 2009) Exam 2

Name: Solution Date: Oct. 23, 2009

Note: Only calculator, pencils, and pens are allowed.

1. (10 points) True or false:

(a) In a CMOS inverter, the maximum short circuit current occurs when the input voltage is at the switching threshold voltage. (T)

(b) By definition, V_{IL} is maximum input voltage of a logic gate that still can be detected as zero. (T)

(c) The dynamic power in a CMOS inverter is the amount of power that is consumed in the load capacitor. (F)

(d) To have a better noise margin in logic gates, it is better to maximize V_{oH} and minimize V_{IH}. (T)

(e) In a CMOS inverter, reducing the NMOS threshold voltage, V_{tn}, reduces the low-to-high propagation delay, t_{pLH}. (F)

2. (15 points) Compute the leakage power consumption in a C MOS inverter that is used in a clock distribution network of a digital circuit using 90nm technology node. Assume that the V_{DD} is 1.2 V, $I_{OFF(NMOS)}$=12 nA/um, and $I_{OFF(PMOS)}$=26 nA/um, $(W/L)_n$= 650, $(W/L)_p$= 950, and L=90nm.

$P_{leakage} = \frac{1}{2} V_{DD} \left(I_{off(nmos)} + I_{off(pmos)} \right)$

$W_n = 58.5\,\mu m$ $\quad I_{off(nmos)} = 702\,nA$

$W_p = 85.5\,\mu m$ $\quad I_{off(pmos)} = 2223\,nA$

$P_{leakage} = \frac{1}{2} * 0.5 * (702nA + 2223nA) = 1.755\,\mu W$

3. (20 points) You are given two digital systems, A and B, and are asked to connect the outputs of system A to the inputs of system B. The power supply voltage for system B is 1.5V, but the power supply voltage of system A is slightly less; at 1.2V.

(a) Assume that all the logic gates inside systems A and B can be treated as CMOS inverters. Determine V_{OH} and V_{OL} for the outputs of system A?

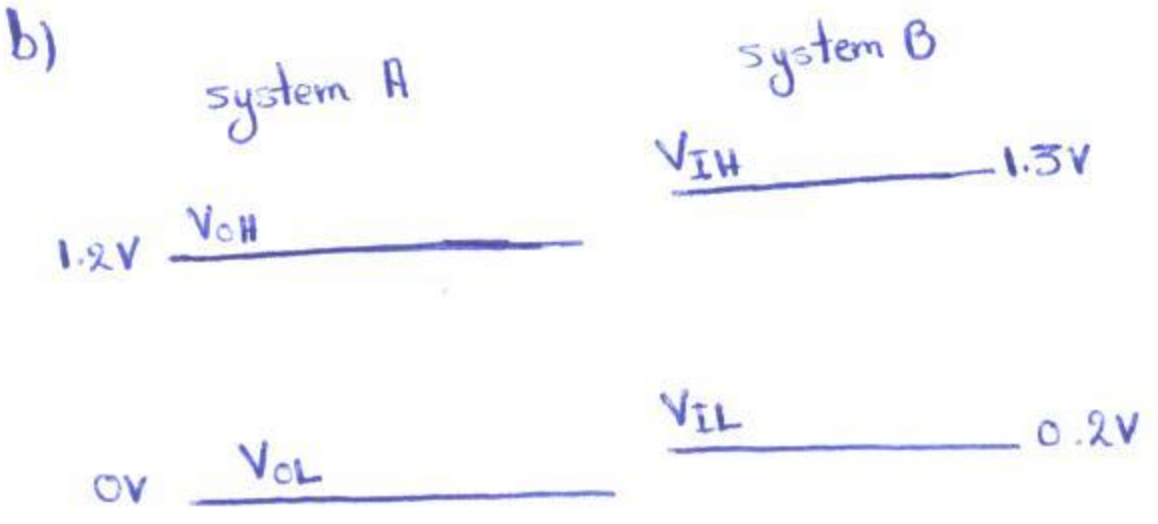
(b) For the system B, assume that V_{IL}=0.2 and V_{IH}=1.3. Draw the noise margin map and compute NMH and NML.

(c) Explain why the overall system won't work.

a) for CMOS inverters operation is "rail-to-rail"

$V_{OH} = V_{DD} = 1,2\,V$ $\quad$ $V_{OL} = 0\,V$

b)

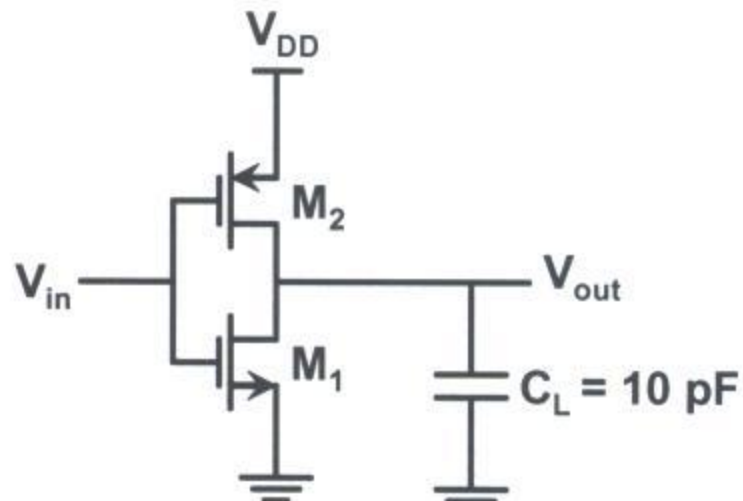


$NMH = V_{OH} - V_{IH} = 1.2 - 1.3V = -0.1V$

$NML = V_{IL} - V_{OL} = 0.2V - 0.0V = 0.2V$

c) The maximum output of A is below the minimum input for high logic of system B. When A tries to communicate a logic high, it will appear as undefined logic to system B.

4. (30 points) We would like to design an inverter to drive a long interconnect (clock line) with effective capacitance of 10 pF. By computing the *average current* that charges/discharges C_L, determine $(W/L)_P$ such that t_{PLH} = 250 ps. Assume that V_{DD}= 2.5V, V_{tp}= -0.4 V, and K'_p= -60 μA/V^2.



$$I_{av} = \frac{1}{2}\left[I(V_{in}=0 \;\&\; V_{out}=0) + I\left[V_{in}=0,\ V_{out}=\frac{Vdd}{2}\right)\right]$$

↓ nmos off, pmos sat

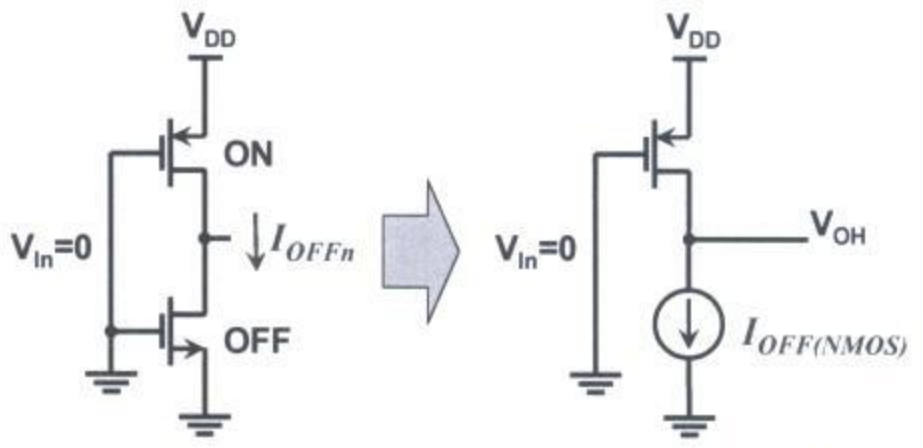
↓ nmos off, pmos linear

$$|I_{av}| = \frac{1}{2}\left[\frac{|K'_p|}{2}\left(\frac{W}{L}\right)_p (V_{DD}-|V_{tp}|)^2 + |K'_p|\left(\frac{W}{L}\right)_p\left((V_{DD}-|V_{tp}|)\frac{V_{DD}}{2} - \frac{Vdd^2}{8}\right)\right]$$

$$|I_{av}| = \frac{1}{2}\left[1.325\times10^{-4}\left(\frac{W}{L}\right)_p + 1.106\times10^{-4}\left(\frac{W}{L}\right)_p\right] = 1.215\times10^{-4}\left(\frac{W}{L}\right)_p$$

$$t_{pLH} = \frac{C_L \times \frac{Vdd}{2}}{I_{av}} \longrightarrow 250ps = \frac{10pF \times 1.25V}{I_{av}} \longrightarrow \left(\frac{W}{L}\right)_p = 411.65$$

5. (25 points) In an ideal CMOS inverter, V_{OH} is equal to V_{DD}. However, the NMOS leakage may slightly reduce V_{OH}. In this problem, we want to calculate the V_{OH} in the presence of NMOS leakage. To measure V_{OH}, you connect the input to the ground, where the PMOS is in *linear region* and the NMOS is in cut off region. However, in the presence of leakage, you can approximate that the NMOS behaves like a current source with the current of $I_{OFF(NMOS)}$ as shown in the circuit below. Compute V_{OH}, if $I_{OFF(NMOS)}$=1 μA, V_{DD}=1.0 V, V_{tp}=-0.4 V, K'_p=-40 μA/V^2, and $(W/L)_p$=2.



$$|I_{offn}| = |K'_P| \left(\frac{W}{L}\right)_p \left[(V_{dd} - |V_{tp}|)(V_{dd} - V_{oH}) - \frac{(V_{dd} - V_{oH})^2}{2} \right]$$

$$1\mu A = 40\mu A/V^2 * 2 * \left[(1 - 0.4)(1 - V_{oH}) - \frac{(1 - V_{oH})^2}{2} \right]$$

$$V_{oH} = 0.9787\ V$$