heat since they are designed for very high speed to expedite the digital traffic. Server system powers run from low end of about 200 W to over 15 kW for high-volume applications.

The point is that every fraction of a watt should be challenged. A design that burns 1 W less than another design and has one million ICs manufactured per year will save one million watt-hours of user's energy. Integrated circuit designs are manufactured in the millions and billions during the product life. The impact of lower power design is huge. This book will not detail the many tricks and theory of low power design but will later include some theory and problems to sensitize us to a paramount specification. By the way, the 100 -watt PC example gives the same calculation for the yearly coal burned for a 100 W light bulb.

### 1.10. Summary

This chapter reviewed basic logic theory and analysis of circuits with power supplies, resistors, capacitors, and diodes. Kirchhoff's current and voltage laws were combined with Ohm's law to calculate node voltages and element currents for a variety of circuits. The technique of solving for currents and voltages by inspection is powerful for rapid insight into the nature of circuits. Finally, the diode illustrated circuit analysis with a nonlinear element. The problems at the end of the chapter should provide sufficient drill to prepare for subsequent chapters that will introduce the MOSFET transistor and its simple logic configurations.

## Bibliography

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## Exercise

## Logic Gates and Boolean Functions

When signal invert symbols appear in the following figures, do not draw an inverter; treat an inverted signal as it is.

1-1. (a) Draw the logic gate implementation for the Boolean function $G=A(B+C) \times$ ( $D \bar{E} F$ ).
(b) Draw the logic gate implementation for the Boolean function $G=(A+B) \times$ $(C+D \bar{E} F)$.

1-2. (a) Draw the logic gate implementation for the Boolean function $F=$ $(W \bar{X})(Y+Z)$.
(b) Write the DeMorgan equivalent Boolean statement in part (a) and draw its logic gate schematic.

1-3. Write the DeMorgan equivalent Boolean statement and draw its logic gate schematic for
(a) $F=A(\bar{B}+D)+E F$
(b) $F=(A+B C) D$

1-4. Draw the DeMorgan equivalent logic gate circuit for


## Boolean and Logic Gate Reduction

1-5. Minimize the function $F=X+\overline{X+Y}+X Y$
1-6. Minimize the function $F=\overline{\overline{X Y}+\overline{Z Y}}$.
1-7. Minimize the function $F=\overline{X Y}+\overline{Z Y}$ putting it in a logical inverter form.

1-8. Reduce to the logic circuit to its minimum function.


1-9. Reduce this logic gate circuit to its minimum function using Boolean reduction.


## Terminal Resistance by Inspection

1-10. Write the shorthand expression for $R_{e q}$ between the terminals.


1-11. Write the shorthand expression for $R_{e q}$ between the terminals.


## Voltage Dividers by Inspection

1-12. (a) Write the $V_{o}$ expression by inspection and solve for $V_{o}$ using a voltage divider.
(b) Write the $V_{o}$ expression by inspection and solve for $V_{o}$ using a current divider.


1-13. Calculate $V_{o}$ by first writing a voltage divider expression and then numerically solving for $V_{o}$ for both circuits.

(a)

(b)

1-14. (a) Write the $V_{o 1}$ expression by inspection and solve for $V_{o 1}$ using a voltage divider.
(b) Write the $V_{o 2}$ expression by inspection and solve for $V_{o 2}$ using a voltage divider.


Current Dividers by Inspection
1-15. Repeat Problem 1-14, but solve by including a current divider.

1-16. Write the general expressions and solve for all resistor currents.

$\mathbf{1 - 1 7}$. Given the circuit

(a) Write the expression for $I_{450}$ and solve.
(b) Write the expression for $V_{800}$ and solve.
(c) Show that $I_{800}+I_{400}=2 \mathrm{~mA}$.

1-18. (a) Calculate $V_{o}$ using a voltage divider written by inspection
(b) Calculate $I_{2 M}$ using a current divider written by inspection.


1-19. For the circuit
(a) Solve for $V_{o}$ using a voltage divider expression.
(b) Solve for $I_{2 k}$.
(c) Solve for $I_{900}$.


1-20. Calculate $I_{2 k}$ using the circuit analysis technique by inspection.


