University of New Mexico

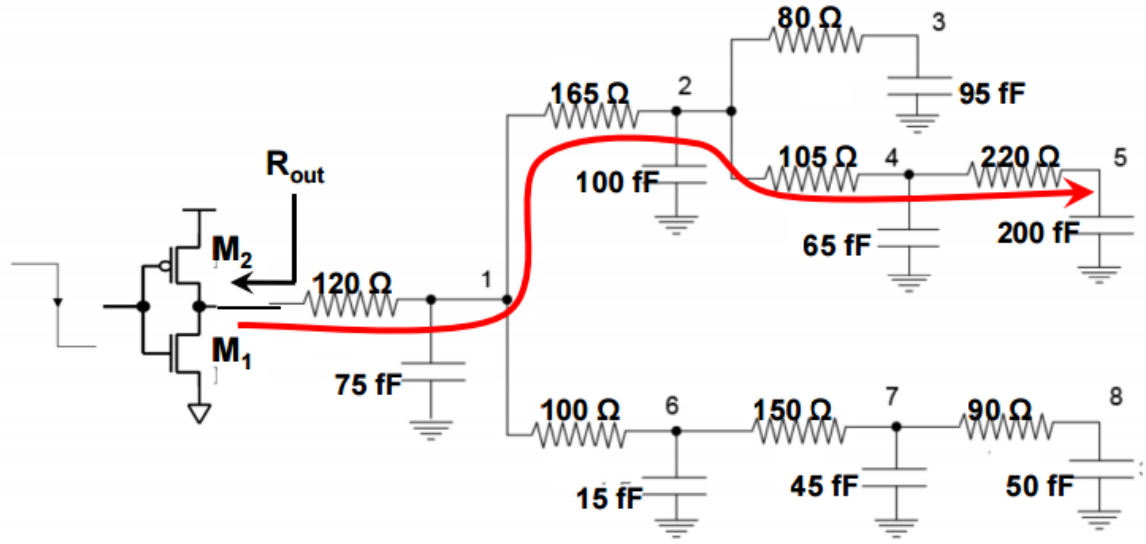
Department of Electrical and Computer Engineering

ECE 321L – Electronics I (Fall 2023) Bonus Homework

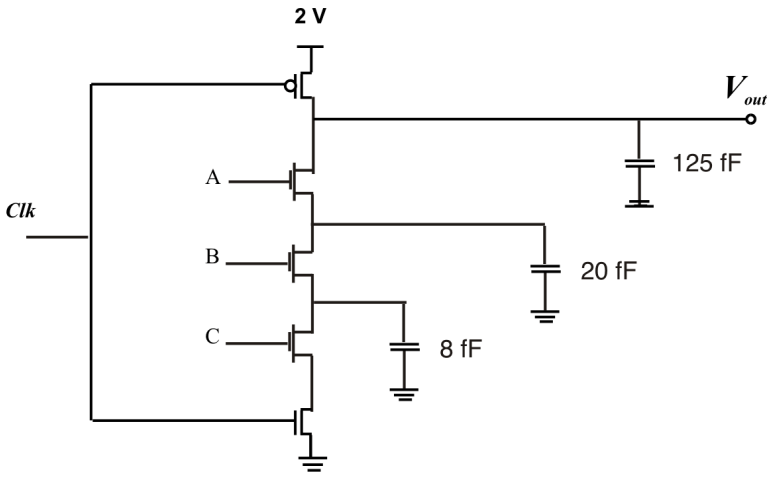
Due in class: Wednesday December 6, 2023

1. Assume that we have an inverter with V_{DD}=1.5 V, K'_n=100 uA/V^2, V_{tn}=0.4 V, λ_n=0.1 V^{-1}, $(W/L)_n$=10, K'_p=60 uA/V^2, V_{tp}=-0.4 V, λ_p=0.2 V^{-1}, $(W/L)_p$=17. Find R_{out}.
Hint: connect a test capacitor of 100fF to the gate, calculate the LH propagation delay (t_{pLH}) using average current technique, then equate the propagation delay to a simple RC network and find R_{out}. This will effectively be $R_{out(LH)}$.

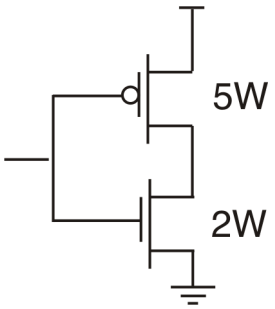
2. We plan to use the inverter of problem 1 in the following circuit. Use Elmore technique to compute the time constant and LH propagation delay (t_{PLH}) of the network from the gate input to node 5.

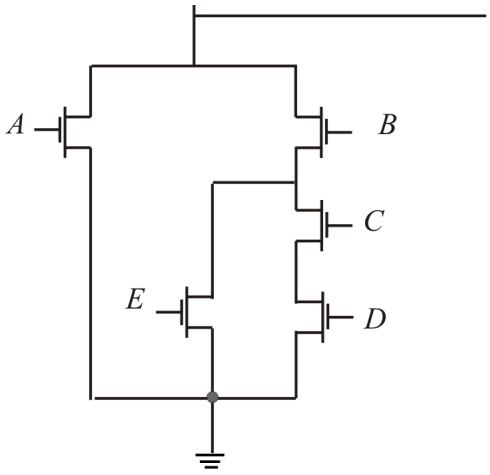


3. During the evaluate phase, $V_A = V_B = 2$ V, and $V_C = 0$ V. Use the charge sharing method, compute the final voltages at the V_{out} and 20 fF and 8 fF capacitors. Assume that V_T=0.7V.



4. Sketch the pull up network, and write the scaling values on the schematic for all transistors with respect to the inverter. What is the Boolean function of this complex CMOS logic gate?





5. Compute the leakage power consumption in a CMOS inverter that is used in a clock distribution network of a digital circuit using 90nm technology node. Assume that the VDD is 1.2 V, $I_{OFF(NMOS)}$=12 nA/um, and $I_{OFF(PMOS)}$=26 nA/um, $(W/L)_n$= 650, $(W/L)_p$= 950, and L=90nm.

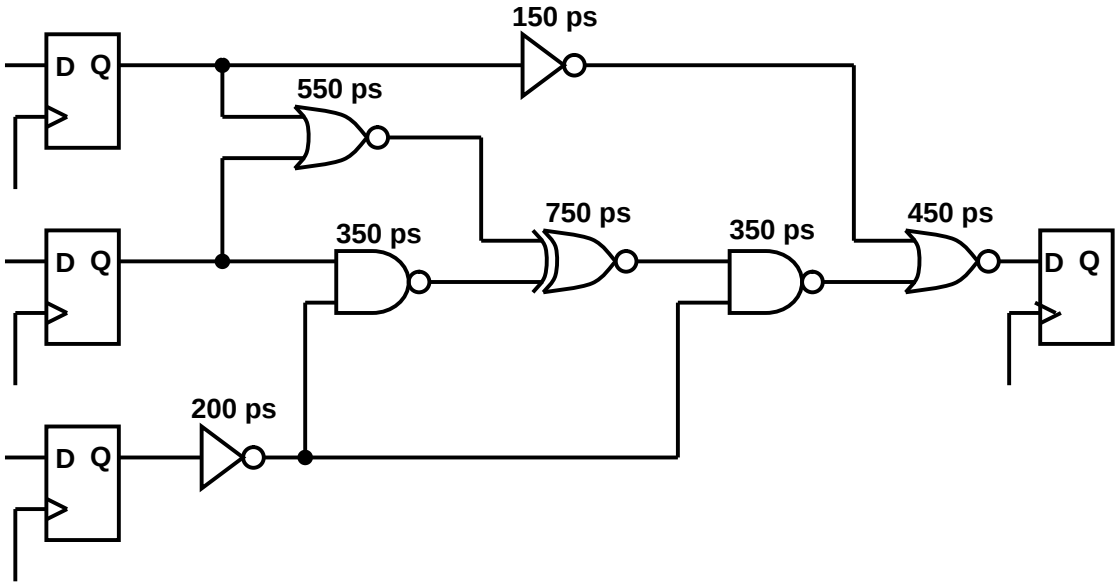
6. Consider the following sequential circuit with 4 edge-triggered flip-flops and some logic gates. Assume that t_{SU} = 3 ns, t_{hold}= 2 ns, and t_{C2Q} = 1 ns.

(a) Identify the path with the maximum delay (critical path) on the schematic.

(b) What is the maximum operating frequency of this circuit?

(c) Identify the path with minimum delay on the schematic.

(d) Does this circuit violate the hold time constraint? Why?



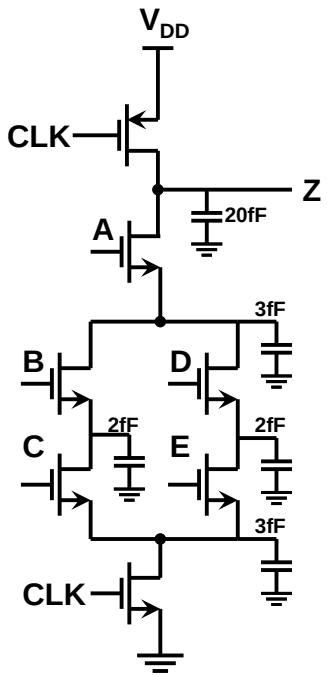
7. The following circuit is a 4-input dynamic logic.

(a) Identify the logic function for the output Z.

(b) What input vector imposes the worst case charge sharing during the evaluation time?

(c) Compute the final voltage at Z, if the input vector is ABCDE=11000 during evaluation after charge sharing. Assume that V_{tn} = 0.4V.

(d) Determine the width of the PMOS such that the maximum worst case pre-charge time delay (0 to 90%) is limited to 250ps. (The worst case is when all the inputs are at V_{DD} such that all the intermediate capacitors contribute to the delay). Assume that V_{DD} = 1.2 V, K'_p = 50 uA/V^2, and V_{tp} = -0.5 V in the 100nm technology node. For simplicity assume that the PMOS will stay in saturation during the transition.



8. Dynamic logic design problem:

(a) Draw the circuit diagram of a dynamic logic that performs $\boldsymbol{Z = \overline{A + B(C + D)}}$.

(b) Determine the width of NMOS transistors, such that the worst case t_{pHL} delay becomes roughly equivalent to a referenced inverter with W_n=1um and W_p=2um.