Laboratory Goals

- Introduce text-based SPICE simulations
- Test transistor circuits using SPICE netlists
- Simulate output response for transistor-based circuits

Pre-lab reading

- Read the pre-lab introduction below
- Visit the Cadence website (maker of PSPICE)

Equipment needed

- Lab notebook, pen
- Workstation PC, with PSPICE application

Parts needed

- No electronic parts are needed for this lab

Lab safety concerns

- There are no specific safety concerns for this lab

1. Pre-Lab Introduction

Some Important Facts and Rules about SPICE Netlist Scripting

- Spice is not case sensitive, so names as *Vbias*, *VBIAS*, *vBias* orv *vBiaS* are equivalent.
- All element names must be unique, so you can't have two resistors named Rbias.
- The first line in the netlist file is used as a title. It is printed at the top of each output page. You should use this line to store your name, the assignment, the class and any other information appropriate for a title page. Spice will ignore this line as circuit data. Do not place any actual circuit information in the first line.
- There must be a reference node "0" against which all voltages are calculated.
- Each node must have at least two elements attached to it.
- Spice accepts ordinary text for node designations. If you want to declare a node as "nodeA", you can. The only restriction is that you can't embed spaces in a node name. Use the underscore ("_") character to simulate spaces.
- The last line in any data file must be ".END" (with a period before the word)
- All lines that are not blank (except for the title line) must have a character in column 1, the leftmost position on the line.
- Use "*" (an asterisk) in column 1 in order to create a comment line.

- Use "+" (plus sign) in column 1 in order to continue the previous line (for better readability of very long lines).
- Use "." (period) in column 1 followed by the rest of the "dot command" to pass special instructions to the program like .probe or .lib
- Use the designated letter for a part in column 1 followed by the rest of the name for that part with no spaces in the part name.
- Use "whitespace" (spaces or tabs) to separate data fields on a line.
- Use ";" (semicolon) to terminate data on a line if you wish to add commentary
- information on that same line.

Large and Small Numbers in SPICE

Spice is used mostly by engineers and scientists. Accordingly, it was created with the ability to recognize the typical metric units for numbers. Unfortunately, Spice cannot recognize Greek fonts or even upper vs. lower case. Thus, our usual understanding and use of the standard metric prefixes must be modified. For example, in everyday usage, "M" indicates "mega" (10^6) and "m" stands for milli (10^{-3}). Clearly, this would be ambiguous in Spice, since it is not case sensitive. Thus, in Spice, a factor of 10^6 is indicated by "MEG" or "meg." "M" or "m" is reserved for 10^{-3}. Another quirk of Spice is the designation for 10^{-6} with “u”.

Number Prefix *Common Name*

- 10^{12} - "T" or "t" *tera*
- 10^{9} - "G" or "g" *giga*
- 10^{6} - "MEG" or "meg" *mega*
- 10^{3} - "K" or "k" *kilo*
- 10^{-3} - "M" or "m" *milli*
- 10^{-6} - "U" or "u" *micro*
- 10^{-9} - "N" or "n" *nano*
- 10^{-12} - "P" or "p" *pico*
- 10^{-15} - "F" or "f" *femto*

An alternative to this type of notation, which is in fact, the default for Spice output data, is "textual scientific notation." This notation is written by typing an "E" followed by a signed or unsigned integer indicating the power of ten. Some examples of this notation are:

656,000 = 6.56E5
-0.0000135 = -1.35E-5
8,460,000 = 8.46E6

2. Pre-Lab Circuit Analysis

- Calculate all node voltages by hand for the circuits shown in figures 1 and 2.
- Also find I_D, V_{GS} and V_{DS} using:
  $K'_n = 500\ \mu A/V^2$, W/L = 1, and $V_T = 1V$ for the NMOS transistor and
  $K'_p = 250\ \mu A/V^2$, and W/L = 1, $V_T = -1V$ for the PMOS transistor

3. MOSFET Circuits at DC

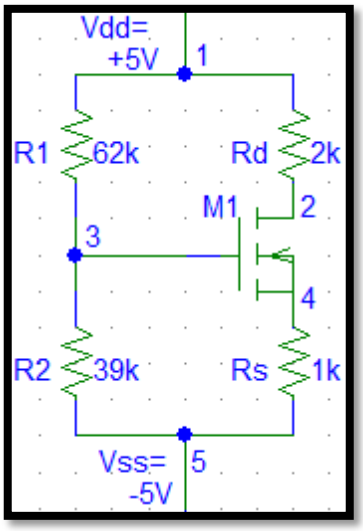

Figure 1. NMOS Circuit

- Create a folder in **My Documents** for your PSPICE designs to be stored.
- Open the PSPICE application called Pspice **AD**.
- Create a new File by selecting "File New Text File" or by clicking the icon.
- Rather than graphically drawing a circuit, you will now write the circuit's netlist.
- SPICE requires the first line be a text title by which you can identify the circuit.
- Commenting may be added in your netlist by using "*" to indicate the comment line.
- Type the following line to add the part library:
  .lib "nom.lib"
  This command directs the software to load the standard PSICE libraries
- Next, create your voltage source by entering these lines:
  Vdd 1 0 DC 5V
  Vss 5 0 DC -5V
- SPICE identifies each node in a circuit with a name or number, with ground usually being node number 0.
- Enter the drain resistor Rd by typing Rd 1 2 2k. This line instructs the software to connect a 2kΩ resistor between nodes one and two. Resistor labels do not have to consist entirely of numbers and can directly be entered as labeled Rd and Rs.
- Likewise, for the remaining resistors enter the following code lines:
  R1 1 3 62k
  R2 3 5 39k
  Rs 4 5 1k
- Just as R identifies and element as a resistor, other circuit elements must also be identified. A transistor can be labeled by M. The given transistor is coded as:
  M1 2 3 4 4 ntype L=1.0u W=1.0u
  .model ntype nmos level=2 Vto=1 Kp=5e-4

- More than one transistor may be included in a circuit just as more than one resistor, and multiple transistors are numbered accordingly M1, M2, etc. A transistor is a three terminal device and its connecting nodes are identified as the drain, gate, source, and body. By convention the source and body are shorted together.
- The .model line specifies that the ntype label identifies an NMOS. The level corresponds to various transistor circuit parameters, and the rest of the line identifies the turn on threshold voltage and the process transconductance parameter k' value.
- Enter .op in the next line. This indicates to perform a dc analysis of the circuit
- Finally add .end in the last line, to tell SPICE that the file is finished.
- In order to run the simulation, you must change the file type to a circuit file (.cir). To do this simply click on Save As and input .cir after the filename.
- To run the analysis, click on the simulation queue button on the left side of the screen. If the simulation queue button is greyed out, this means that the PSPICE Software is still displaying the file as a text file instead of a .cir file. To solve this issue, close the file and reopen it with the proper .cir extension.
- In the new simulation queue window, click on the run simulation button.
- After running the simulation, the software will report any errors in your netlist.
- The results of the analysis can be seen by selecting the "View Output File" button or by selecting Output File from the View drop down menu.
- The Output File will display the netlist code, as well as the node voltages.
- Currents, including the bias current Id, can be calculated with Ohm's law using the generated node voltages. Additionally, the desired Vgs and Vds values can also be obtained by subtracting appropriate nodes.
- Compare the simulation results to your hand computed analysis from the pre-lab.
- Repeat all the steps in this section for the following PMOS circuit (W/L=1, V_{TP}=-1V).
  Use the model line: .model ptype pmos level=2 Vto=-1 Kp=2.5e-4

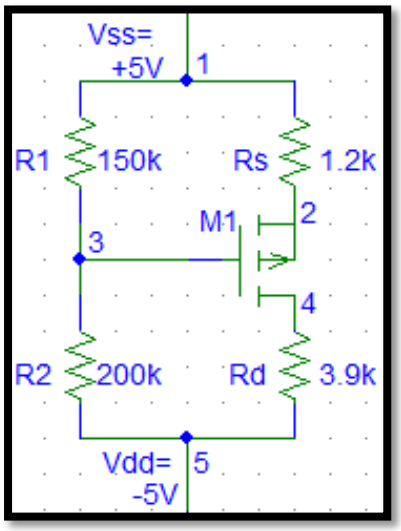

Figure 2. PMOS Circuit

4. CMOS Logic Gates

Basic Inverter

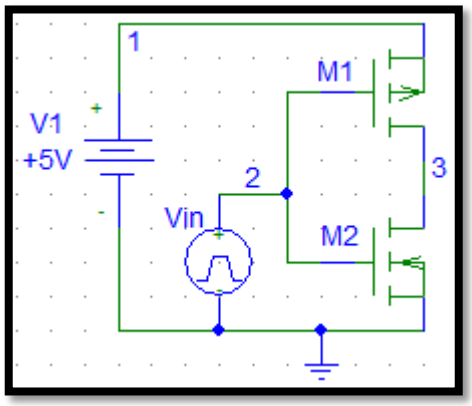

Figure 3. Inverter Logic Gate Circuit

- A CMOS Inverter logic gate circuit combines one NMOS and one PMOS to perform a Not logic function. SPICE modeling may be used to verify the circuit function as opposed to analyzing the circuit by hand.
- Open a new page to write the Netlist in. Save the file as a .cir filetype.
- For circuit three shown above, the transistor parameters are K'n= K'p = 50 μA/V^2, and L=2u, W=8u, V_{TN} = 0.6V and V_{TP} = -0.6V.
- The nodes are labeled as shown with the ground of the circuit being node zero.
- Enter a first text line identifying the circuit as an Inverter
- The circuit voltage V1 may be identified in the circuit as follows: V1 1 0 DC 5V
- In addition to the input voltage pulse must be generated. This can be done with:

  Vin 2 0 pulse(0V 5V 0us 1us 1us 40us 80us)

  The first two pulse parameters are the low and high voltages respectively. The following number specifies the start time delay, the next two numbers identify the rise and fall times of the transistors respectively. The final two numbers are the pulse width and period respectively.
- Both transistors must be identified with their connecting nodes labeled:

  M1 3 2 1 1 cmosp L=2u W=8u

  M2 3 2 0 0 cmosn L=2u W=8u
- Two .models are required to describe both the NMOS and PMOS transistors:

  .model cmosp pmos level=2 Vto=-0.6 Kp=50u

  .model cmosn nmos level=2 Vto=0.6 Kp=50u
- An output capacitance is also required to accurately model the gate. This capacitor is included in SPICE with C1 3 0 100f

  This line specifies a capacitor between nodes 3 and 0 with a capacitance of 100fF
- Perform a transient analysis with a step size of 1us and a final time of 80us by using:

  .probe

  .tran 1us 80us
- Add the .end line, save the netlist, and run the simulation.

- A blank screen graph plot will pop up on the screen. To graph your plots, you must press the add trace button on the menu. A new window will appear for you to select the parameters you wish to plot. Select the input voltage V(2) and output voltage V(3).
- Your circuit inputs and outputs should look something like a square wave. To print this graph, you can simply use print, or if you like you may use the Microsoft paint program to capture a screenshot by pressing print screen, then cut and paste it into your report.

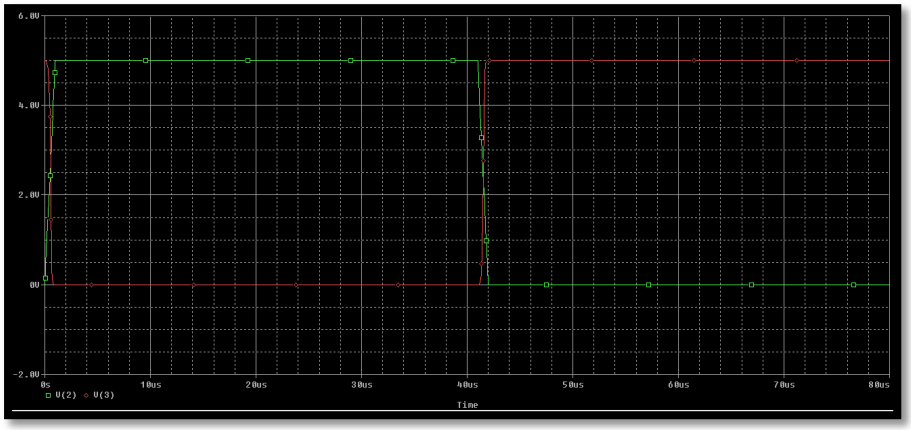

Figure 4. Example Output of Inverter Simulation

- Print the circuit code as well as simulation results to be included with your lab report
- In order to print the plots, they first must be saved by choosing the save plots option from the file drop down menu. The saved plots may then be opened and printed, or screenshots may also be taken and saved in a Word document.

2-Input NAND Logic Gate

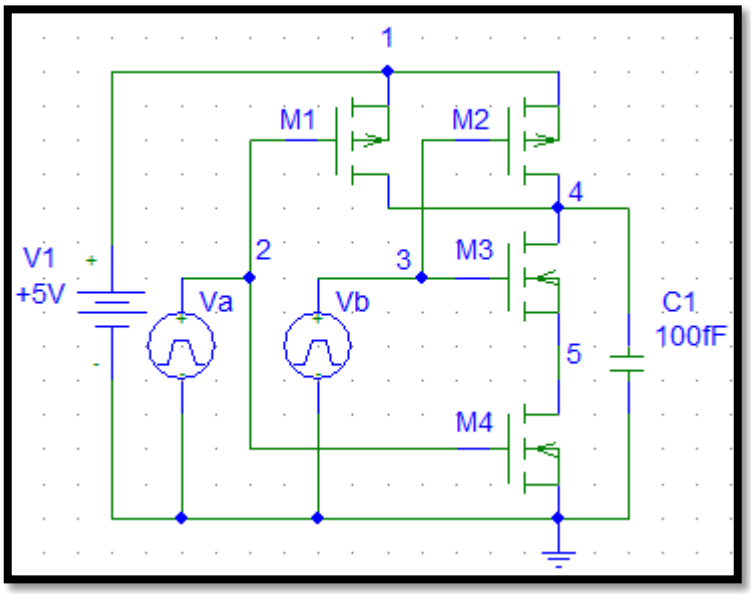

Figure 5. 2-Input NAND Logic Gate Circuit

- A two input NAND circuit combines four transistors to perform the logic function. Use SPICE modeling to verify the circuit function. Use the same transistor parameters and models used for the inverter. And the following input pulses:
  Va 2 0 pulse(0V 5V 0us 1us 1us 20us 40us)
  Vb 3 0 pulse(0V 5V 0us 1us 1us 40us 80us)
- Perform a transient analysis simulation with a step size of 1us and a final time of 80us.
- Plot the two input V(2), V(3) and the output voltage V(4).

2-Input NOR Logic Gate

Provide a simulation for the following 2 Input NOR Gate and plot the inputs and output.

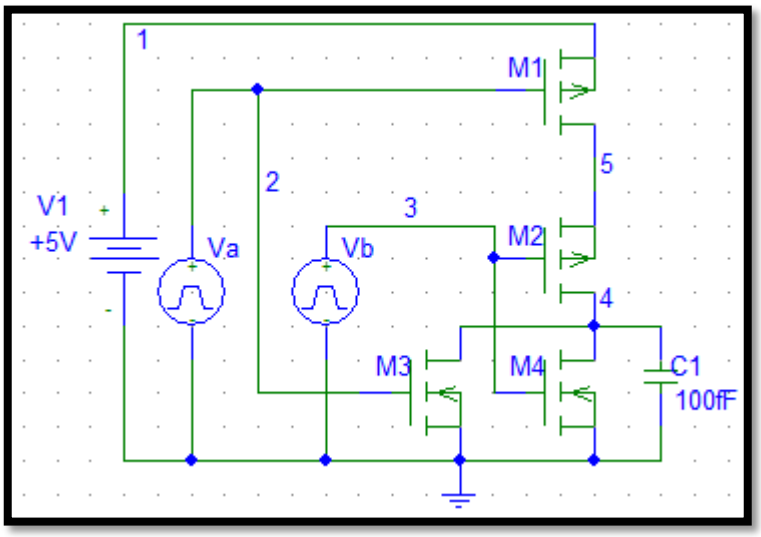

Figure 6. 2-Input NOR Logic Gate Circuit

2-Input AND Logic Gate

Provide a simulation for the following 2 Input AND Gate and plot the inputs and output.

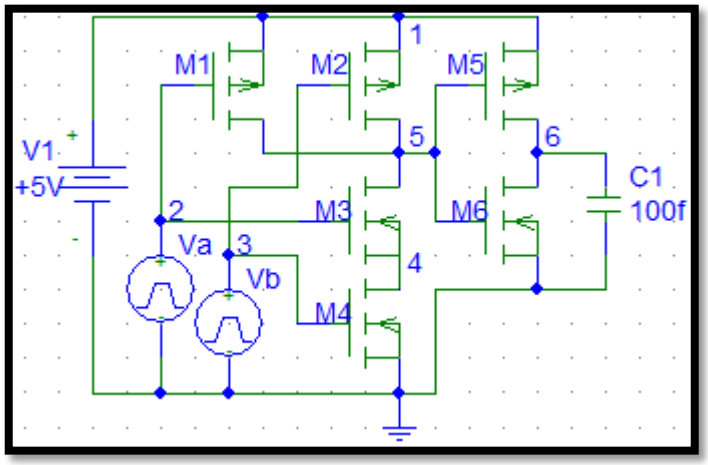

Figure 7. 2-Input AND Logic Gate Circuit

2-Input OR Logic Gate

Provide a simulation for the following 2 Input OR Gate and plot the inputs and output.

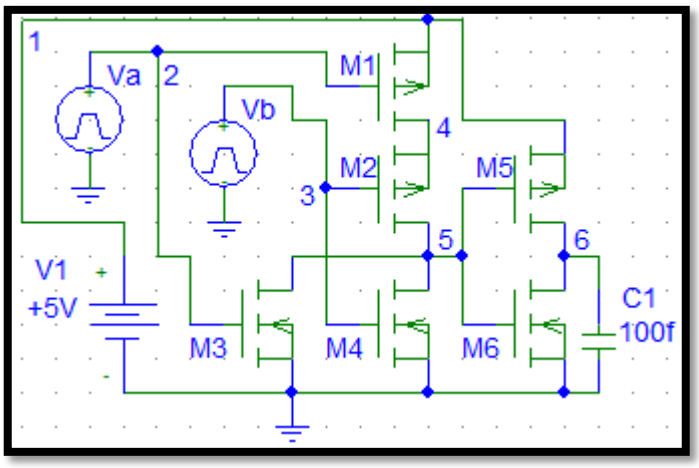

Figure 8. 2-Input OR Logic Gate Circuit

3-Input NAND Logic Gate

Provide a simulation for the following 3 Input NAND Gate and plot the inputs and output.

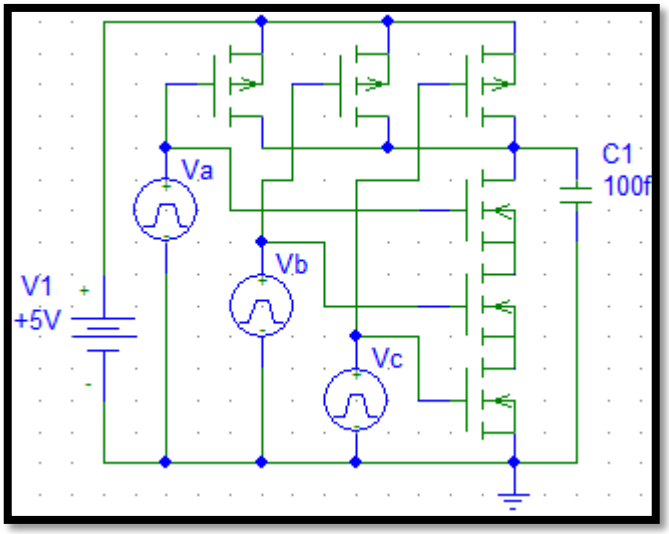

Figure 9. 3-Input NAND Logic Gate Circuit

Use SPICE modeling to verify the circuit function. Use the same transistor parameters and models used for the inverter. And the following input pulses:

Va 2 0 pulse(0V 5V 0us 1us 1us 10us 20us)
Vb 3 0 pulse(0V 5V 0us 1us 1us 20us 40us)
Vc 4 0 pulse(0V 5V 0us 1us 1us 40us 80us)

3-Input NOR Logic Gate

Provide a simulation for the following 3 Input NOR Gate and plot the inputs and output.

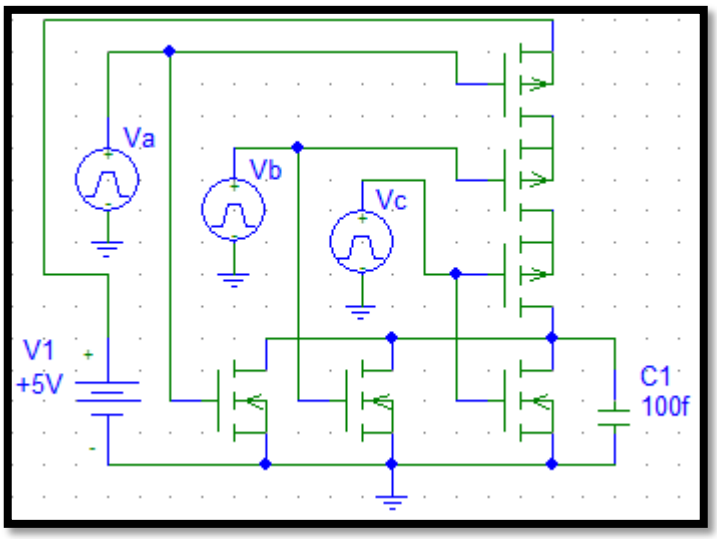

Figure 10. 3-Input NOR Logic Gate Circuit

Use the same transistor parameters and models used for the inverter.

3-Input AND Logic Gate

Provide a simulation for the following 3 Input AND Gate and plot the inputs and output.

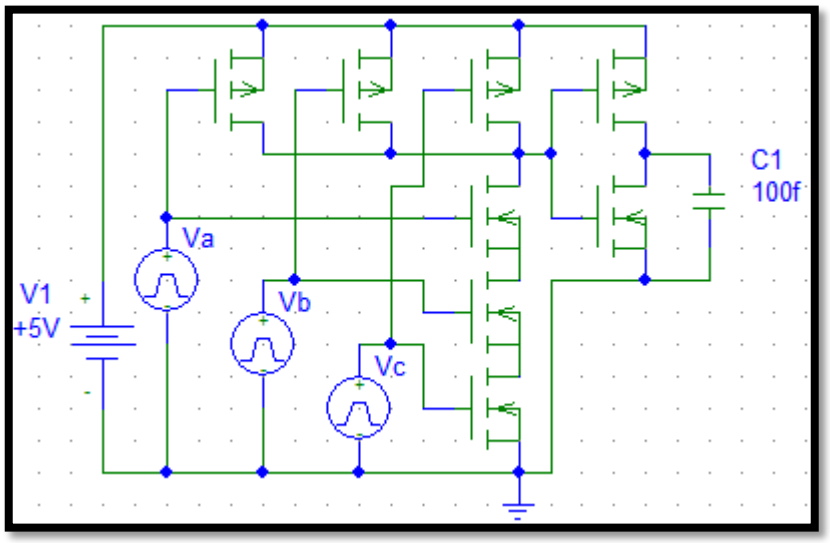

Figure 11. 3-Input AND Logic Gate Circuit

Use the same transistor parameters and models used for the inverter.

3-Input OR Logic Gate

Provide a simulation for the following 3 Input OR Gate and plot the inputs and output.

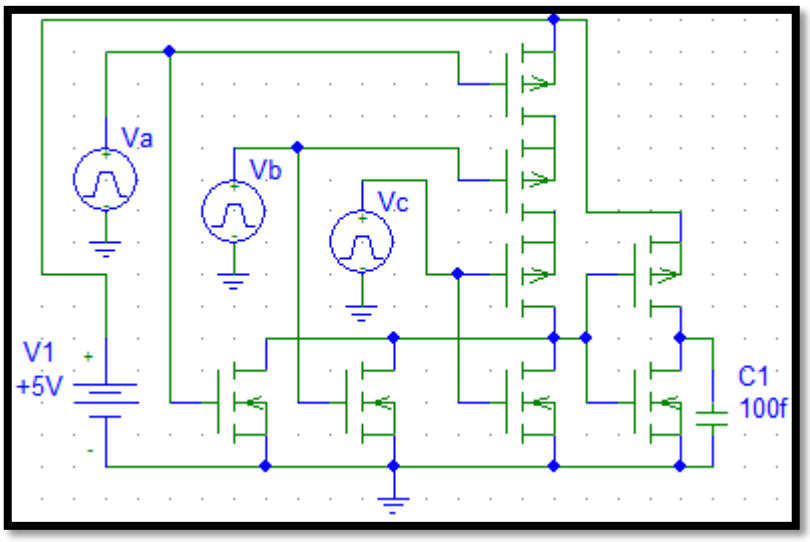

Figure 12. 3-Input OR Logic Gate Circuit

Use the same transistor parameters and models used for the inverter.

10. Analysis

Write a brief summary report for this lab. Be sure to also include the following topics:

Compare the results from your pre-lab computations to the PSPICE models you created. Record your findings in your lab notebook

Include print outs of the code, circuit diagrams with nodes labeled and simulation results.

Explain any difficulties you had with this lab. (Please include suggestions to improve the lab, if you have them).