Laboratory Goals

- Design and construct a CMOS Inverter using CMOS Transistors
- Measure propagation delay of Inverter with comparison to IC Inverter

Pre-lab reading

- Course Textbook
- *Analysis and Design of Digital Integrated Circuits* published by McGraw-Hill, Copyright 2004. (Chapter 4)
- *CMOS Electronics, How it works, How it fails* published by Wiley-Interscience, Copyright 2004.
- *P-Channel enhancement mode vertical D-MOS transistor* published by Philips Semiconductor, Copyright 1995
- *N-Channel enhancement mode Field Effect Transistor* published by Fairchild Semiconductor, Copyright 1995
- Read the pre-lab introduction below

Equipment needed

- Lab notebook, pen
- Agilent 54622 Digital Oscilloscope
- 2 oscilloscope probes (attached to the oscilloscope)
- Agilent 33120A Function Generator
- 1 BNC/EZ Hook test lead

Parts needed

- Circuit breadboard
- Lab parts kit
- Transistor, P-MOS, BS250
- Transistor, N-MOS, BS170 or 2N7000
- Jumper wires
- 7404 Inverter Chip

Lab safety concerns

- Make sure all circuit connections are correct, and no shorted wires exist
- Adjust signal generator to the proper level before connecting it to the circuit
- Transistors may be extremely hot after the lab. Handle with care

1. Pre-Lab Introduction

For this lab's measurements a formal definition of the propagation delay in an inverter must be first introduced. As shown in Figure 1, an input pulse with finite (nonzero) rise and fall times (t_r and t_f) is applied. The inverted pulse at the output exhibits finite rise and fall times (labeled t_{TLH} and t_{THL} , where the subscript T denotes transition, LH denotes low to high, and HL denotes high to low). There is also a delay time between the input and output waveforms. The usual way to specify the propagation delay is to take the average of the high-to-low propagation delay, t_{PHL} , and the low-to-high propagation delay, t_{PLH} . As indicated, these delays are measured between the 50% points of the input and output waveforms. Also note that the transition times are specified using the 10% and 90% points of the output excursion (VOH − VOL).

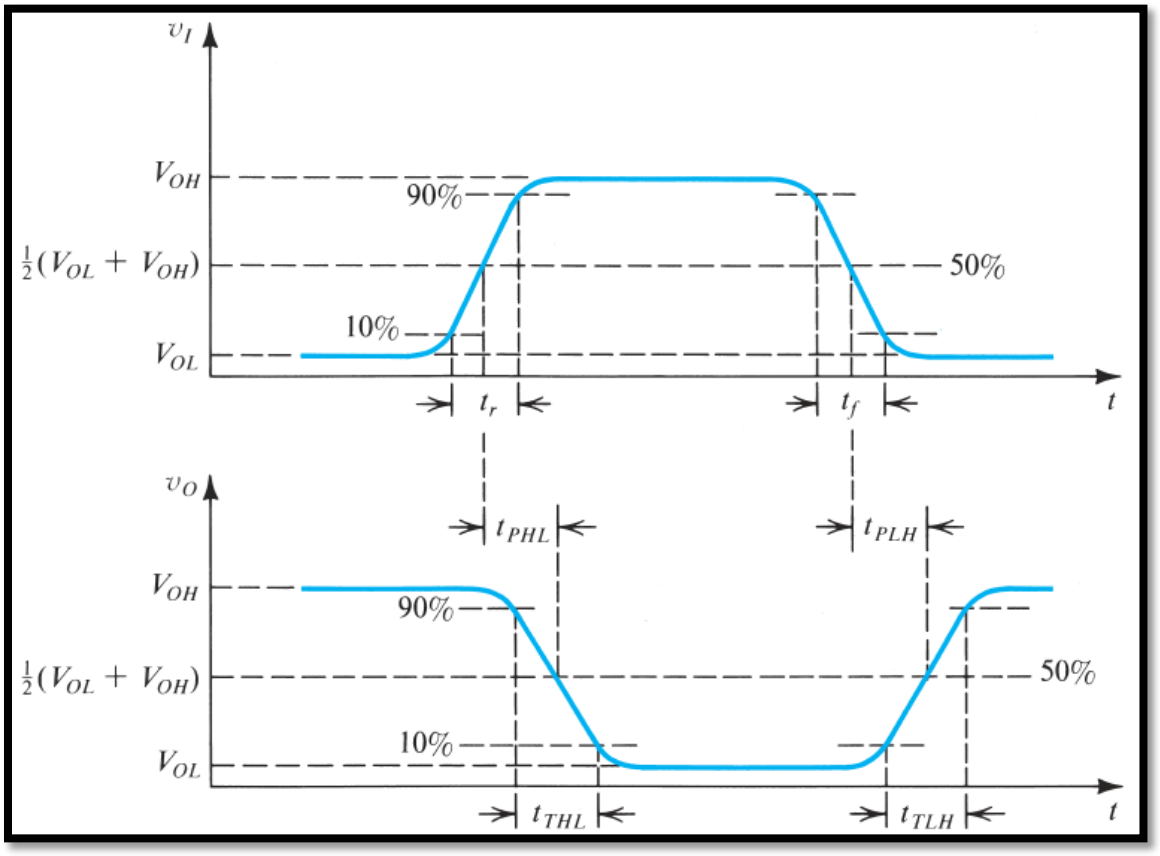

Figure 1. Definitions of propagation delays and transition times of the logic inverter.

2. Pre-Lab Inverter Design

- Draw a schematic within PSPICE of an Inverter for layout purposes (Labeling the gate, source, and drain nodes)
- Create the truth table for an Inverter

3. Circuit Construction and Signal Measurement

- For this lab and the following ones, we will use input pulse signals with finite (nonzero) rise and fall times (t_r and t_f). Hence, we will design the pulse with the Waveform Editor and apply it using the Arbitrary Waveform Generator.
- Design the pulse to operate between 0V and 5V with at least 1us rise and fall times.
- Build the circuit you created from your Pre-Lab and show it to your TA
- Connect the Analog Output of the ELVIS to the gate input of the Inverter.
- Clip the **CH1** oscilloscope probe and ground clip to the circuit input and ground respectively
- Clip the **CH2** oscilloscope probe and ground clip to the circuit output (V_{out}) and ground respectively
- Using the Oscilloscope's Cursors measure and record the following:
  - Input Signal Rise Time (t_r)
  - Input Signal Fall Time (t_f)
  - Output Signal High to Low Transition Time (t_{THL})
  - Output Signal Low to High Transition Time (t_{TLH})
  - High to Low Propagation Delay (t_{PHL})
  - Low to High Propagation Delay (t_{PLH})
- Taking the average of t_{PHL} and t_{PLH} calculate the propagation delay for the gate.
- Repeat Steps for IC Inverter (7404 Inverter Chip)

Before leaving the lab, take a few minutes to clean up your workstation, and return all equipment to your cabinet.

3. Analysis

Write a summary report for this lab. Be sure to also include the following topics:

What is the difference between the IC inverter propagation delay and the constructed inverter propagation delay? What reasons can you give for the difference, if any?

What applications can you think of for this circuit?

Explain any difficulties you had with this lab. (Please include suggestions to improve the lab, if you have them).