Laboratory Goals

- Design and construct CMOS NAND and AND Gates using CMOS Transistors.
- Measure propagation delay of NAND Gate with comparison to 7400
- Measure propagation delay of AND Gate with comparison to 7408
- Compare a SPICE simulation to the measured output values

Pre-lab reading

- Course Textbook
- *Analysis and Design of Digital Integrated Circuits* published by McGraw-Hill, Copyright 2004.(Chapter 4)
- *CMOS Electronics, How it works, How it fails* published by Wiley-Interscience, Copyright 2004.
- *P-Channel enhancement mode vertical D-MOS transistor* published by Philips Semiconductor, Copyright 1995
- *N-Channel enhancement mode Field Effect Transistor* published by Fairchild Semiconductor, Copyright 1995

Equipment needed

- Lab notebook, pen
- Agilent 54622 Digital Oscilloscope
- 2 oscilloscope probes (attached to the oscilloscope)
- Agilent 33120A Function Generator
- 1 BNC/EZ Hook test lead
- ELVIS workstation

Parts needed

- Circuit breadboard
- Lab parts kit
- 4 P-MOS Transistors (BS250)
- 4 N-MOS Transistors (BS170 or 2N7000)
- Jumper wires
- 7400 NAND Chip
- 7408 AND Chip

Lab safety concerns

- Make sure all circuit connections are correct, and no shorted wires exist.
- Adjust the signal generator to the proper level before connecting it to the circuit.
- Transistors may be extremely hot after lab handle with care.

1. Pre-Lab Inverter Design

- Simulate using PSPICE a 2 Input and a 3 Input NAND Gate.
- Simulate using PSPICE a 2 Input and a 3 Input AND Gate.
- Create the truth table for the All Gates.

2. Circuit Construction and Signal Measurement

- Design the pulses using the waveform editor to operate between 0V and 5V with finite (nonzero) rise and fall times. The period of the second pulse should be twice of the first.
- Build the circuit for a 2-Input NAND Gate shown below.

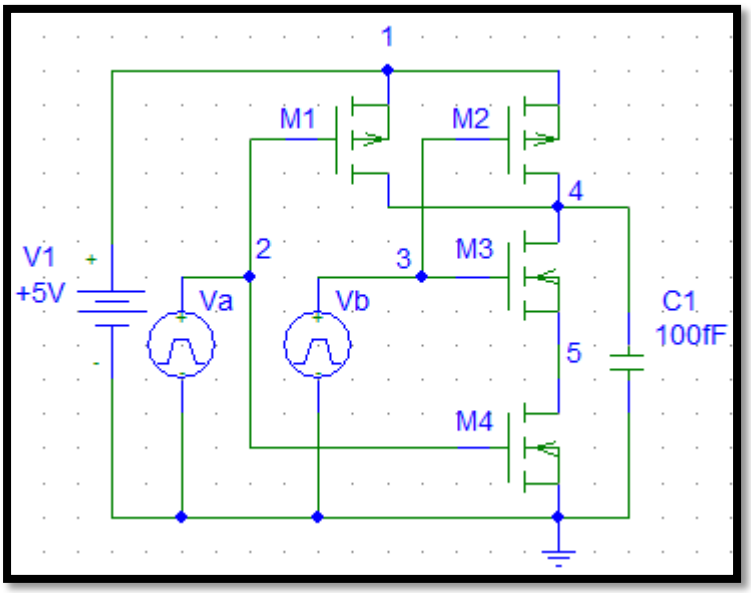

Figure 1. 2-Input NAND Logic Gate Circuit

- Connect the Analog Outputs to the inputs of the circuit.
- Using the 8-channel oscilloscope, graph the 2 inputs and the output simultaneously.
- Using the Oscilloscope's Cursors measure and record the following:
  High to Low Propagation Delay (t_{PHL}) for each transition
  Low to High Propagation Delay (t_{PLH}) for each transition
- Taking the averages of t_{PHL} and t_{PLH} calculate the propagation delay for the gate.
- Add an inverter at the output to form an AND gate and repeat the measurements.
- Repeat Steps for IC NAND (7400 NAND Chip) and for IC AND (7408 AND Chip).

Further Exploration

If time permits, build and analyze the 3-Input CMOS NAND/AND Gates shown in Figures 3 and 4. Include all measurements done with the oscilloscope in your report.

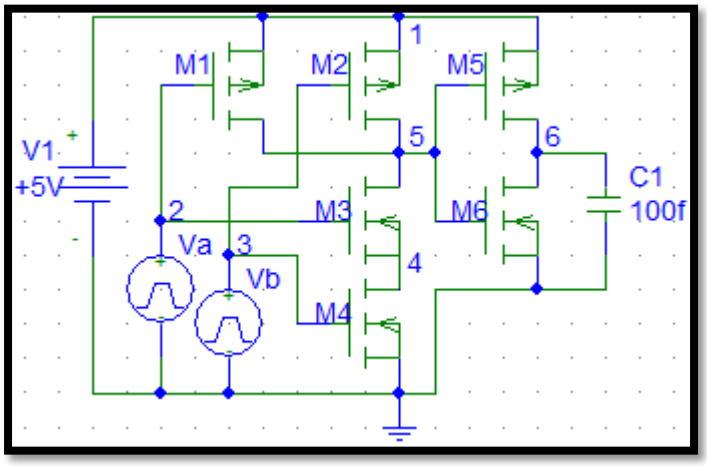

Figure 2. 2-Input AND Logic Gate Circuit

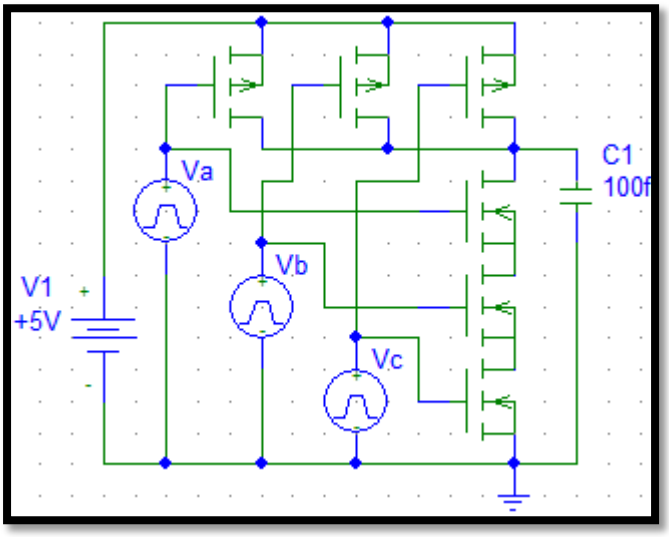

Figure 3. 3-Input NAND Logic Gate Circuit

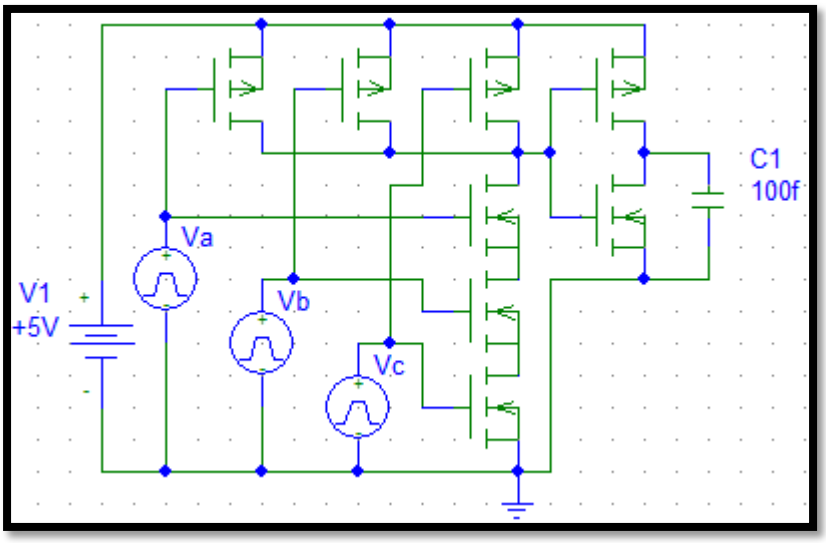

Figure 4. 3-Input AND Logic Gate Circuit

3. Analysis

Write a summary report for this lab. Be sure to also include the following topics:

What is the difference between the IC NAND/AND Gate propagation delay and the constructed NAND/AND Gate propagation delay? What reasons can you give for the difference, if any?

What applications can you think of for this circuit?

Explain any difficulties you had with this lab. (Please include suggestions to improve the lab, if you have them).