

# ECE321 – Electronics I

## Lecture 10: Basic Digital Circuits with nMOSFET

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# *Review of Last Lecture*

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- Subthreshold Conduction (leakage)**
- Velocity Saturation**
- Threshold Voltage Roll-off**
- Drain Induced Barrier Lower Effect (DIBL)**
- Hot Electron**

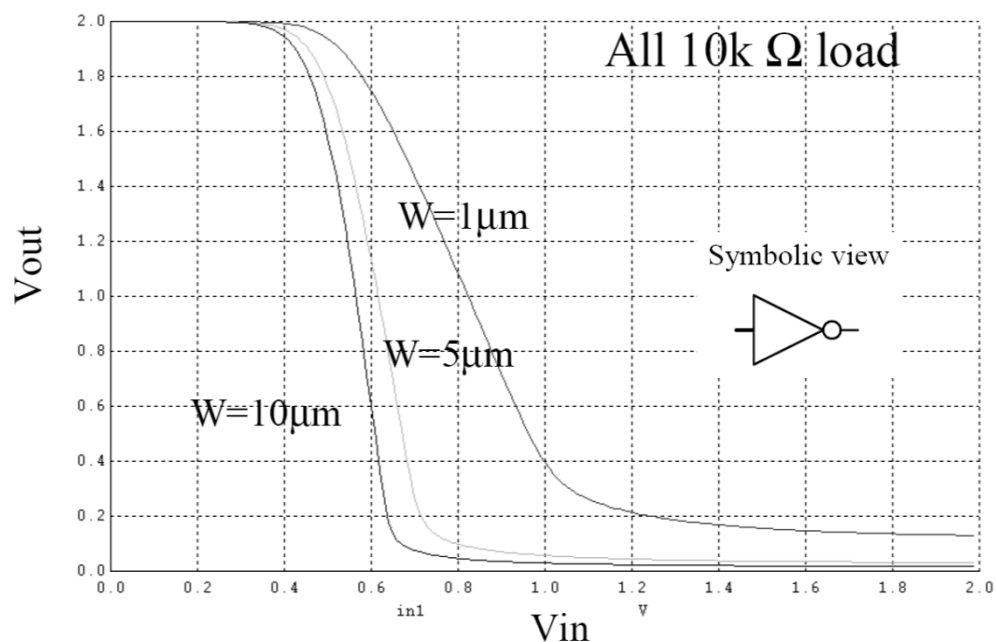
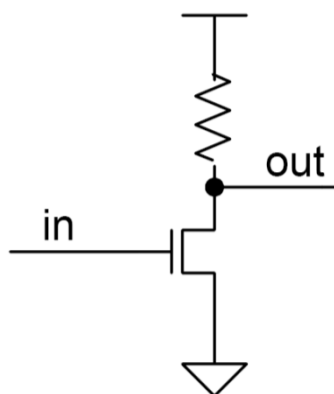
# *Today's Lecture*

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- ❑ **BASIC CMOS Inverter**
  - Resistive load inverter
- ❑ **Introduction to SPICE**

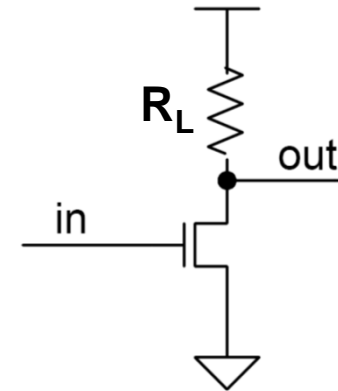
# Resistive Load Inverter

- A resistive load inverter consists of a pull down NMOS and a pull up resistor
  - Voltage Transfer Characteristic (VTC) is a function of transistor size and resistor value
  - A good inverter provide a fast transition in VTC curve



# Resistive Load Inverter Design

- ❑ The pull up resistor must be calculated to maintain a specific low level voltage ( $V_{OL}$ ) at the output
- ❑ Example:
  - $K'_n = 100 \mu\text{A}/\text{V}^2$
  - $V_{T0} = 0.7 \text{ V}$
  - $V_{OL} = 0.25 \text{ V}$
- ❑ How to compute  $R_L$  as a function of  $(W/L)$ ?
- ❑ How much is  $R_L$  for  $(W/L)=5$  ?

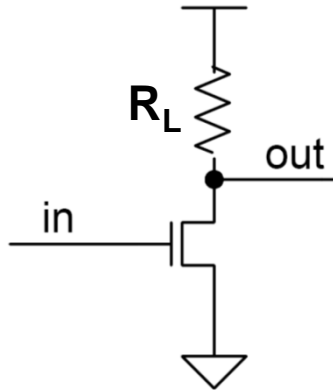


# Power in Resistive Load Inverter

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- ❑ When the output is high, there is no current drawn from  $V_{DD}$
- ❑ When the output is high, a DC current is drawn from  $V_{DD}$
- ❑ Assuming probability is 50% for logic high and logic low
- ❑ How to compute Power in the previous example?



- ❑ How much is the power for a design with 100K similar resistive load logic gate?

# Overview of TSPICE (input file)

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\* Test Circuit for VLSI Class

```
Vdd Vp gnd DC 5V
```

```
RL Vp Vout 10K
```

```
M1 Vout Vin gnd gnd CMOSN W=8um L=1.6um
```

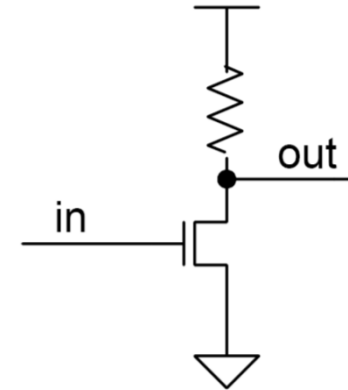
```
Vin Vin gnd DC 5V
```

```
.DC Vin 0 5 0.05
```

```
.plot Vout
```

```
.model CMOSN NMOS LEVEL=1 VTO=0.7 KP=100U GAMMA=0.1  
LAMBDA=0.01 PHI=0.3
```

```
.end
```



# Overview of TSPICE (output waveform)

