ECE321 – Electronics I

Lecture 11: CMOS Inverter: VTC & ITC

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Review of Last Lecture

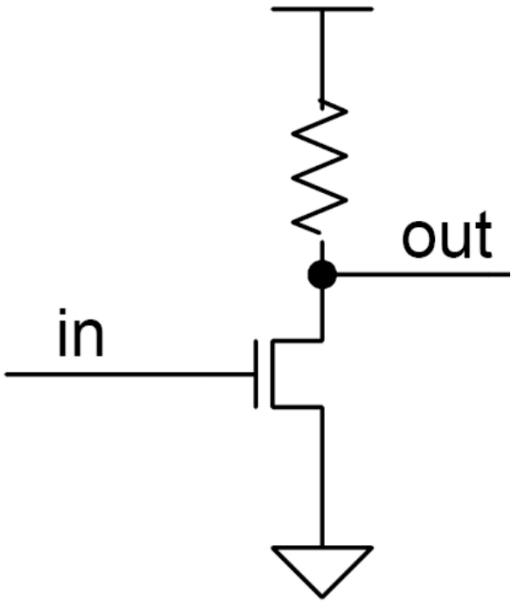
- **BASIC CMOS Inverter**
  - **Resistive load inverter**
- **Introduction to SPICE**

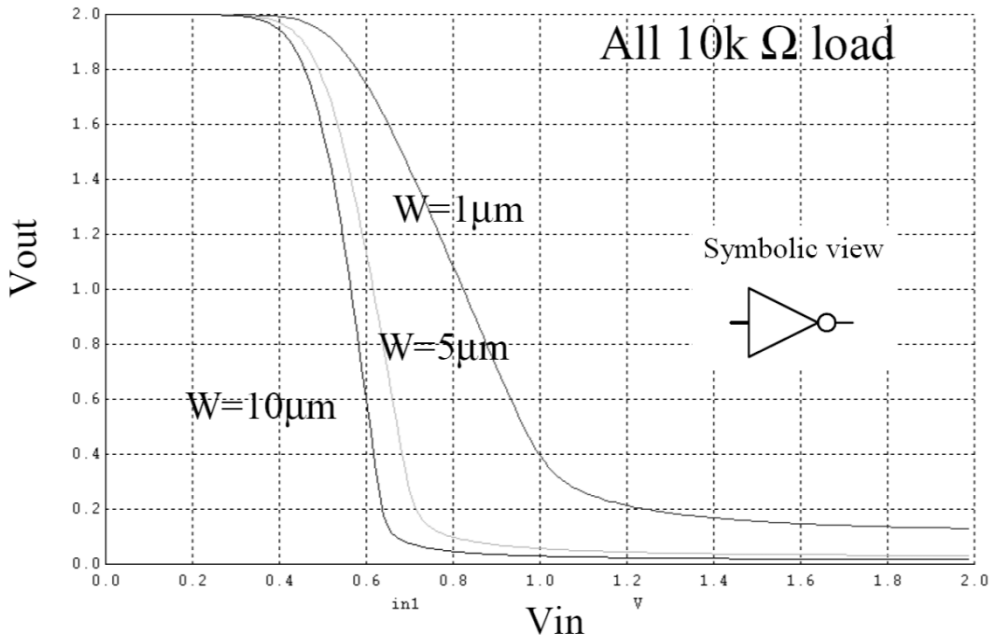
Today's Lecture

- **CMOS Inverter**
- **Voltage Transfer Characteristics (VTC)**
  - **Switching threshold voltage**
  - **Output high voltage**
  - **Output low voltage**
  - **Input high voltage**
  - **Input low voltage**
- **Current Transfer Characteristics (ITC)**
  - **Peak current**

Review: Resistive Load Inverter

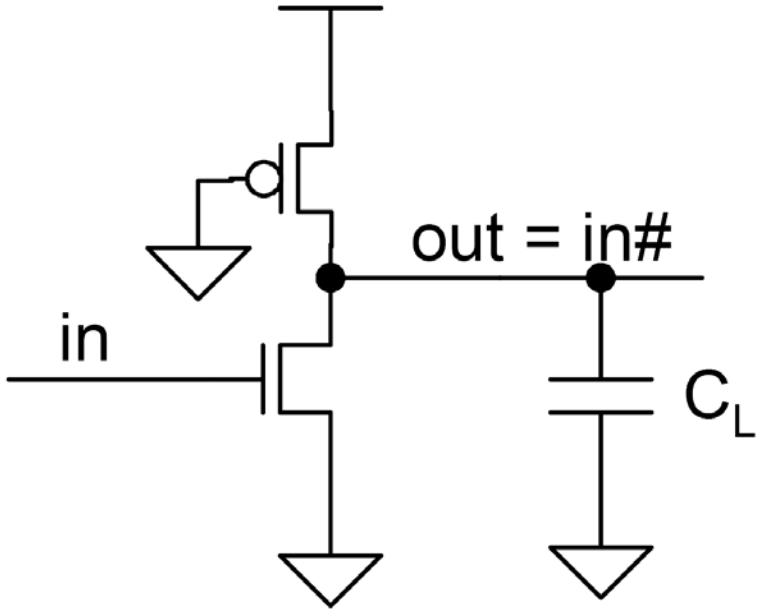
- **A resistive load inverter consists of a pull down NMOS and a pull up resistor**
  - **When the output is high, there is no current drawn from VDD**
  - **When the output is high, a DC current is drawn from VDD**





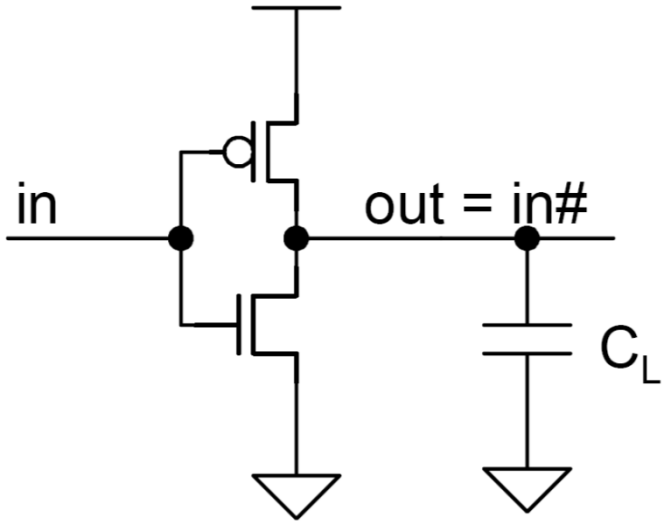
Pseudo NMOS Inverter

- Since a resistor is so big, it's better to use a single PMOS transistor that is always on:
  - PMOS pull up
  - NMOS pull down
- Why don't we use NMOS pull up?



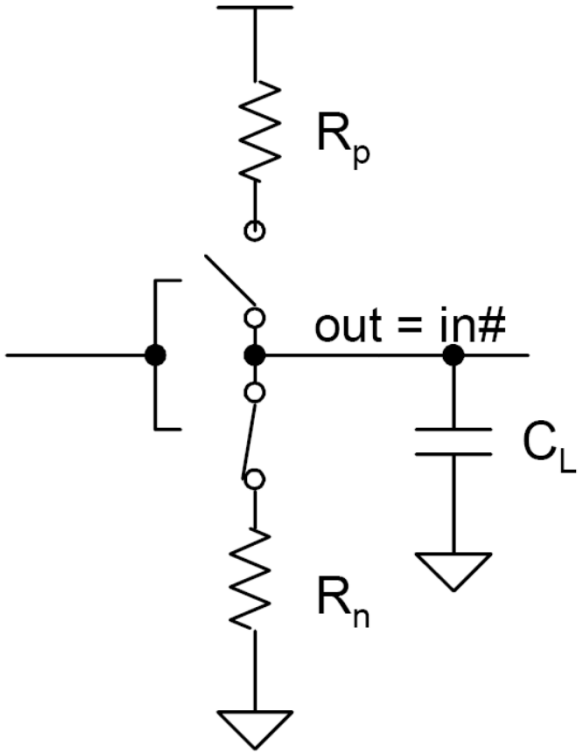
CMOS Inverter

- **CMOS inverter is comprised of**
  - PMOS pull up
  - NMOS pull down
- **Advantages**
  - No direct path from V_{DD} to GND (zero static power - except for leakage)
  - Better noise margin (Rail-to-rail output swing)
  - Ratio-less logic (output level not depend on gate size)
  - Always finite resistance to V_{DD} or GND
  - Very high input impedance

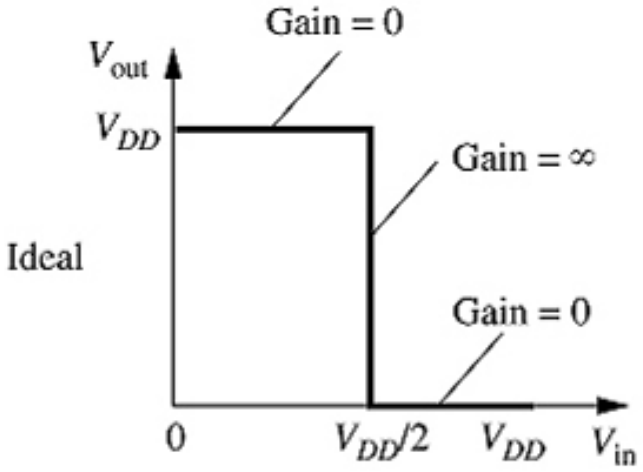


Switching model of CMOS Inverter

- Treat each transistor as either on or off
- Each transistor has an on resistance
  - This isn't a bad model as long as the input transition is quite a bit faster than the output transition and it's very intuitive
- Delay of the gate depends of the effective transistor resistant and load capacitance



Ideal Voltage Transfer Characteristic VTC



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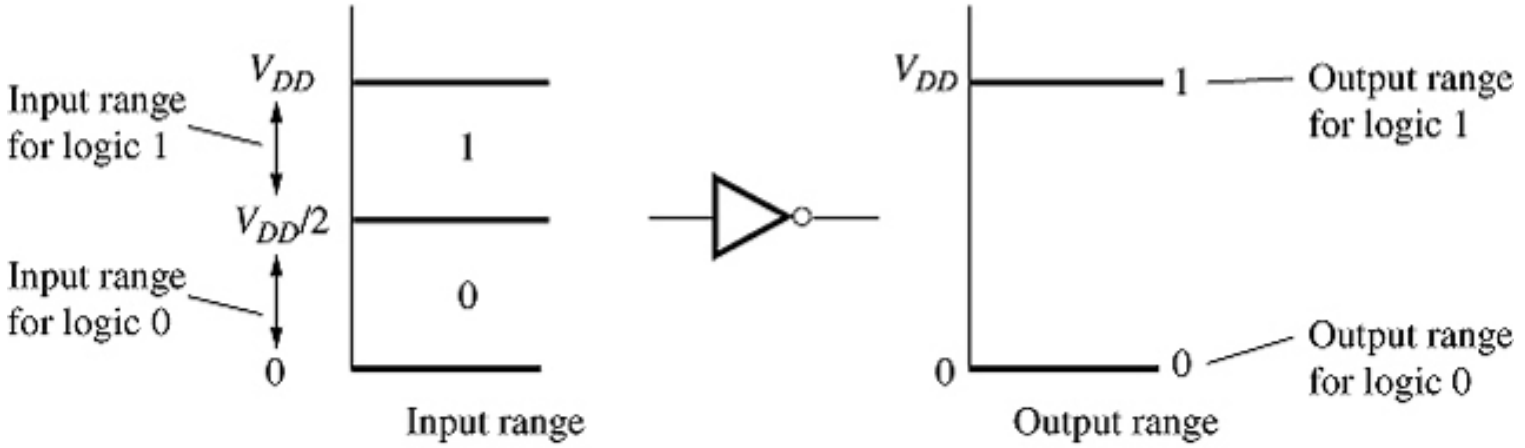

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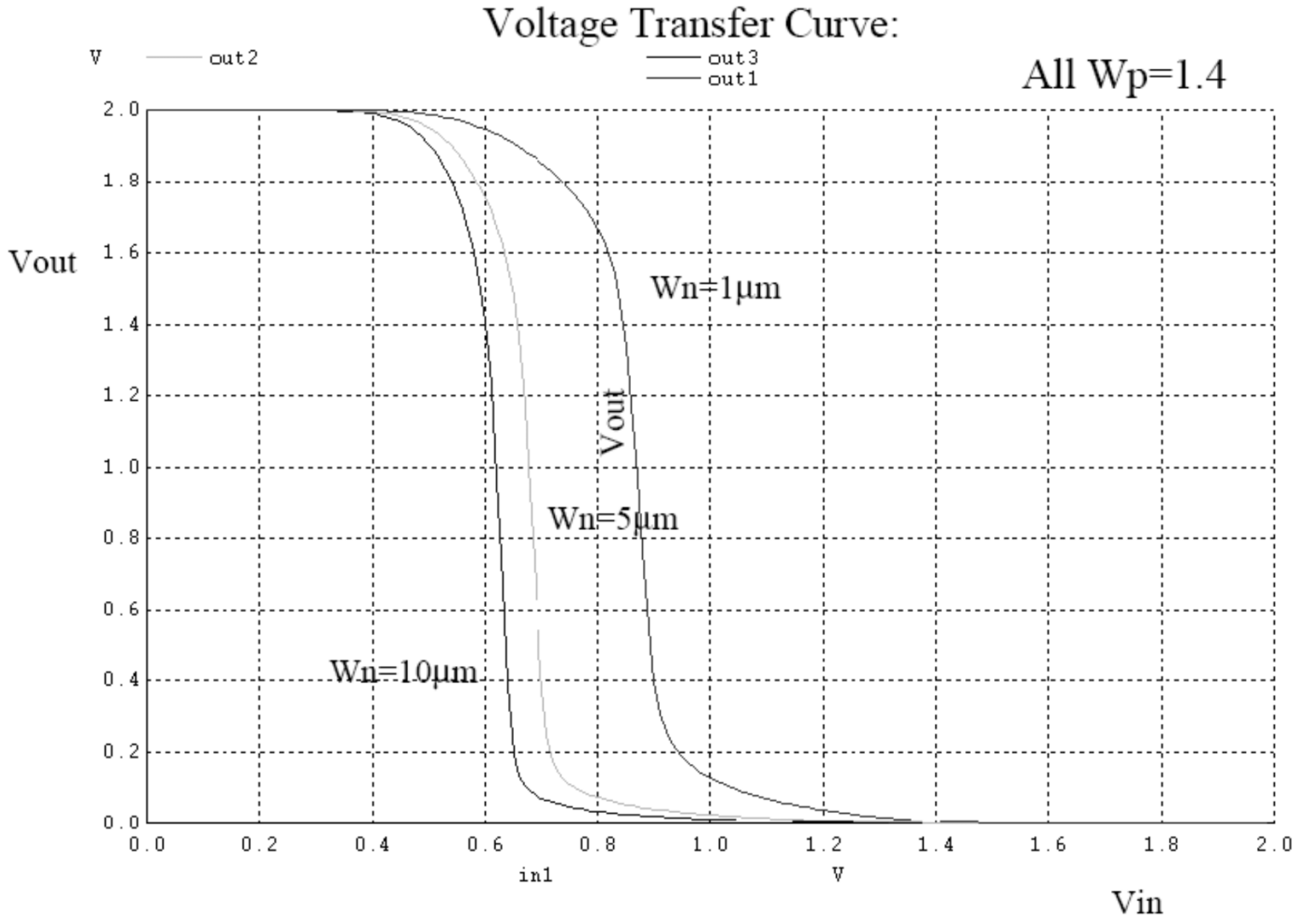
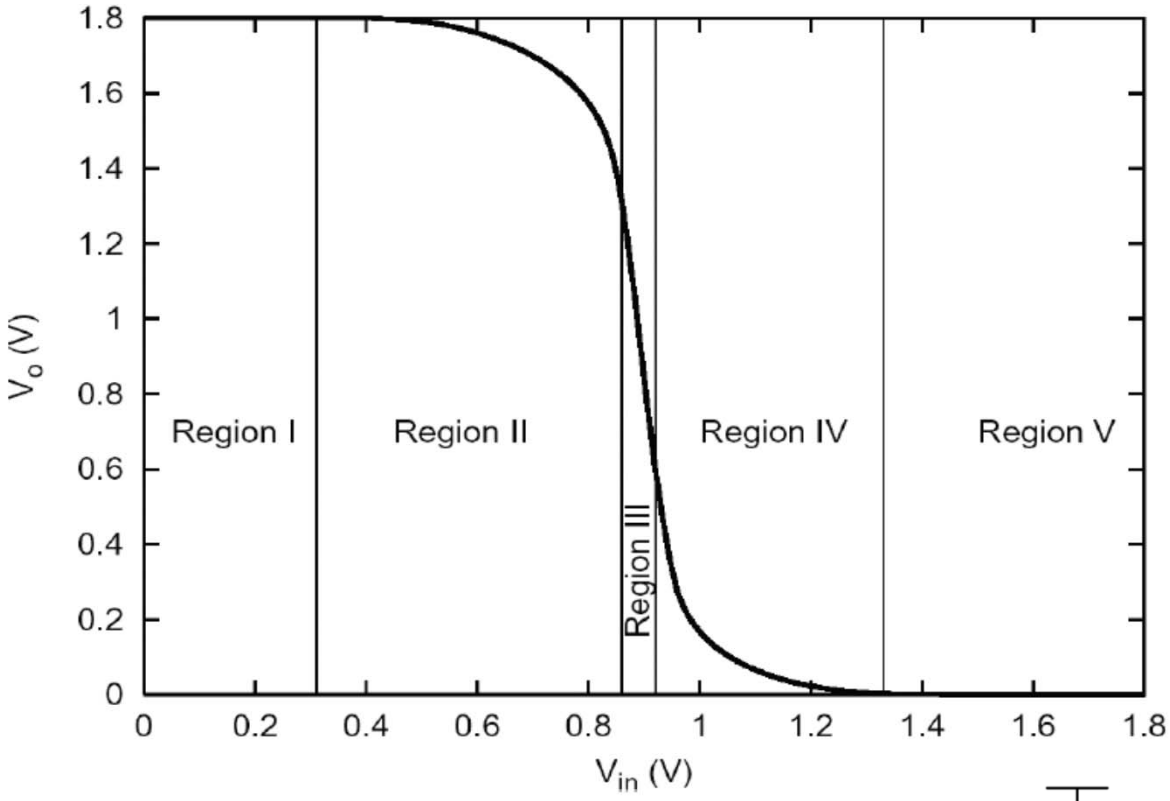
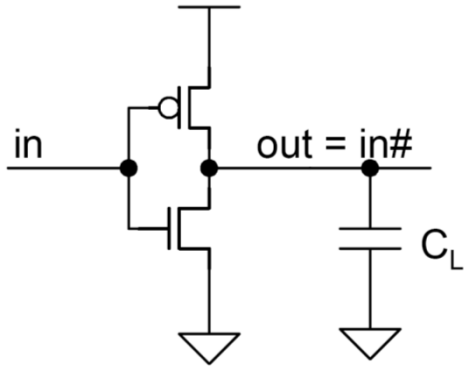
CMOS Inverter VTC



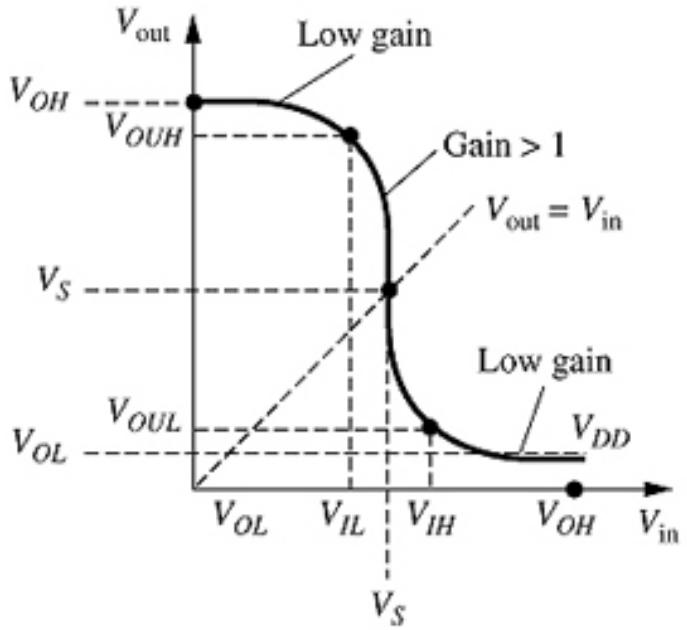
Closer Look at CMOS Inverter VTC



- **Region I – NMOS off, PMOS ohmic**
- **Region II – NMOS saturated, PMOS ohmic**
- **Region III – NMOS saturated, PMOS saturated**
- **Region IV – NMOS ohmic, PMOS saturated**
- **Region V – NMOS ohmic, PMOS off**



VTC Characterization



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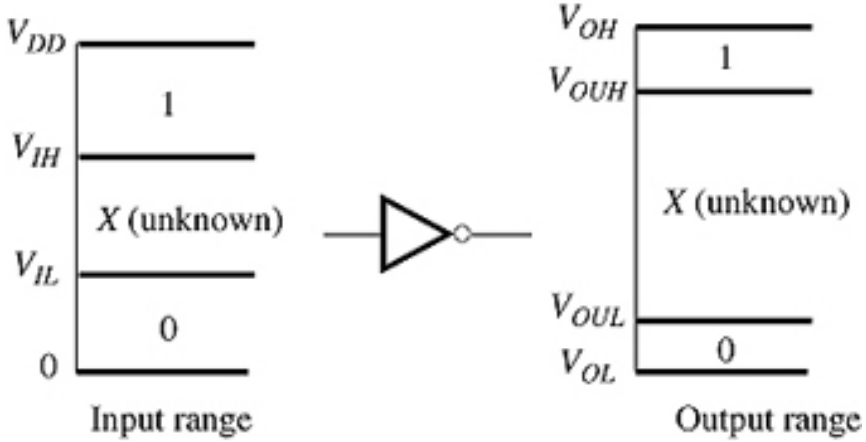


Important Parameters on VTC:

- Switching Threshold Voltage V_S or V_M
- Gain at V_S or V_M
- Output High Voltage V_{OH}
- Output Low Voltage V_{OL}
- Input High Voltage V_{IH}
- Input Low Voltage V_{IL}

CMOS Inverter Switching Threshold

- How to compute V_M in CMOS logic gate?
  - Use current equation in saturation to compute V_M
  - Assume long channel model, we will get:

$$V_M = \frac{\sqrt{\frac{K'_p (W/L)_p}{K'_n (W/L)_n}}\left(V_{DD} - |V_{Tp}|\right) + V_{Tn}}{1 + \sqrt{\frac{K'_p (W/L)_p}{K'_n (W/L)_n}}}$$

  - To set $V_M = V_{DD}/2$ for a symmetric CMOS inverter, we need to have:

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}\left[\frac{V_{DD} - 2V_{Tn}}{V_{DD} - 2|V_{Tp}|}\right]^2$$

Example: Switching Threshold Voltage

Compute the ratio of *n*MOS and *p*MOS transistor width to obtain a symmetric inverter for a 0.18 μm technology in which $\mu_n = 360\ \text{cm}^2/\text{V}\bullet\text{s}$, $\mu_p = 109\ \text{cm}^2/\text{V}\bullet\text{s}$, $V_{tn} = 0.35$ V, $V_{tp} = -0.4$ V, and $V_{DD} = 1.8$ V.

Solution:

$$\frac{W_p}{W_n} = \frac{360\ cm^2/V}{109\ cm^2/V}\left[\frac{1-\frac{2(0.35)}{1.8}}{1-\frac{2|-0.4|}{1.8}}\right]^2 = 4.0$$

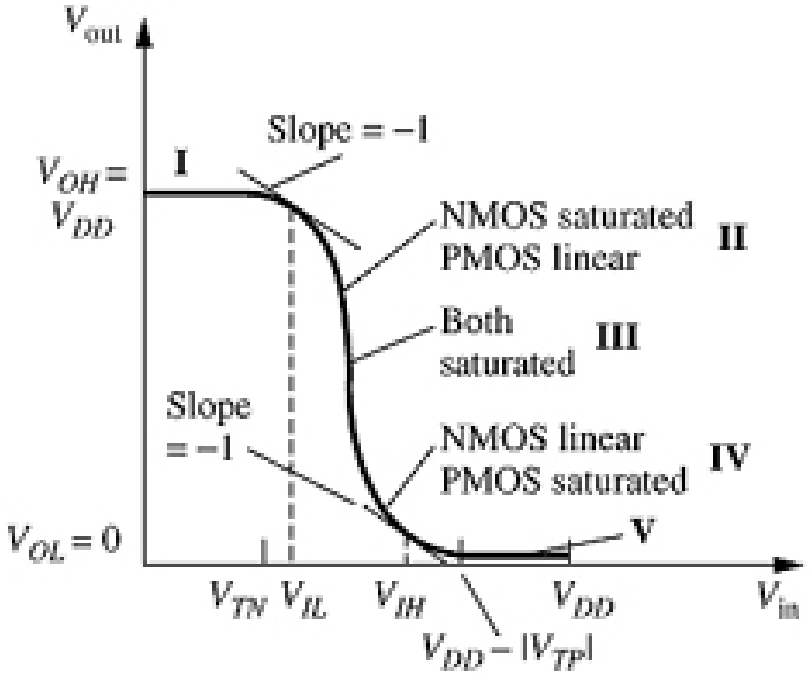
CMOS Inverter V_{OH} and V_{OL}

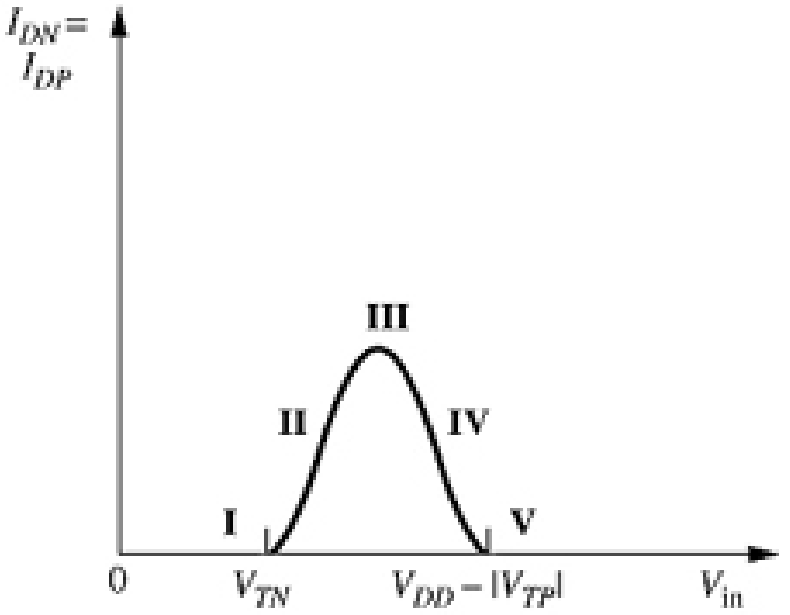
- **How to compute gain at V_{OH} and V_{OL} in CMOS logic gate?**
  - **In an ideal CMOS inverter V_{OH} is V_{DD} and V_{OL} is zero.**
  - **In a resistive NMOS inverter or any non-CMOS inverter V_{OH} and V_{OL} needs to be computed.**
  - **V_{OH} is the output of inverter when the input is zero.**
  - **V_{OL} is the output of the inverter when the input is V_{DD}.**

CMOS Inverter V_{IH} and V_{IL}

- **How to compute gain at V_{IH} and V_{IL} in CMOS logic gate?**
  - **V_{IL} is the input voltage when the slope of VTC becomes -1 at the lower input voltage.**
  - **V_{IH} is the input voltage when the slope of VTC becomes -1 at the higher input voltage.**
  - **Usually it is not easy to find V_{IH} is V_{IL} in CMOS inverter.**
  - **However, there is an approximation technique to find V_{IH} is V_{IL} that we will discuss in the next lecture.**

Current Transfer Characteristics





CMOS Inverter Peak Current

- How to compute peak current in CMOS logic gate?
  - Use current equation in saturation and use V_M
  - Assume long channel model, we will get:

$$I_{DD} = \frac{K'_n}{2}\left(\frac{W}{L}\right)_n (V_M - V_{Tn})^2 = \frac{K'_p}{2}\left(\frac{W}{L}\right)_p \left(V_{DD} - V_M - |V_{Tp}|\right)^2$$