ECE321 – Electronics I

Lecture 12: CMOS Inverter: Noise Margin & Delay Model

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Tuesday 2:00-3:00PM or by appointment
E-mail: pzarkesh.unm.edu

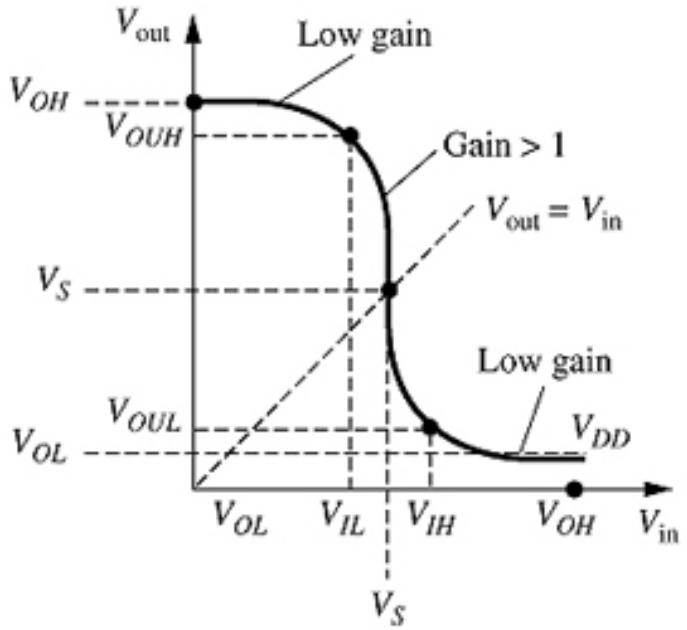
Review of Last Lecture

- **CMOS Inverter**
- **Voltage Transfer Characteristics (VTC)**
  - **Switching threshold voltage**
  - **Output high voltage**
  - **Output low voltage**
  - **Input high voltage**
  - **Input low voltage**
- **Current Transfer Characteristics (ITC)**
  - **Peak current**

Today's Lecture

- Noise Margin Definition
- Approximation of Noise Margin for CMOS Inverter
- Propagation Delay
- Rise and Fall Times
- Input and Self Loading (Load) Capacitances
- Delay Approximation

Review: Voltage Transfer Characteristics



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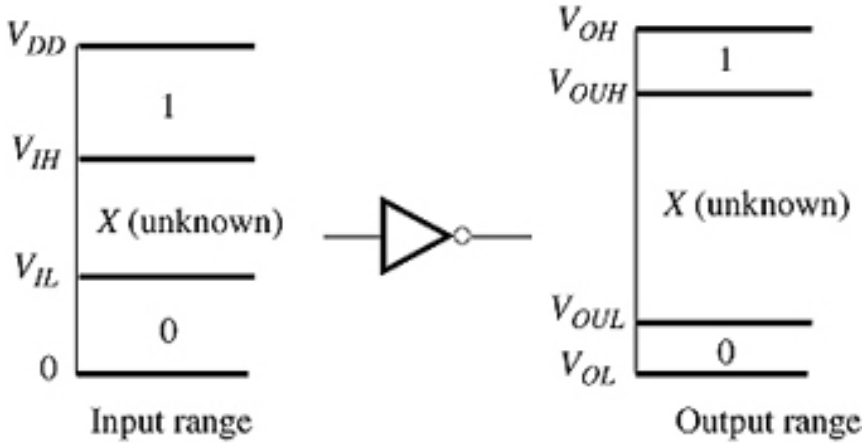
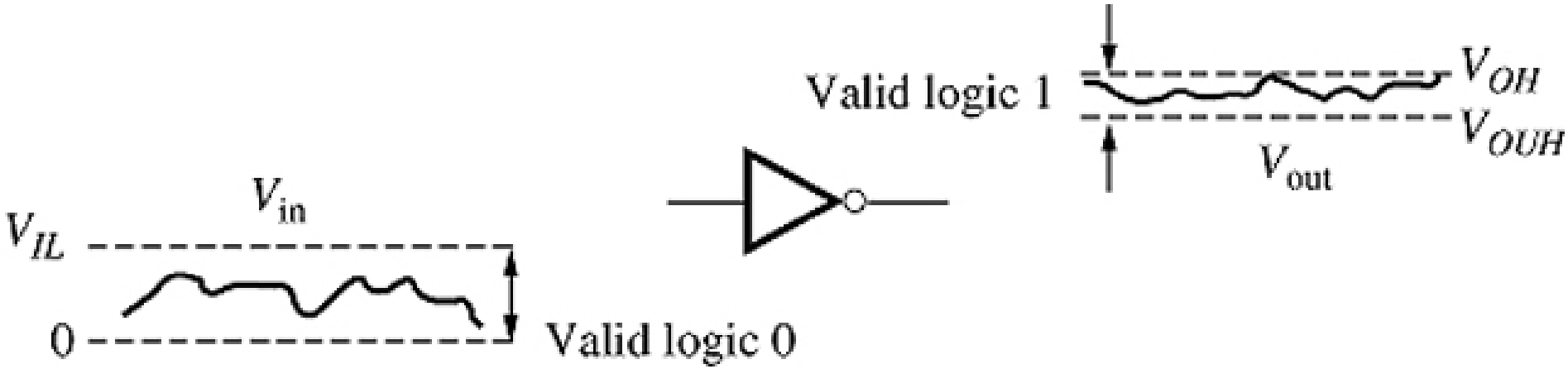


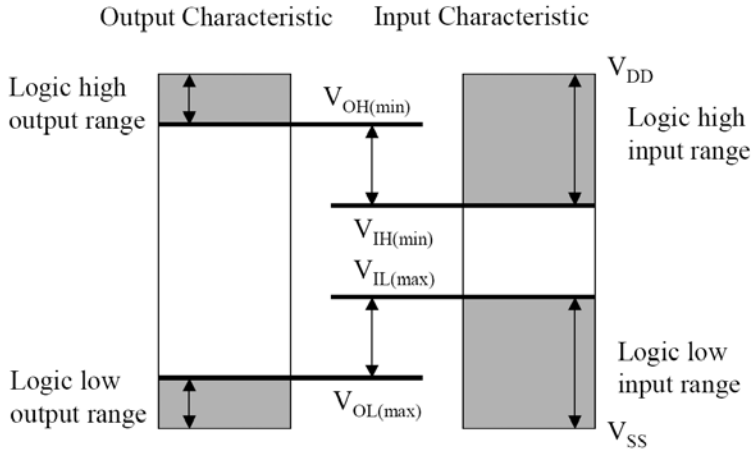
Important Parameters on VTC:

- Switching Threshold Voltage V_S or V_M
- Gain at V_S or V_M
- Output High Voltage V_{OH}
- Output Low Voltage V_{OL}
- Input High Voltage V_{IH}
- Input Low Voltage V_{IL}

Effect of Noise on a CMOS Inverter



Noise Margin



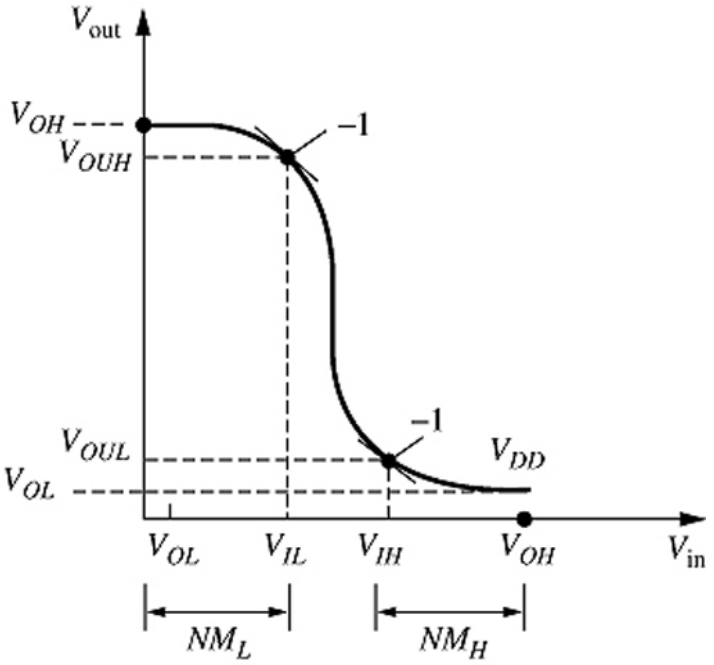
- **Noise Margin**

$$NM_H = V_{OH} - V_{IH}$$

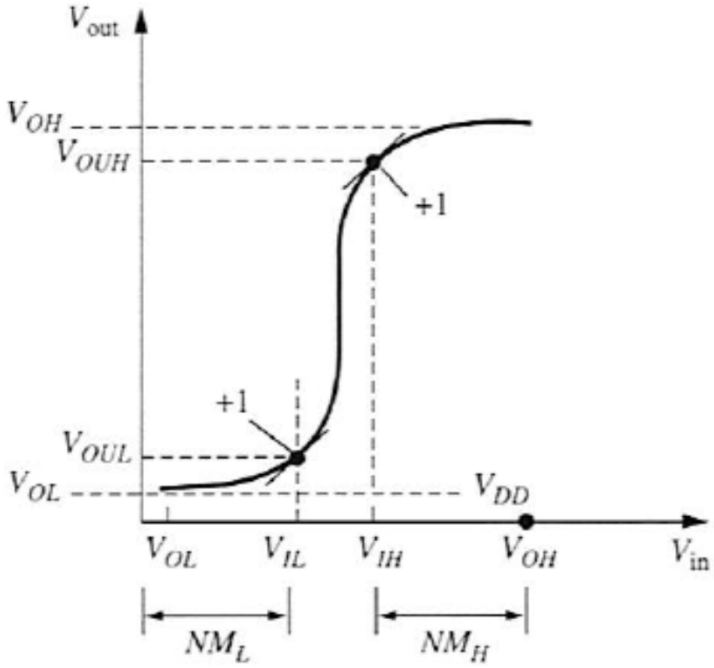
$$NM_L = V_{IL} - V_{OL}$$

- **It is better to have:**
  - $V_{OH} = V_{DD}$
  - $V_{OL} = V_{SS}$
  - Large NM_H
  - Large NM_L

Noise Margin in Inverter and Buffer



VTC of an inverter

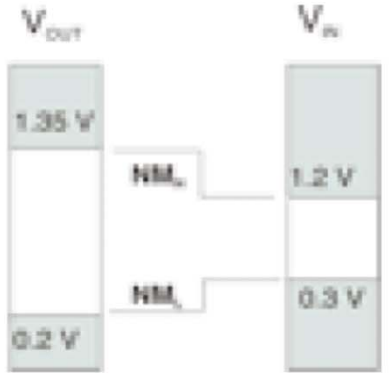


VTC of a buffer

Example: Noise Margin Calculation

An IC with $V_{DD} = 1.5$ V shows $V_{OH} = 1.35$ V, $V_{OL} = 0.2$ V, $V_{IH} = 1.2$ V, and $V_{IL} = 0.3$ V. Calculate the NM_L and NM_H for this IC.

Sketch the NM rectangles



$NM_H = 1.35 - 1.2 = 150$ mV

$NM_L = 0.3 - 0.2 = 100$ mV

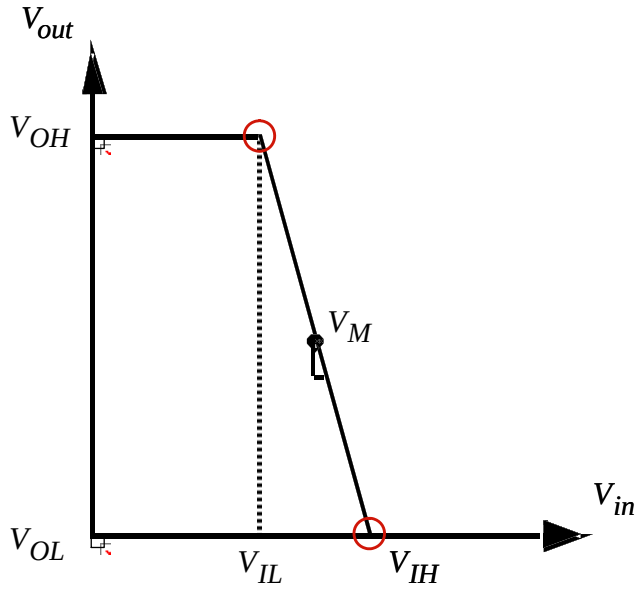
Noise Margin Approximation

- **How to compute Noise Margin**
  - Usually it is harder to compute the exact value of NM
  - Use approximation (gain factor)
  - Determine gain at V_M
  - Extrapolate V_{IL} and V_{IH}
  - V_{OL} and V_{OH} are easy to compute
- **Example:**
  - NM_L and NM_H in CMOS inverter

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$



  - where

$$g = \frac{-2}{\lambda_n + |\lambda_p|}\left(\frac{1}{V_M - V_{Tn}} + \frac{1}{V_{DD} - V_M - |V_{Tp}|}\right)$$

Example: Noise Margin Approximation

- A CMOS inverter has V_{DD}=5V is designed to have V_M=2.9V. If V_{Tn}=0.7, V_{Tp}=-0.5, λ_n=0.05 V^{-1} and λ_p=-0.08 V^{-1}. Find the noise margins NMH and NML.

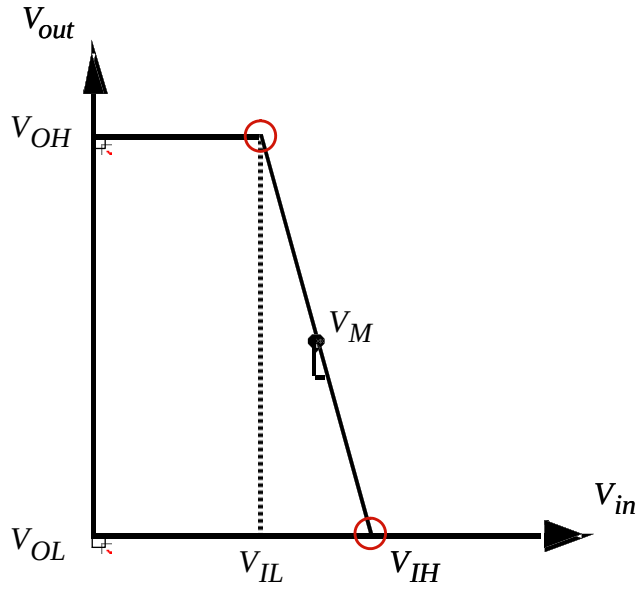
$$g = \frac{-2}{0.05+0.08}\left(\frac{1}{2.9-0.7}+\frac{1}{5-2.9-0.5}\right) = -16.6$$

$$V_{IL} = 2.9 + \frac{5-2.9}{-16.6} = 2.77V$$

$$V_{IH} = 2.9 - \frac{2.9}{-16.6} = 3.1V$$

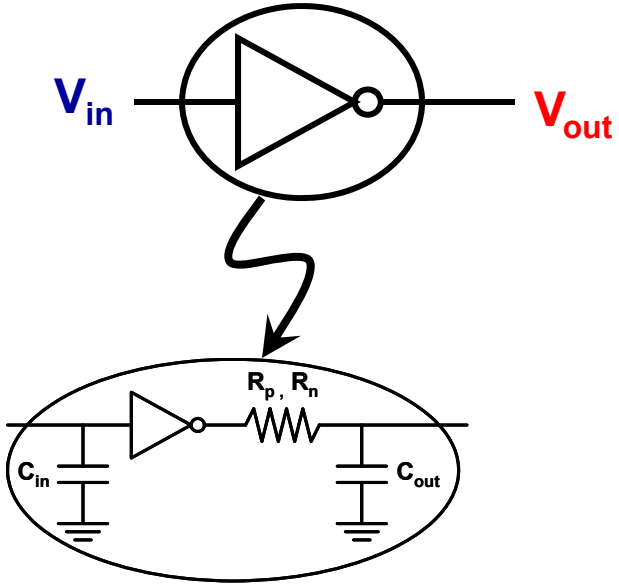
$$NMH = 5 - 3.1 = 1.9V$$

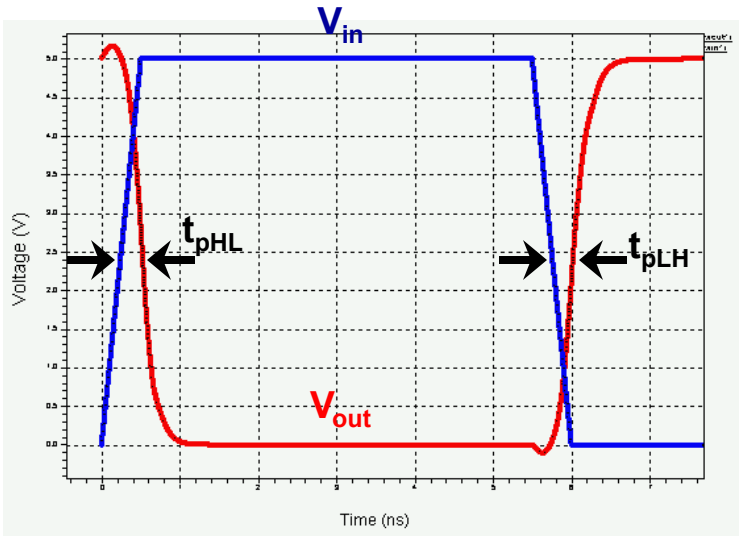
$$NML = 2.77 - 0 = 2.77V$$



Dynamic Behavior of CMOS Inverter

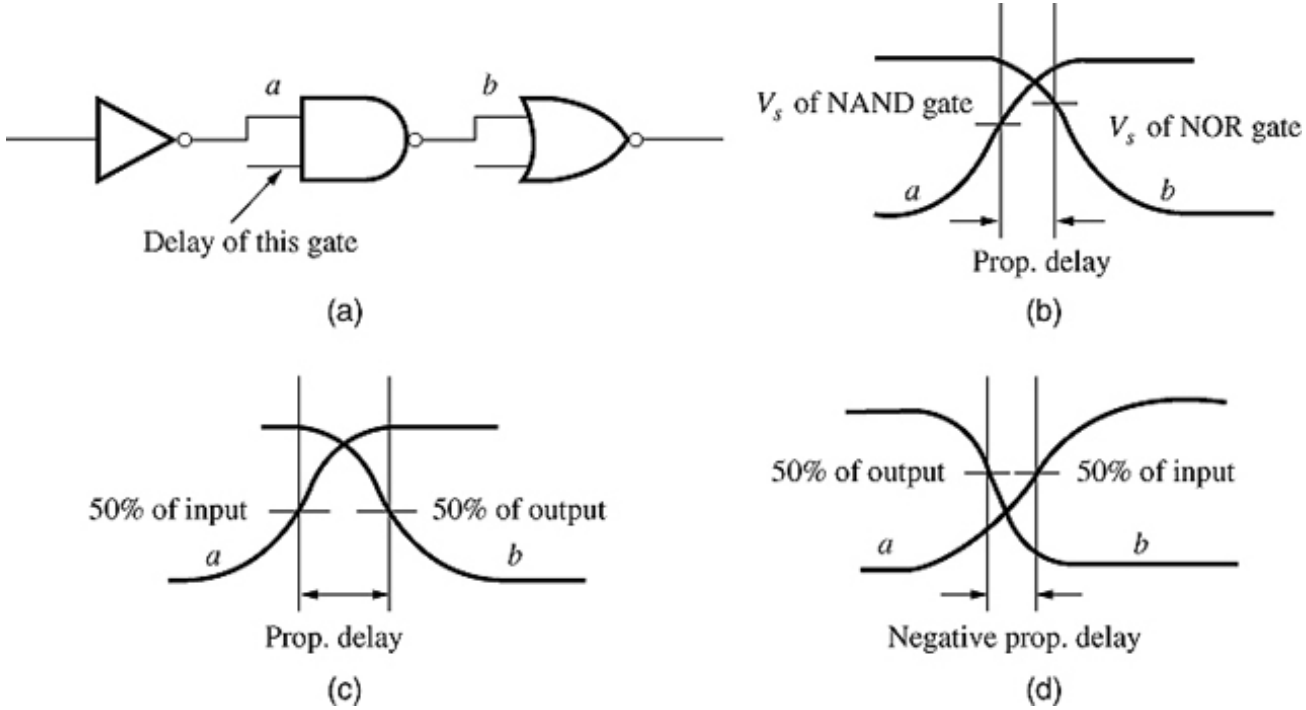
- Changing of the input doesn't instantaneously change the out pf an inverter
- This is mostly due to the time it takes to chrgae or dischage the output/load capacitor
- It is important to know how long it takes to get the signal out of the inverter or any CMOS logic gate





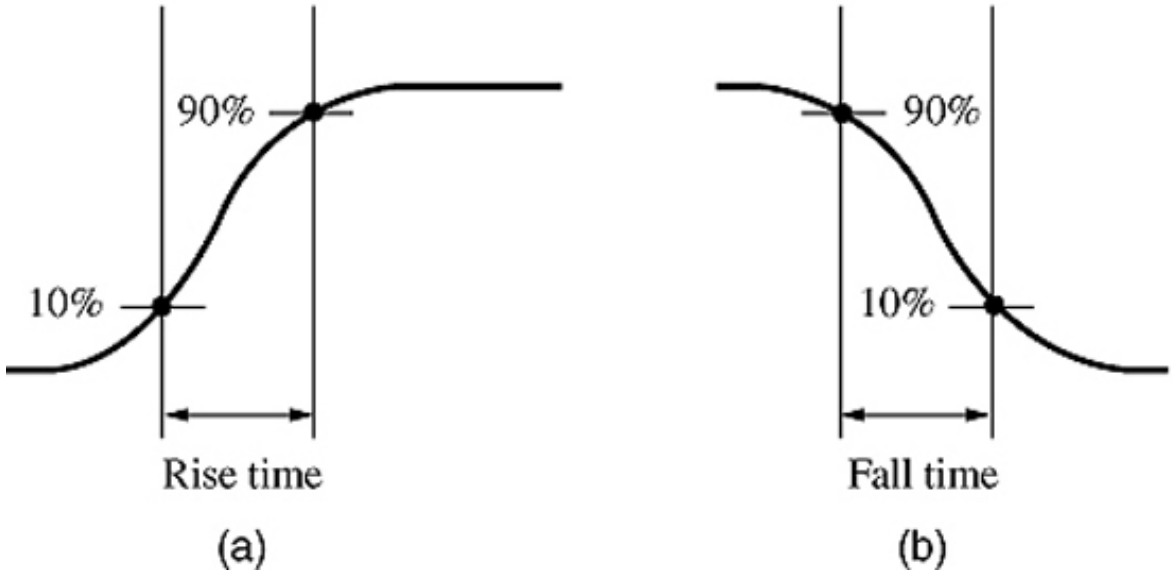
Definition: Propagation Delay

- **Definition of propagation delay**
  - **is delay from where input crosses 50%Vdd to where output crosses 50%Vdd**
  - **Remember: the value of 50%Vdd is from switching threshold voltage (V_M)**
  - **t_{pHL} is propagation delay when *output* switches from "High to Low"**
  - **t_{pLH} is propagation delay when *output* switches from "Low to High"**
- **To compute delay, the inverter must be simplified**



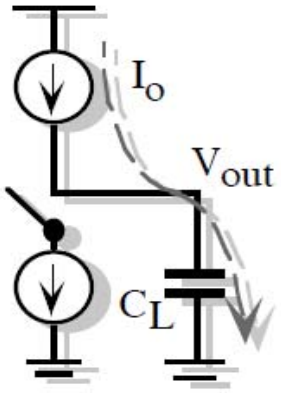
Definition: 10%-90% Rise/Fall Times

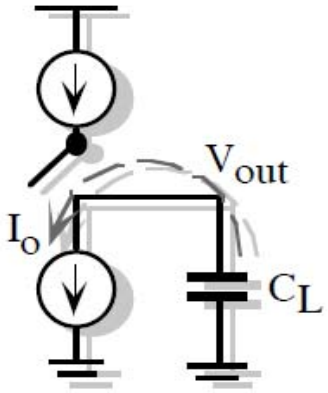
- **Definition of 10%-90% rise time**
  - **is delay from 10%Vdd to 90%Vdd in the output**
  - **t_r is the rise time when *output* switches from "Low to High"**
- **Definition of 90%-10% fall time**
  - **is delay from 90%Vdd to 10%Vdd in the output**
  - **t_f is the fall time when *output* switches from "High to Low"**

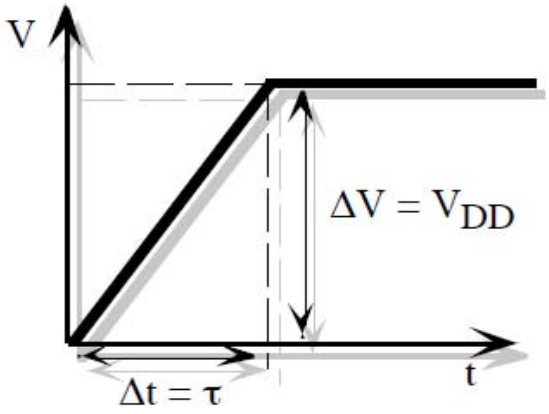


Definition: Linear Rise/Fall Times

- **Definition of rise time (Hawkin's book)**
  - **is delay from 0 to Vdd in the output assuming a constant current source model**
  - **t_r is the rise time when *output* switches from "Low to High"**
- **Definition of fall time (Hawkin's book)**
  - **is delay from Vdd to 0 in the output assuming a constant current source model**
  - **t_f is the fall time when *output* switches from "High to Low"**



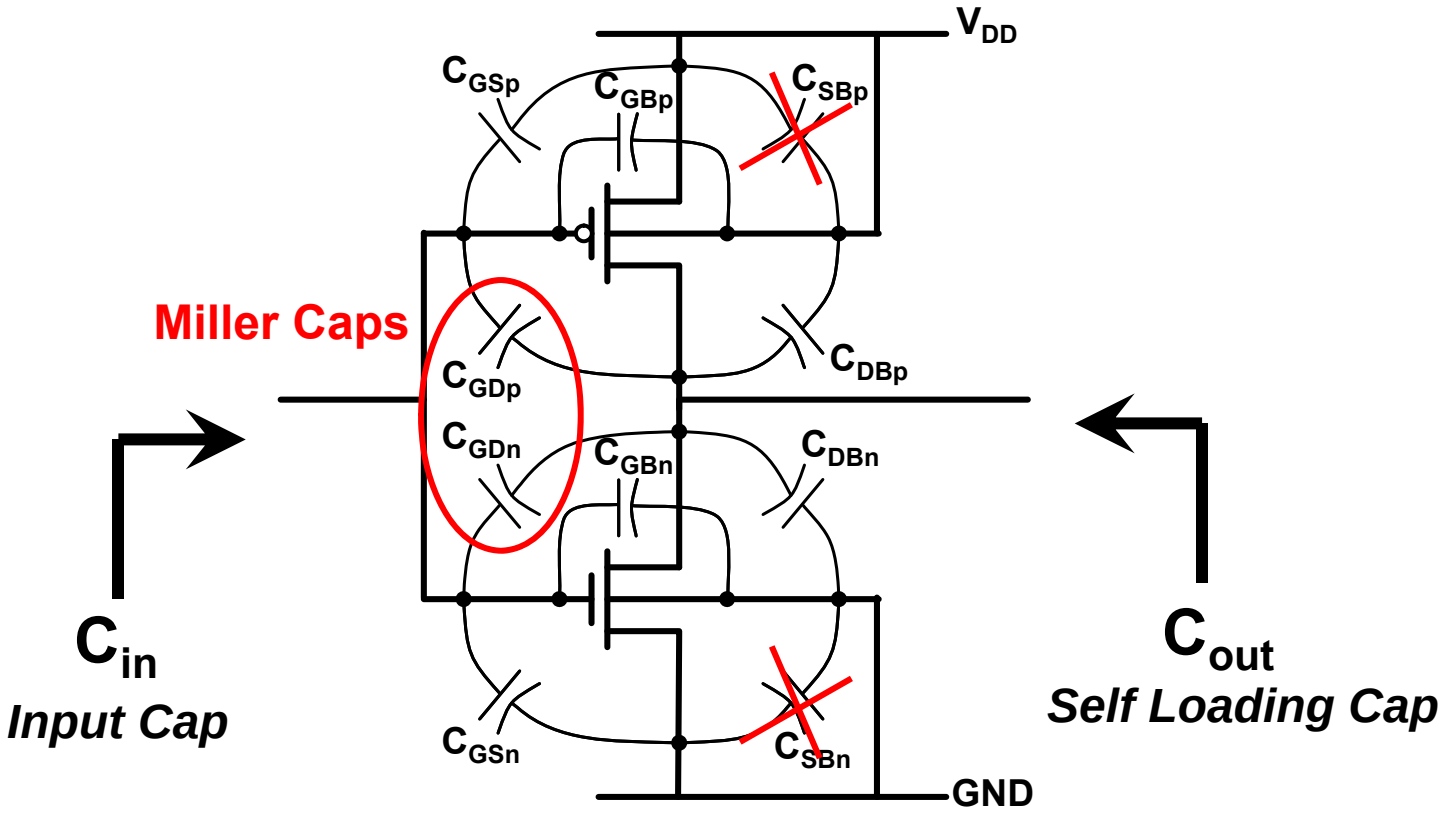




Delay Calculation in CMOS Inveretr

- It is not easy to accurately calculate delay in CMOS inverter, because
  - CMOS inverter is a non-linear circuit, therefore exact delay calculation requires solving a non-linear differential equation
  - Most of the elements in the circuit is voltage dependent (transistor drive current, parasitic capacitances, channel length modulation, etc.)
- A simplified model is required for basic calculations and design process
- Note that SPICE actually does solve the non-linear circuit accurately, but is only good for final verification, not the design

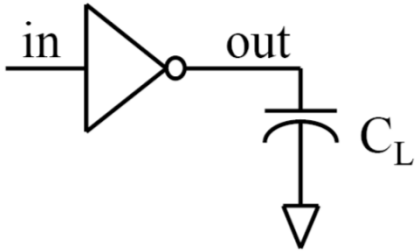
Gate Input/Output Capacitances Components

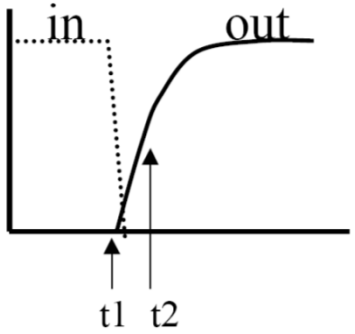


$$C_{in} = \left(C_{GDp} + C_{GSp} + C_{GBp}\right) + \left(C_{GDn} + C_{GSn} + C_{GBn}\right)$$

$$C_{out} = \left(2C_{GDp} + C_{DBp}\right) + \left(2C_{GDn} + C_{DBn}\right)$$

Propagation Delay Model

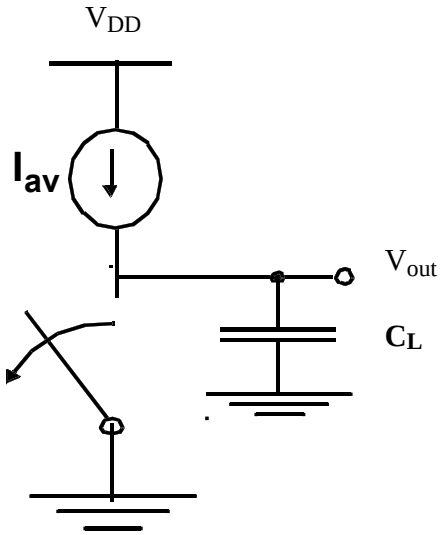




$$Q = I \cdot \Delta t = C \cdot \Delta V$$

$$\Delta t = \frac{C \cdot \Delta V}{I}$$

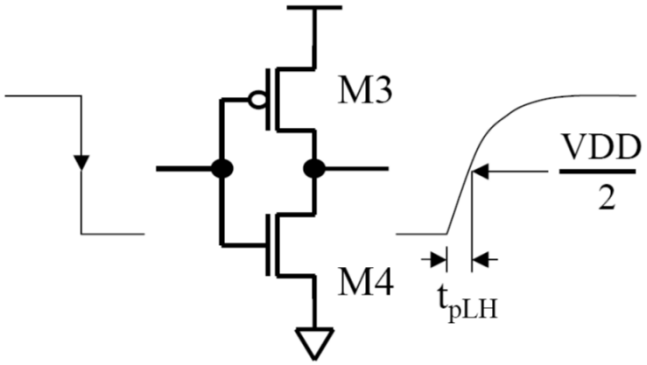
- Propagation delay is defined as the time between the input reaching $V_{DD}/2$ and the output reaching $V_{DD}/2$
- To simplify the model, let's assume I is a constant I_{av}



$$t_{pLH} = t_2 - t_1 = \frac{C_L \cdot (V_{DD}/2)}{I_{av}}$$

Propagation Delay Model

- How to compute I_{av} ?
  - Assume step input
  - NMOS goes into cutoff and stays there
  - PMOS goes into saturation at first because $|V_{DS}| > |V_{GS}| - |V_T|$
  - PMOS will transition to linear, however, before V_{out} reaches $V_{DD}/2$



$$I_{av} = \frac{I_{DS}(V_{out} = 0) + I_{DS}(V_{out} = V_{DD}/2)}{2}$$

$$I_{av} = \left(\frac{K'_p}{2}\right)\left(\frac{W_p}{L_p}\right)\left(\frac{(V_{DD} - |V_{tp}|)^2}{2} + \frac{V_{DD}(V_{DD} - |V_{tp}|)}{2} - \frac{V_{DD}^2}{8}\right)$$

Propagation Delay Model

- A simpler model for I_{av} can be obtained by assuming that the PMOS stays in saturation the whole time, therefore acts as an ideal current source

$$I_{av} = \left(\frac{K'_p}{2}\right)\left(\frac{W_p}{L_p}\right)\left(V_{DD} - |V_{tp}|\right)^2$$

$$t_{pLH} = t_2 - t_1 = \frac{C_L \cdot (V_{DD}/2)}{I_{av}} \quad \Rightarrow \quad t_{pLH} = \frac{C_L \cdot V_{DD}}{K'_p\left(\frac{W_p}{L_p}\right)\left(V_{DD} - |V_{Tp}|\right)^2}$$

- Assuming $V_{DD} >> V_{Tp}$

$$t_{pLH} = \frac{C_L}{K'_p\left(\frac{W_p}{L_p}\right)V_{DD}}$$

- Same arguments hold for t_{pHL}

Minimum Delay Design Techniques

- Reduce C_{in} and C_{out} – Careful layout, keep drain diffusion area as small as possible
- Reduce wiring capacitance – Careful layout, keep devices as close as possible
- Increase (W/L) of devices – Need to be careful not to get into self-loading effect
- Increase V_{DD} – Need to be careful not to get into V_{DSAT} or velocity saturation

Example: CMOS Inverter Delay

- **A CMOS inverter has V_{DD}=5V is designed such that $(W/L)_n$=10 and $(W/L)_p$=20. Assume that V_{Tn}=0.7, V_{Tp}=-0.6, K'_n=100 uA/V^2, K'_p=-60 uA/V^2, and the load capacitance is 100fF.**

  1) Use I_{av} model to find t_{pHL}, t_{pLH}, $t_{r(10\%-90\%)}$, and $t_{f(90\%-10\%)}$.

  2) Use constant current source model to find t_{pHL}, t_{pLH}, $t_{r(10\%-90\%)}$, $t_{f(90\%-10\%)}$, t_r, and t_f.

- ***Answers:***

  1) t_{pHL}=29.64 ps, t_{pLH}=23.73 ps, $t_{r(10\%-90\%)}$=56.71 ps, and $t_{f(90\%-10\%)}$=70.98 ps

  2) t_{pHL}=27.04 ps, t_{pLH}=21.52 ps, $t_{r(10\%-90\%)}$=34.43 ps, and $t_{f(90\%-10\%)}$=43.27 ps, t_r=43.04 ps and t_f=54.98 ps.