ECE321 – Electronics I

Lecture 13: CMOS Inverter: Dynamic Power

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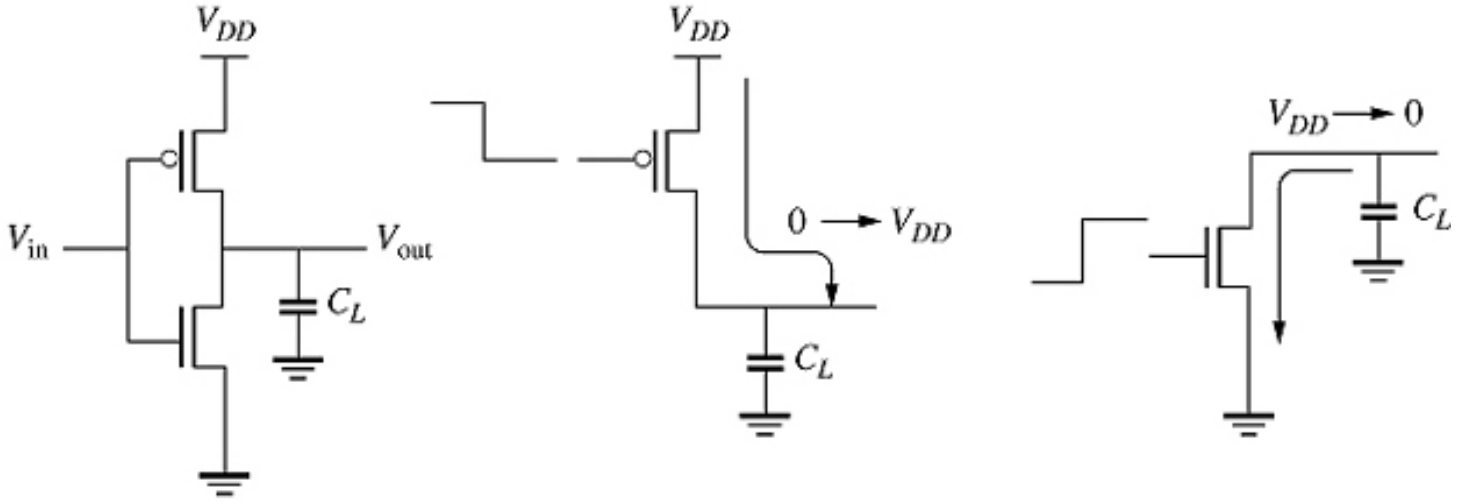
Review of Last Lecture

- **Propagation Delay**
- **Rise and Fall Times**
- **Input and Self Loading (Load) Capacitances**
- **Delay Approximation**

Today's Lecture

- **Mostly Review of Lecture 2 for Dynamic Power Calculation**

CMOS Dynamic Power Consumption



$$P_d = \frac{1}{T}\int_0^T i_{VDD}(t)\cdot V_{DD}\,dt = \frac{V_{DD}}{T}\int_0^T C_L\frac{dV_{out}}{dt}\,dt = \frac{C_L V_{DD}}{T}\int_0^{V_{DD}} dV_{out} = \frac{C_L V_{DD}^2}{T} = C_L V_{DD}^2 f$$

- Need to reduce C_L , V_{DD}, or f to reduce power

Computing Active Power

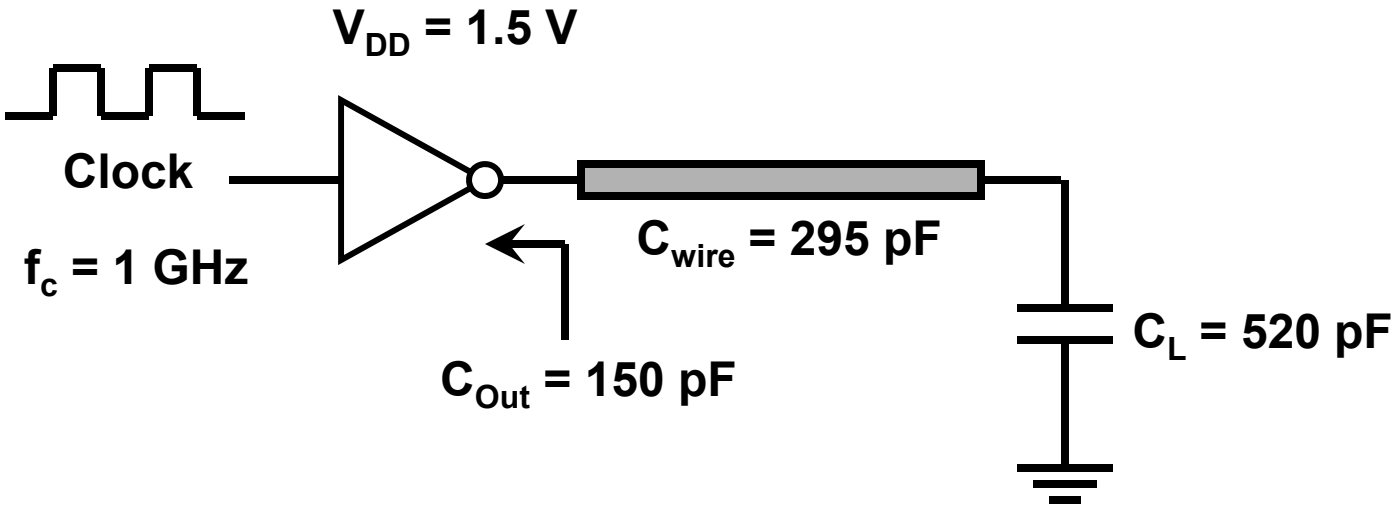
- For clock circuit that toggles twice in each period (low-to-high and high-to-low), the active power consumption is computed as:

$$P_{active} = C_L V_{DD}^2 f$$

- For non-clock circuits that toggles occasionally (with probability of α) once in each period, the active power consumption is computed as:

$$P_{active} = \frac{1}{2}\alpha C_L V_{DD}^2 f = \frac{1}{2}\left(\alpha_{0\to1} + \alpha_{1\to0}\right) C_L V_{DD}^2 f$$

Example: Active Power in a Clock Driver



In this circuit, compute the power consumption in the inverter.

Answer: 2.17 W

Minimum Power Design Techniques

- **Prime choice: Reduce voltage!**
  - **Recent years have seen an acceleration in supply voltage reduction**
  - **Design at very low voltages still open question (0.6 … 0.9 V by 2015!)**
- **Reduce switching activity**
- **Reduce physical capacitance**
- **Reduce clock frequency, but use multi-core architecture to enhance performance**