

# ECE321 – Electronics I

## Lecture 16: Gate Sizing (Inverter Chain)

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**Payman Zarkesh-Ha**

*Office: ECE Bldg. 230B*

*Office hours: Tuesday 2:00-3:00PM or by appointment*

*E-mail: [pzarkesh.unm.edu](mailto:pzarkesh.unm.edu)*

# *Review of Last Lecture*

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- ❑ Leakage Current and Power

# *Today's Lecture*

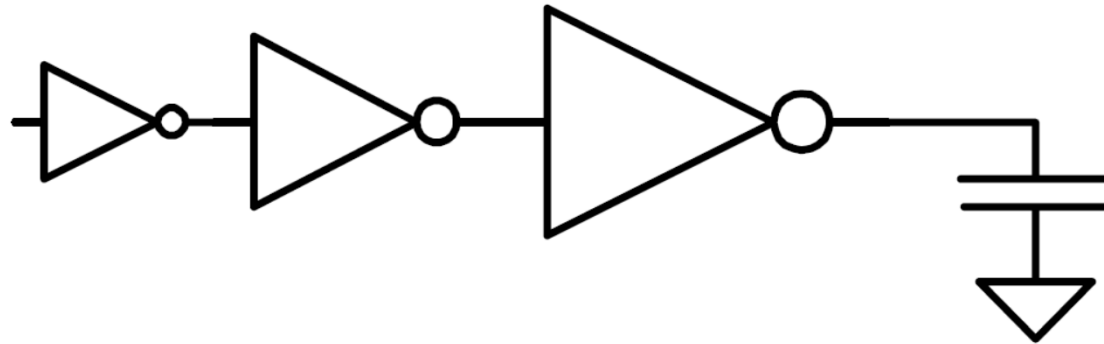
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- ❑ **Gate Sizing (Inverter Chain)**

# Sizing Logic Path for Speed

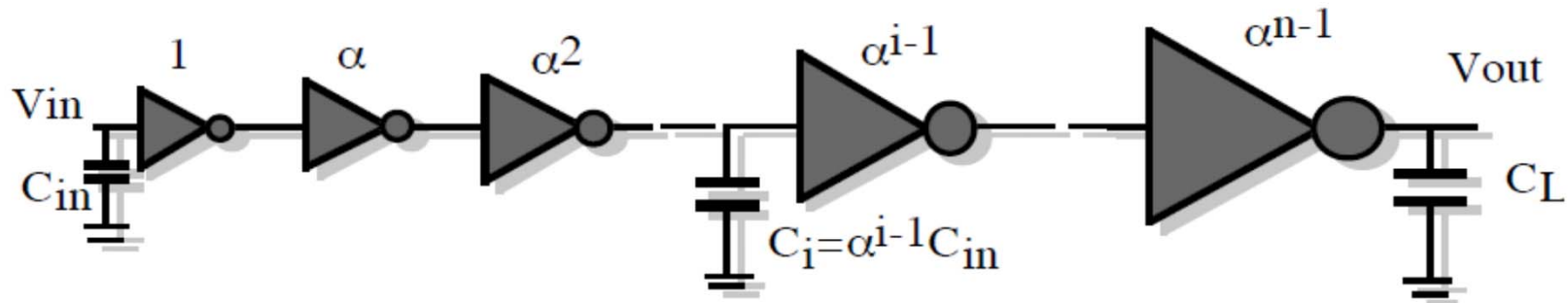
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- ❑ Frequently, input capacitance of a logic path is constrained
- ❑ Logic also has to drive some capacitance
  - Example: output pad capacitive load is in the order of 10pF
- ❑ How do we size the inverter chain to achieve maximum speed?



- ❑ Wide gate to drive a large load must be driven in turn
  - Large block inputs “push their load into the chip”

# Inverter Chain

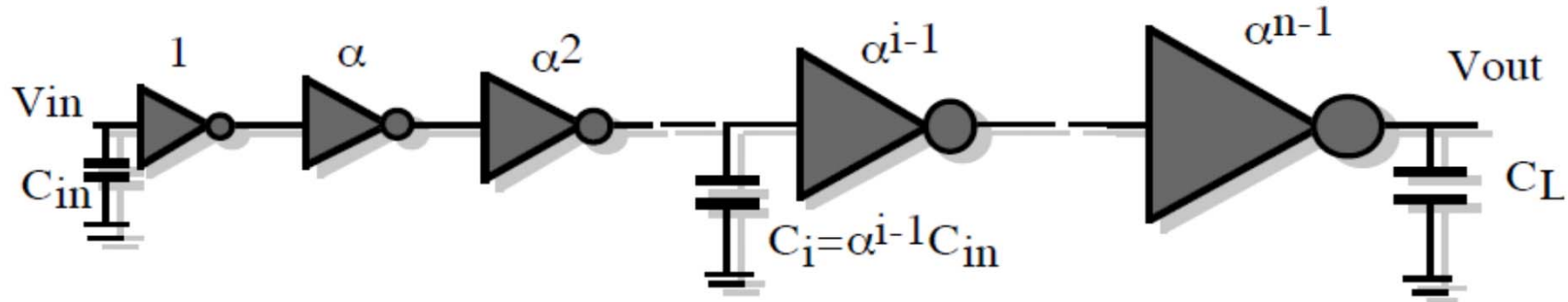


$$C_i = \alpha^{i-1} C_{in} \quad i = 1, 2, \dots, n \quad \Rightarrow \quad C_L = \alpha^n C_{in}$$

$$\alpha^n = \frac{C_L}{C_{in}} \quad \Rightarrow \quad n = \frac{\ln\left(\frac{C_L}{C_{in}}\right)}{\ln \alpha}$$

$$t_{di} = \alpha \tau_0 \quad i = 1, 2, \dots, n \quad \Rightarrow \quad t_d = \sum_{i=1}^n t_{di} = n \alpha \tau_0 \quad \Rightarrow \quad t_d = \ln\left(\frac{C_L}{C_{in}}\right) \frac{\alpha}{\ln \alpha} \tau_0$$

# Optimization Results



$$\alpha_{opt} = e \approx 2.7 \quad \longrightarrow \quad n_{opt} = \ln\left(\frac{C_L}{C_{in}}\right)$$

$$t_d = \sum_{i=1}^n t_{di} = n\alpha\tau_0$$

# Example 1: Optimum Inverter Chain

An IC with a tapered buffer drives a load capacitance on a board that is 100 pF. The input capacitance of the logic gate originating the signal is 100 fF, and that gate has  $W/L = 4$ .

(a) How many buffer gates are required to optimally drive that load using the fixed tapered buffer model?

*Answer:*

$$n = 6.9$$

Seven total stages are needed. We must insert five tapered stages between the original gate and the output driver.

(b) Write the equation that predicts the  $W/L$  ratio of the final buffer in terms of the scaling factor and the originating gate  $W/L$

(c) What is the  $W/L$  ratio of the final output buffer driver to the board?

*Answer:*

$$W/L = 1,614$$