ECE321 – Electronics I

Lecture 17: Interconnect Modeling I

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Review of Last Lecture

- **Gate Sizing (Inverter Chain)**

Today's Lecture

- **Interconnect Resistance**
- **Interconnect Capacitance**
- **Interconnect Inductance**

Interconnect Modeling

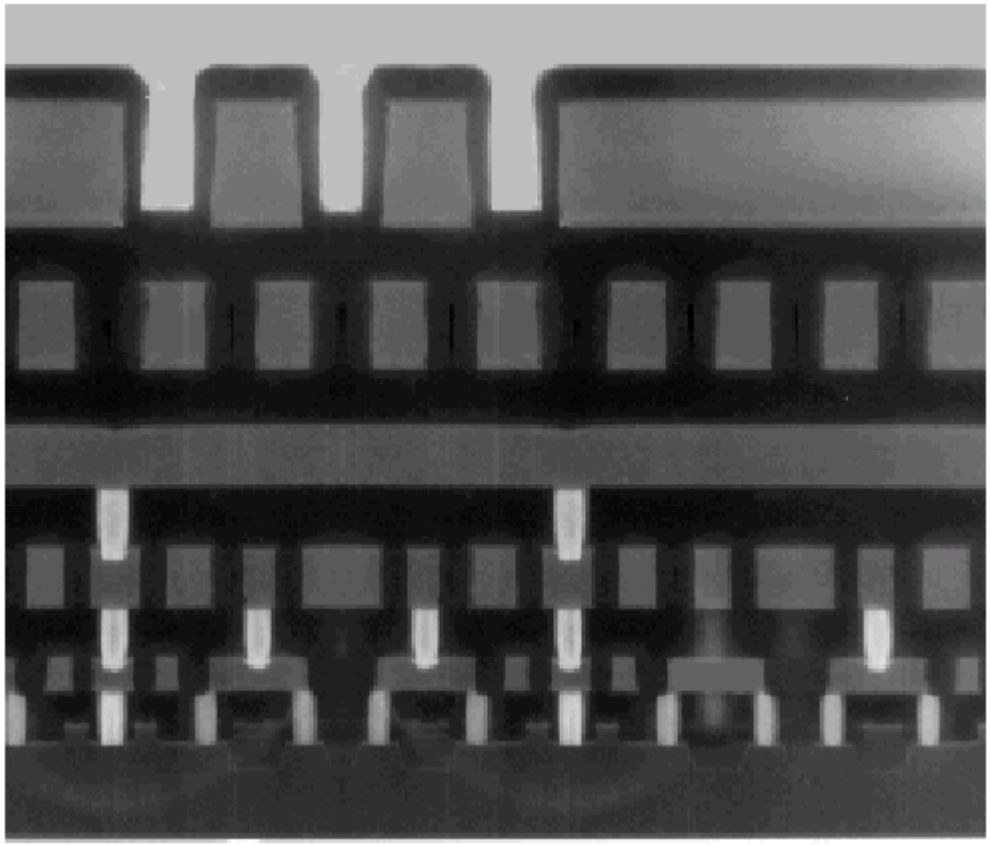
- **Interconnect parasitics**
  - reduce reliability (crosstalk noise)
  - affect performance and power consumption
- **Interconnect Modeling**
  - Parasitic Capacitance
  - Parasitic Resistance
  - Parasitic Inductance

Example: Intel 0.25um backend process

5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

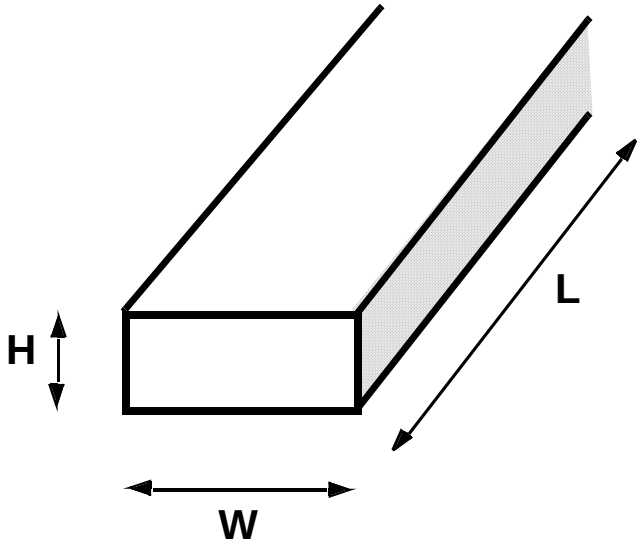
LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio



Interconnect Resistance

- Extraction of interconnect capacitance is simpler except for special cases (test chips where accurate resistance of a pattern is needed)
- Sheet resistance is an easy method of resistance measurement in layout (Only the metal aspect ratio is needed, no thickness information)



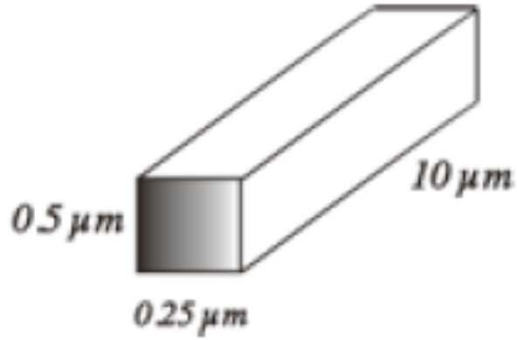
$$R = \frac{\rho L}{WH}$$

$$R = \left(\frac{\rho}{H}\right)\frac{L}{W} = R_{\square}\frac{L}{W}$$

Sheet Resistance

Example: Interconnect Resistance

If the line is made of Cu, calculate the line resistance using sheet resistance at T= 20°C.



The sheet resistance is $R_{square} = \frac{\rho}{t} = \frac{1.72\,\mu\Omega \bullet \text{cm}}{0.5\,\mu m} \times \frac{10^4\,\mu m}{\text{cm}} = \frac{33.99\,\text{m}\Omega}{\text{square}}$

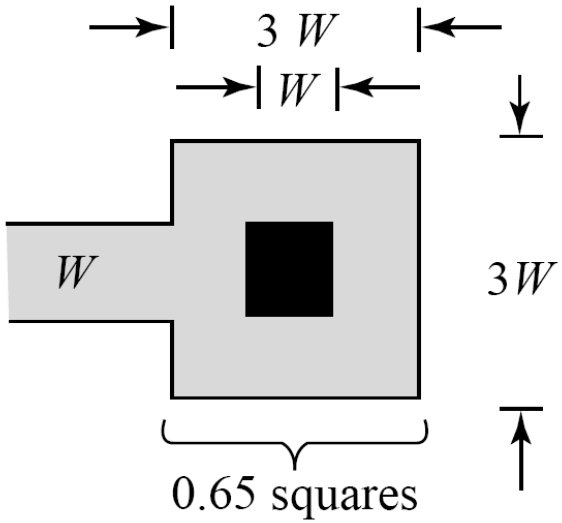
And the total number of squares is l/w = 10 μm/0.25 μm = 40 squares. The total resistance is then

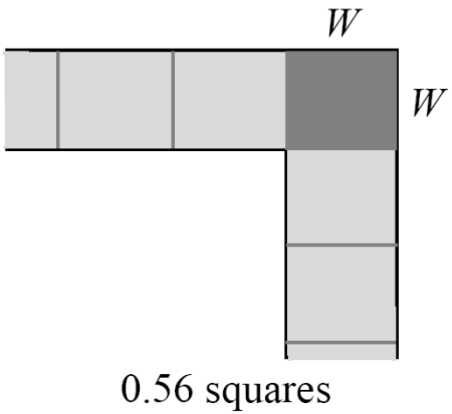
$$R = 33.99\ m\Omega \times 40 = 1.360\ \Omega$$

You get the same result from Eq (1), but deal with one less constant in the sheet resistance calculation.

Sheet Resistance

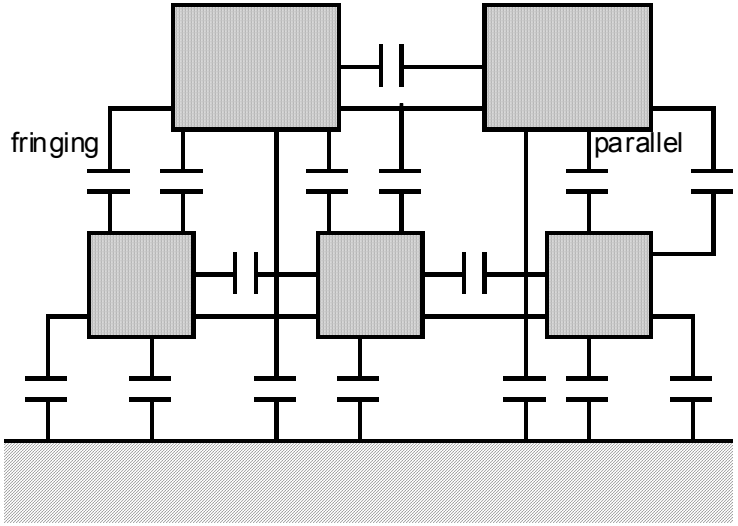
- Measurement shows that the effective number of squares of the "dog bone" style contact region is 0.65 and for a 90º corner is 0.56





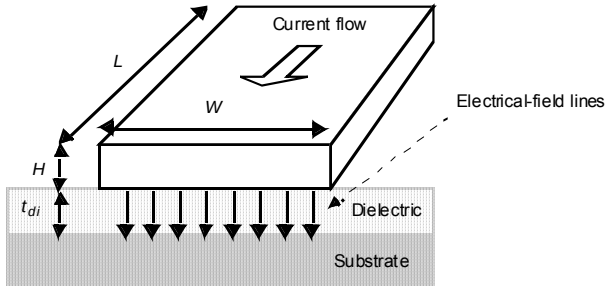
Interconnect Capacitance

- Extraction of interconnect capacitance in modern VLSI technology is very complicated because of
  - Non-homogenous dielectric (etch stop, barrier liner, etc.)
  - Complex pattern of neighboring interconnects (need 3D modeling)
- There are two types of capacitances:
  - Ground capacitances
  - Coupling capacitances



Interconnect Capacitance Modeling

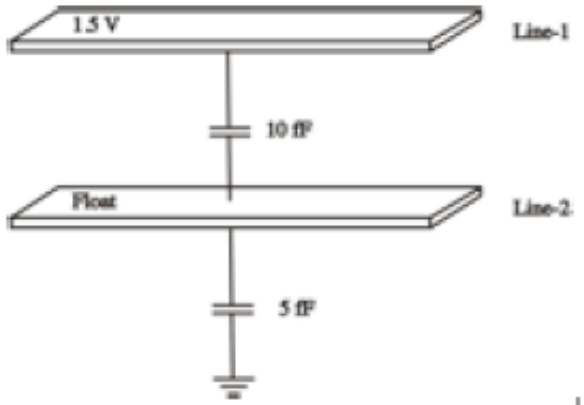
- Often simple parallel plate model is used for hand calculation



$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Example:

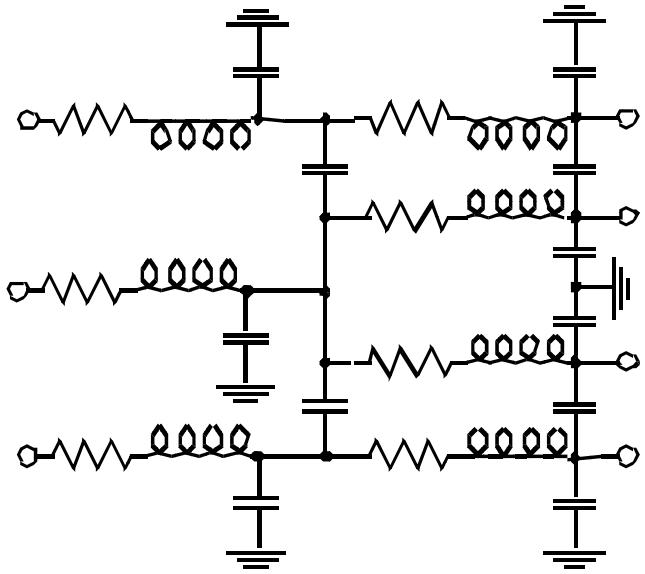
Consider the static situation in the figure where line-1 is at 1.5 V and line-2 is floating. What is the induced voltage on line-2?



$$V_2 = \left[\frac{10}{10+5}\right] 1.5\ \text{V} = 1.0\ \text{V}$$

Interconnect Inductance

- Extraction and modeling of interconnect inductance is extremely hard because of
  - Non-identified return path
  - Unlike capacitance, the effect of inductance goes beyond nearest neighbors
- It is used only for specific nets such as clock and power supply interconnects
- Has not yet been used by industry for timing analysis



Example: Inductance in Power Supply

The inductance in a particular IC connecting metal is 200 pH. What is the inductive voltage generated during a current rise time of 10^9 A/s?

$$v_L = L\frac{di}{dt} = 200 \times 10^{-12} \times 10^9 = 200 \text{ mV}$$

Many ICs use power supply voltages on the order of 1.0 V and less. A 200 mV inductive bite is a severe temporary weakening of the normal voltage that drives logic circuitry.

Dealing with Interconnect Parasitics

- **Reduce interconnect Capacitance**
  - Use better dielectric material (low-K dielectric)
  - Reduce wire-length (efficient layout)
  - Increase wire spacing
- **Reduce Interconnect Resistance**
  - Use better conductor material (Copper)
  - Reduce wire-length (efficient layout)
  - Increase wire width
- **Reduce Interconnect Inductance**
  - Use proper return path
  - Slow down the ramp time