ECE321 – Electronics I

Lecture 18: Interconnect Modeling II

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Review of Last Lecture

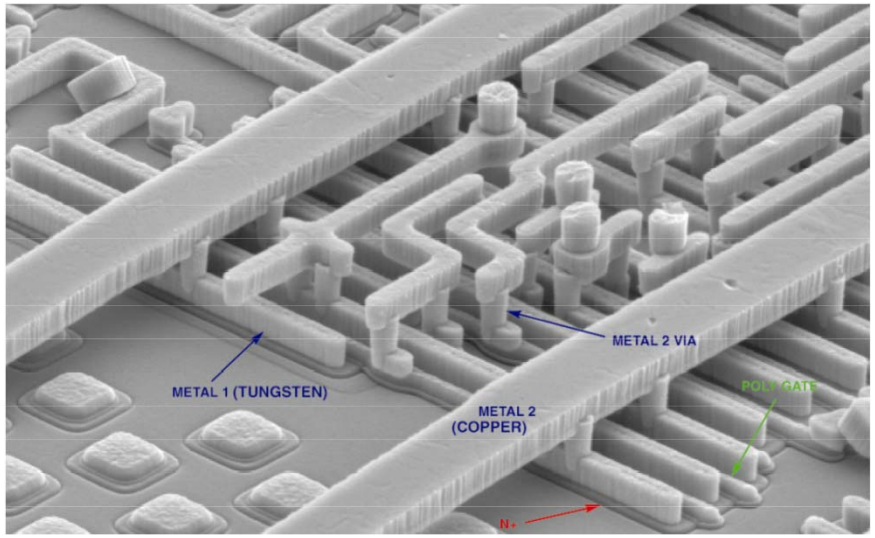
- Interconnect Resistance
- Interconnect Capacitance
- Interconnect Inductance

Today's Lecture

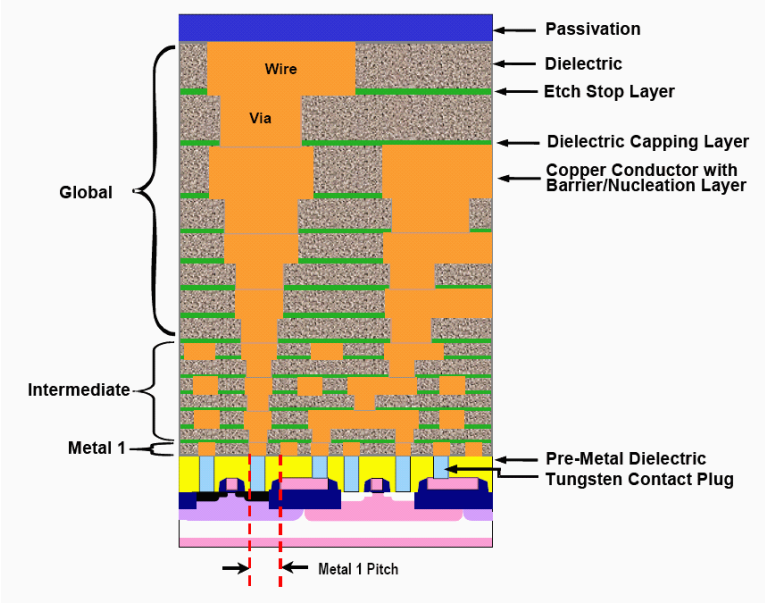
- **Miller Effect**
- **Interconnect Delay**
- **Elmore Delay**

Interconnect Complexity

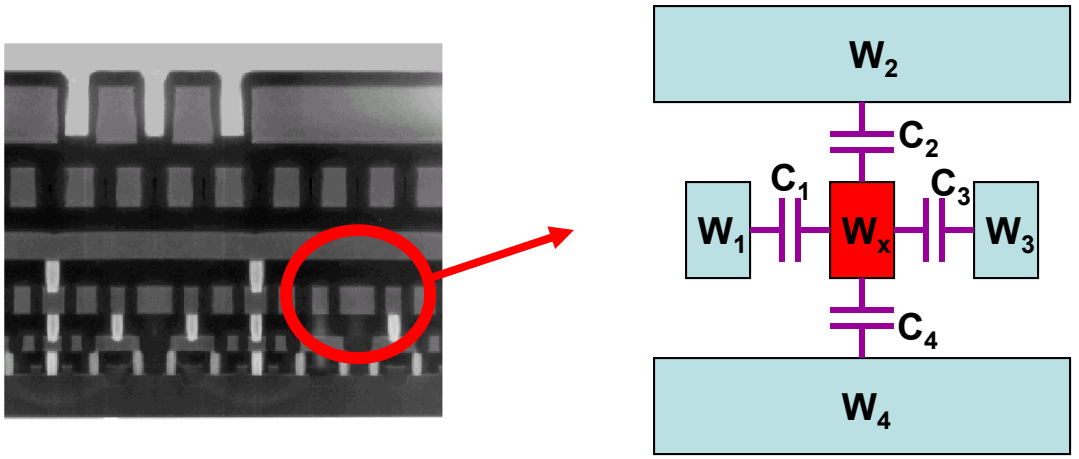
- Interconnects are getting more complex as technology improves
- Current technology can have 12 layers of metal ranging from 1um to 10,000um length
- Wire pitch is 90nm for 45nm technology node



Technology	65 nm (now)	45 nm (2008)	32 nm (2010)
Wire width	65 nm	45 nm	32 nm
Wire Thickness	115 nm	80 nm	60 nm
Total Number of Wires	60 Million	150 Million	300 Million
Total wire length	1 mile	1.4 mile	2 mile



Effective Capacitance & Miller Effect



- If W_1, W_2, W_3, and W_4 are grounded (not switching), then the total capacitance that the W_x wire sees is:

$$C_x = C_1 + C_2 + C_3 + C_4$$

- If W_2, and W_4 are grounded but W_1 and W_3 switches in the same direction of W_x, then the total capacitance that the W_x wire sees is:

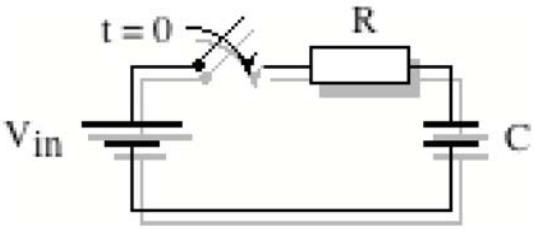
$$C_x = C_2 + C_4$$

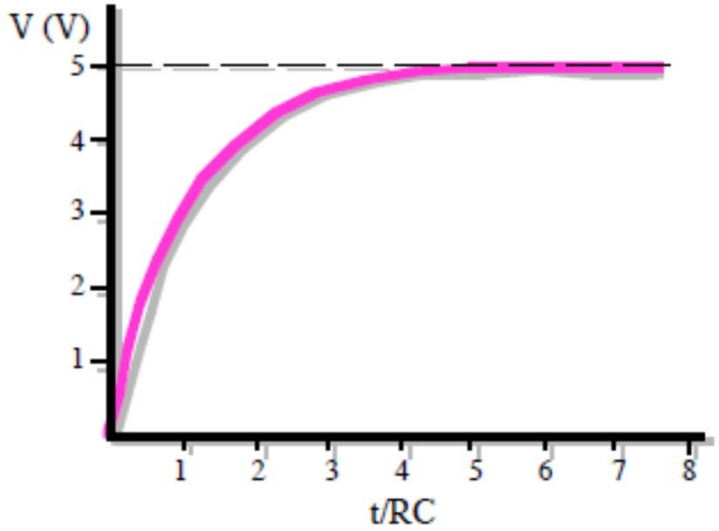
- If W_2, and W_4 are grounded but W_1 and W_3 switches in the opposite direction of W_x, then the total capacitance that the W_x wire sees is:

$$C_x = 2C_1 + C_2 + 2C_3 + C_4$$

Interconnect Time Constant & Delay

- Interconnect circuit can be simplified as an RC network.
- The time constant of an interconnect is simply $\tau = RC$
- However, the propagation delay of an RC interconnect is 0.7RC. Why?



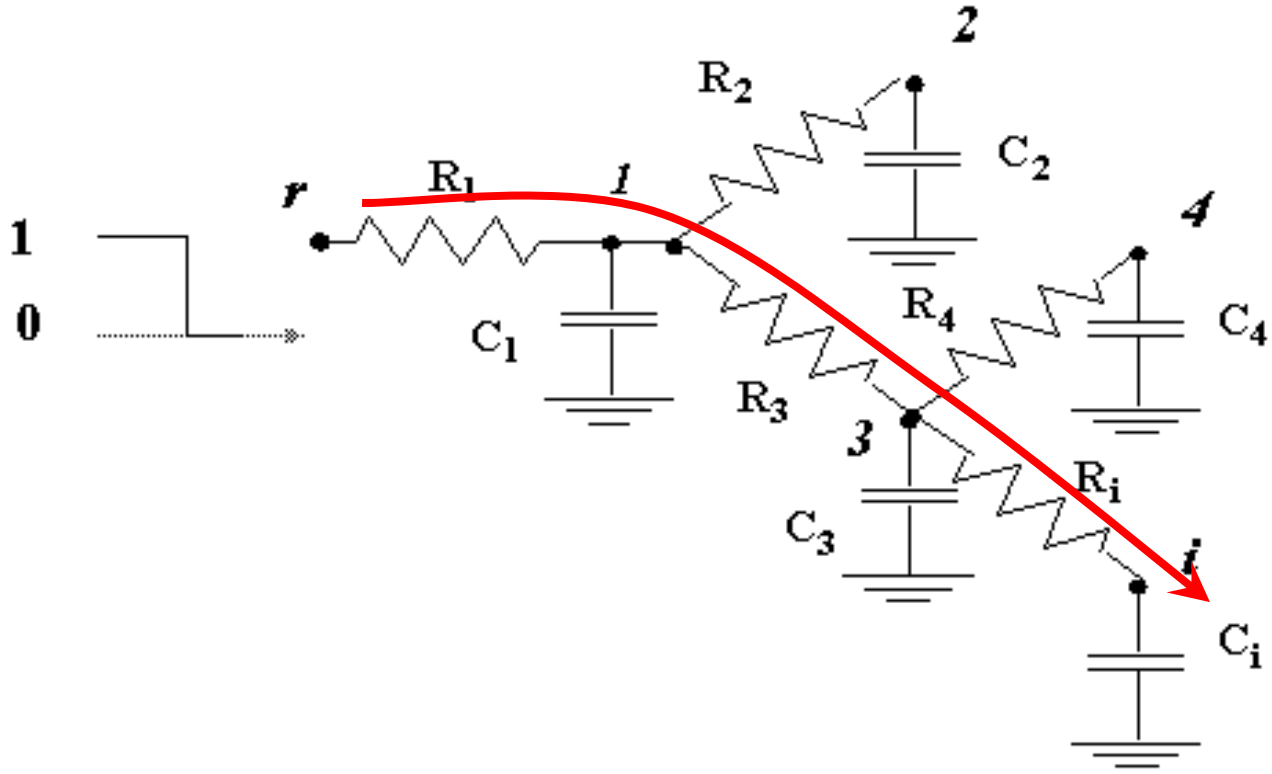


$$\tau = RC$$

$$t_{PHL} = t_{PLH} = 0.7RC = 0.7\tau$$

** Beware that in Prof. Hawkins book the time constant is sometimes called propagation delay*

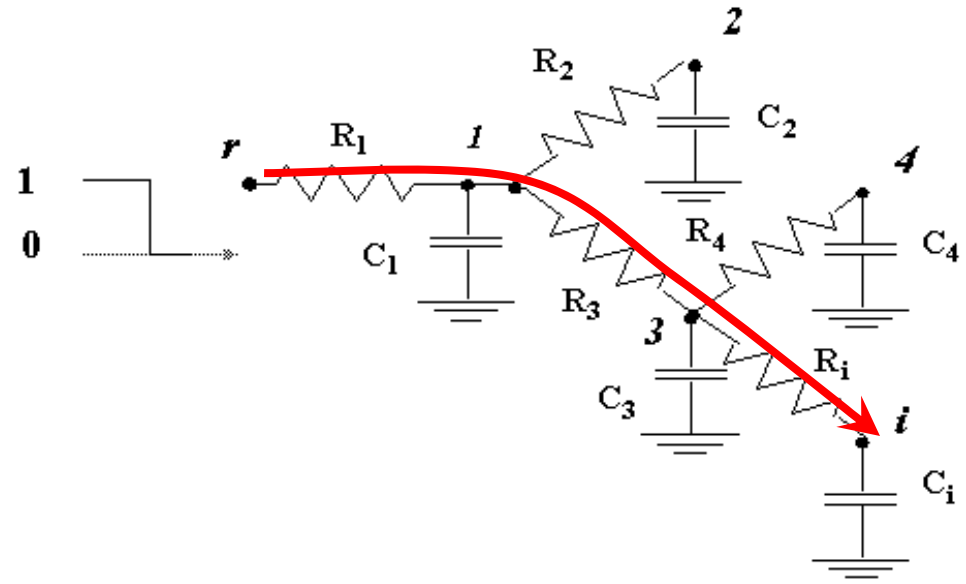
Real Interconnect Circuit Model



How to compute the delay from node r to node I in this complex RC network?

Answer: Use Elmore delay formula!

Elmore Delay Formula

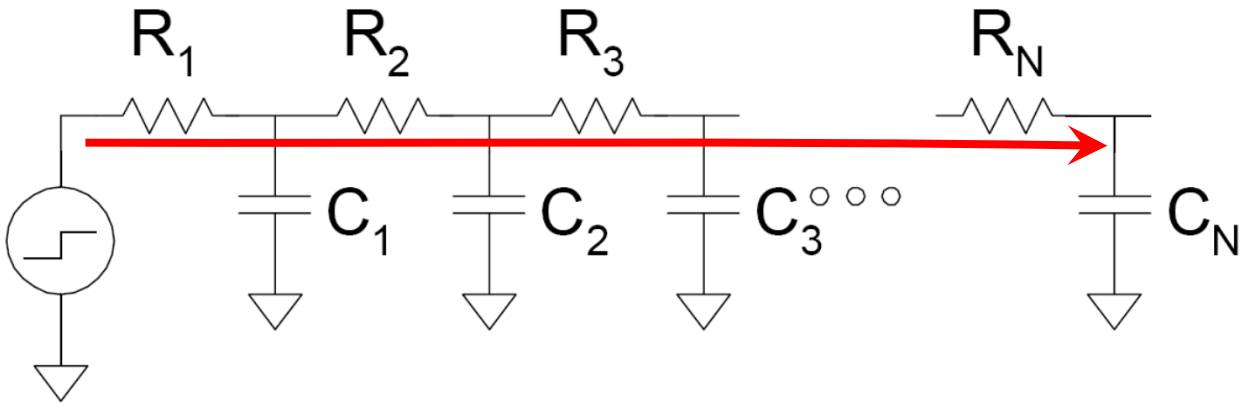


$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \to i) \cap path(s \to k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

$$\tau_{Di} = R_1C_1 + R_1C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3 + R_i)C_i$$

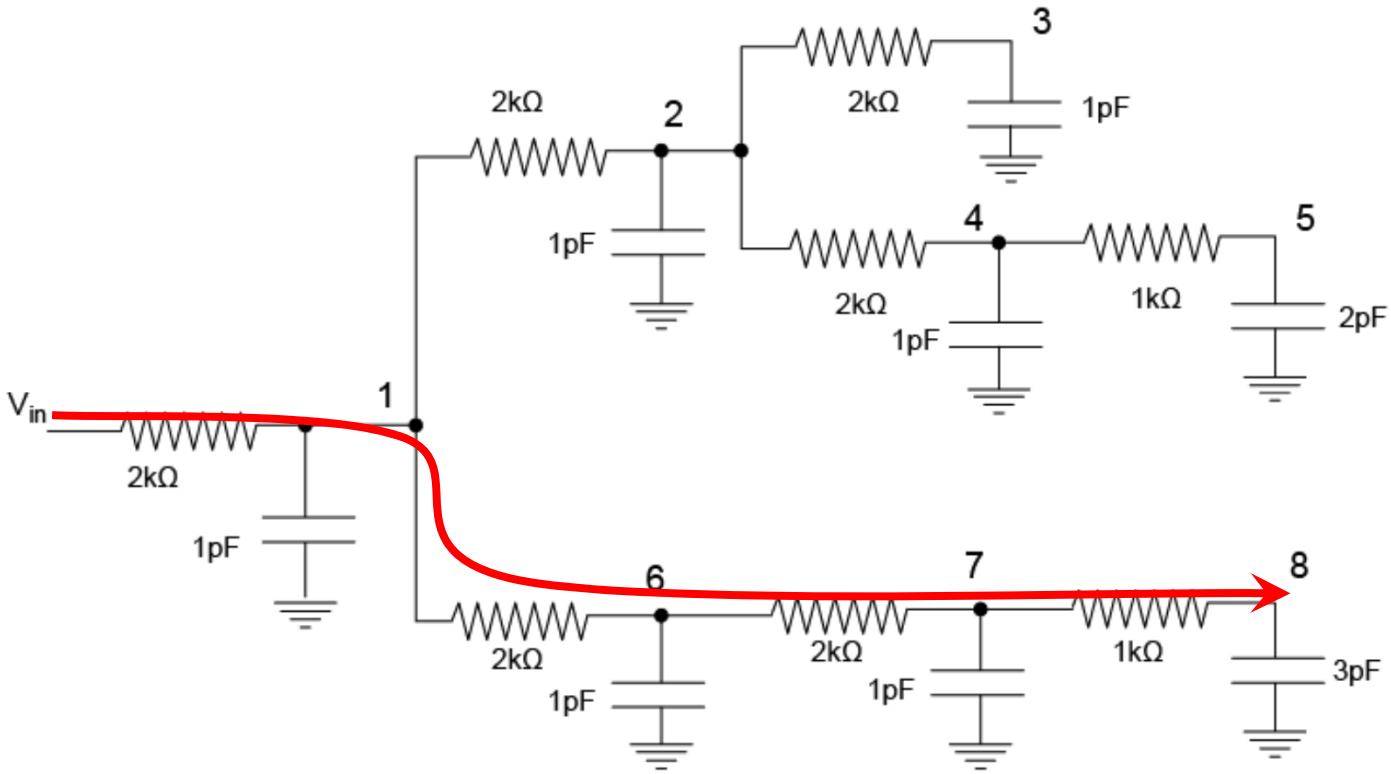
Example 1: Elmore Delay in RC Ladder



$$\tau_{Di} = \sum_{k=1}^{N} R_{ki} C_k$$

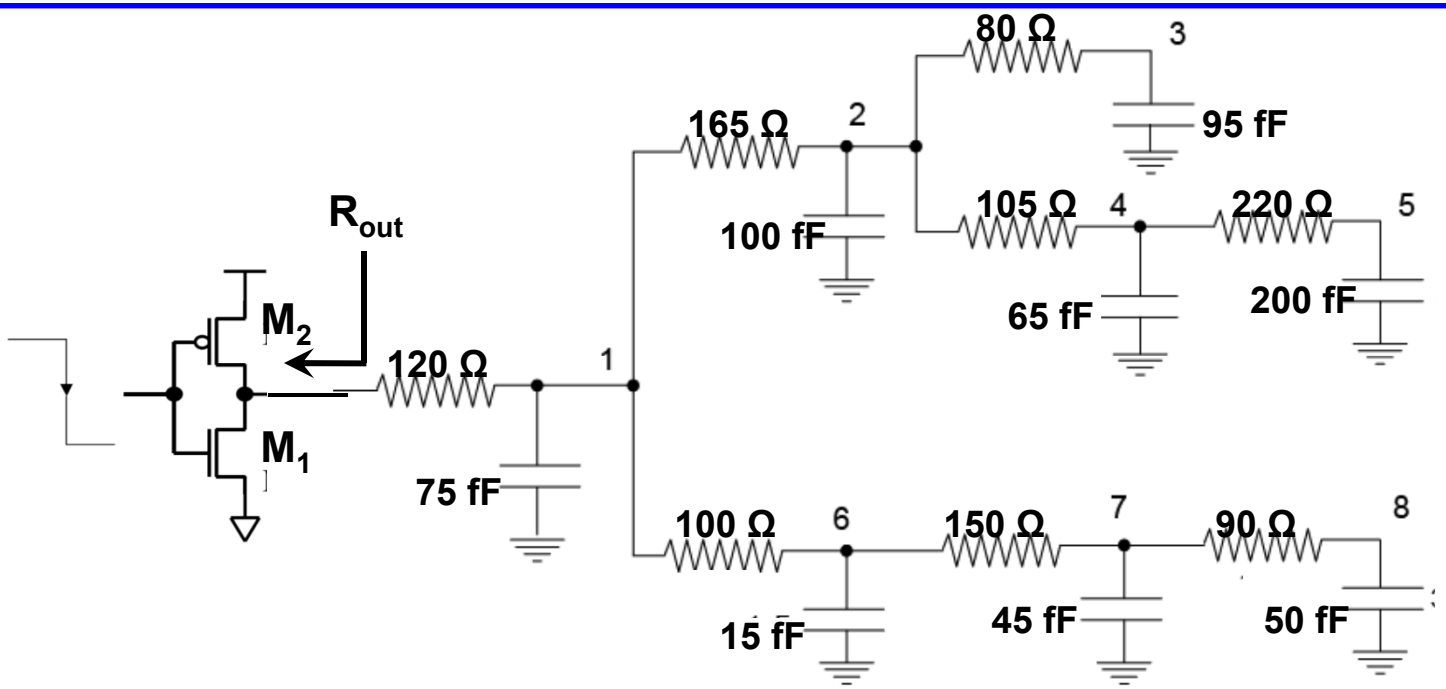
$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$

Example 2: Another Elmore Delay



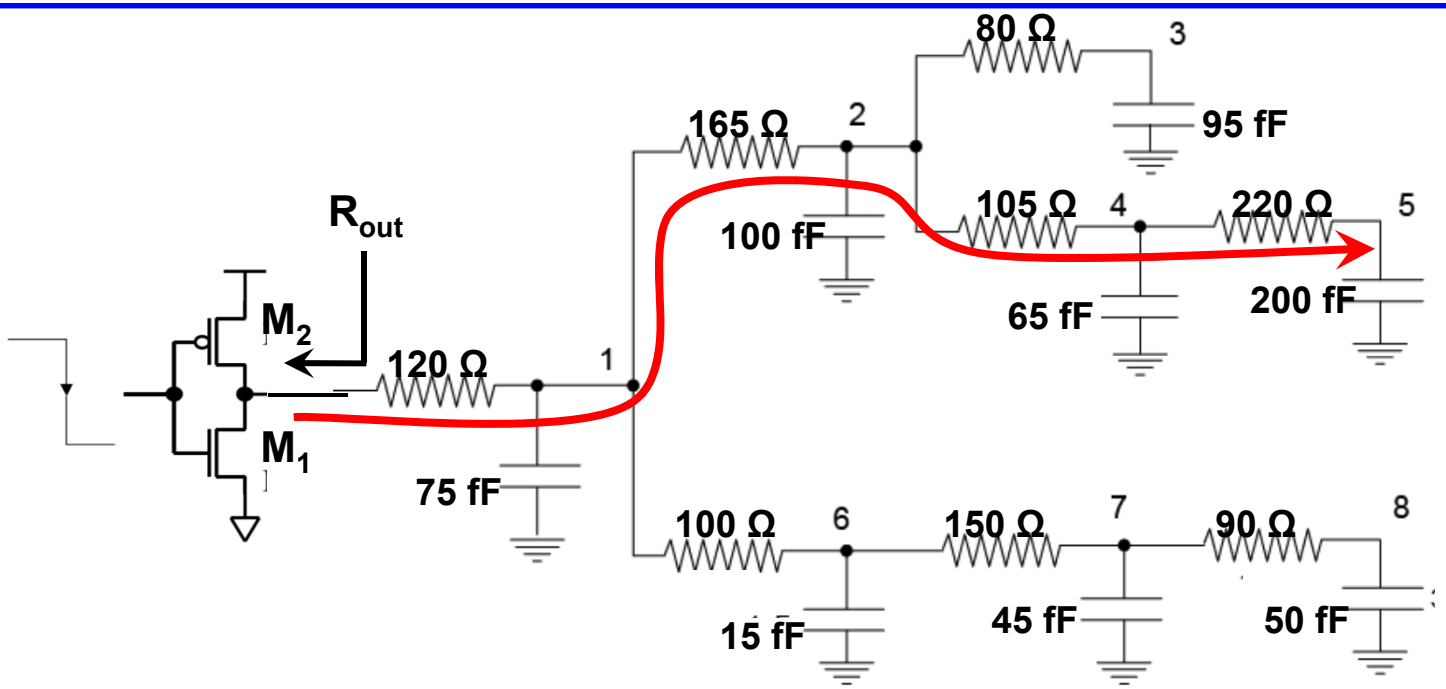
Try this example by yourself. The time constant from Vin to node 8 is 43ns. Therefore, the propagation delay from Vin to node 8 is 30.1 ns

Open Question:



- When an inverter is driving an interconnect, it is better to model the gate as a resistor.
- Based on what you have learned so far, how do you compute the effective output resistance of an inverter?
- Rout is one of the parameters in inverter cell characterization in Electronic Design Automation (EDA) tools.

Homework 15



- Assume that V_{DD}=1.5 V, K'_n=100 uA/V^2, Vt_n=0.4 V, λ_n=0.1 V^{-1}, $(W/L)_n$=10, K'_p=60 uA/V^2, Vt_p=-0.4 V, λ_p=0.2 V^{-1}, $(W/L)_p$=17. Find R_{out}. Hint: connect a load of 100fF to the gate, calculate the LH propagation delay (t_{pLH}) using average current technique, then equate the propagation delay to a simple RC network and find R_{out}. This will effectively be R_{out}(LH).
- Use Elmore technique to compute the time constant and LH propagation delay (t_{PLH}) of the above network from the gate input to node 5.