ECE321 – Electronics I

Lecture 21: Combinational Logic:
NAND & NOR Gate

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Tuesday 2:00-3:00PM or by appointment
E-mail: pzarkesh.unm.edu

Review of Last Lecture

❑ **Layout Techniques**

- **Design for density**
- **Design for performance**
- **Design for reliability**

Today's Lecture

❑ **NAND Gate**

- **Basic circuit for CMOS NAND Gate**
- **Circuit analysis techniques**
- **Proper transistor sizing**

❑ **NOR Gate**

- **Basic circuit for CMOS NOR Gate**
- **Circuit analysis techniques**
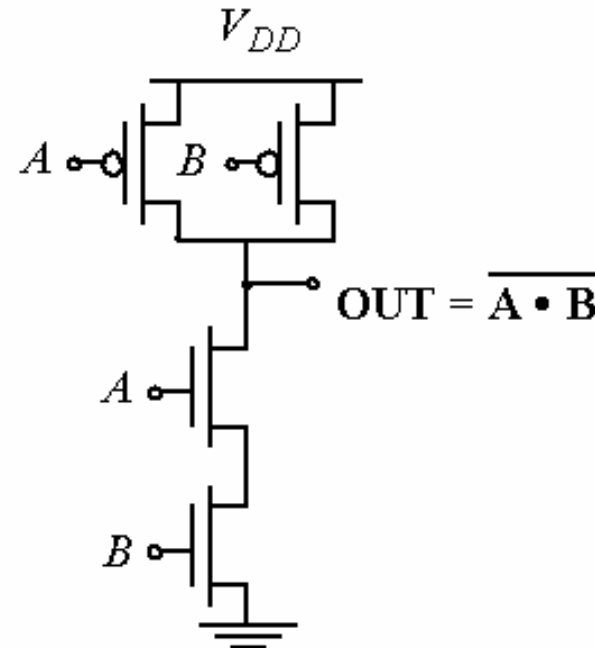- **Proper transistor sizing**

Different Types of Logic Gates

❑ **Besides Inverter and Flip-Flop, the most used logic gates in digital circuits are NAND and NOR gates**
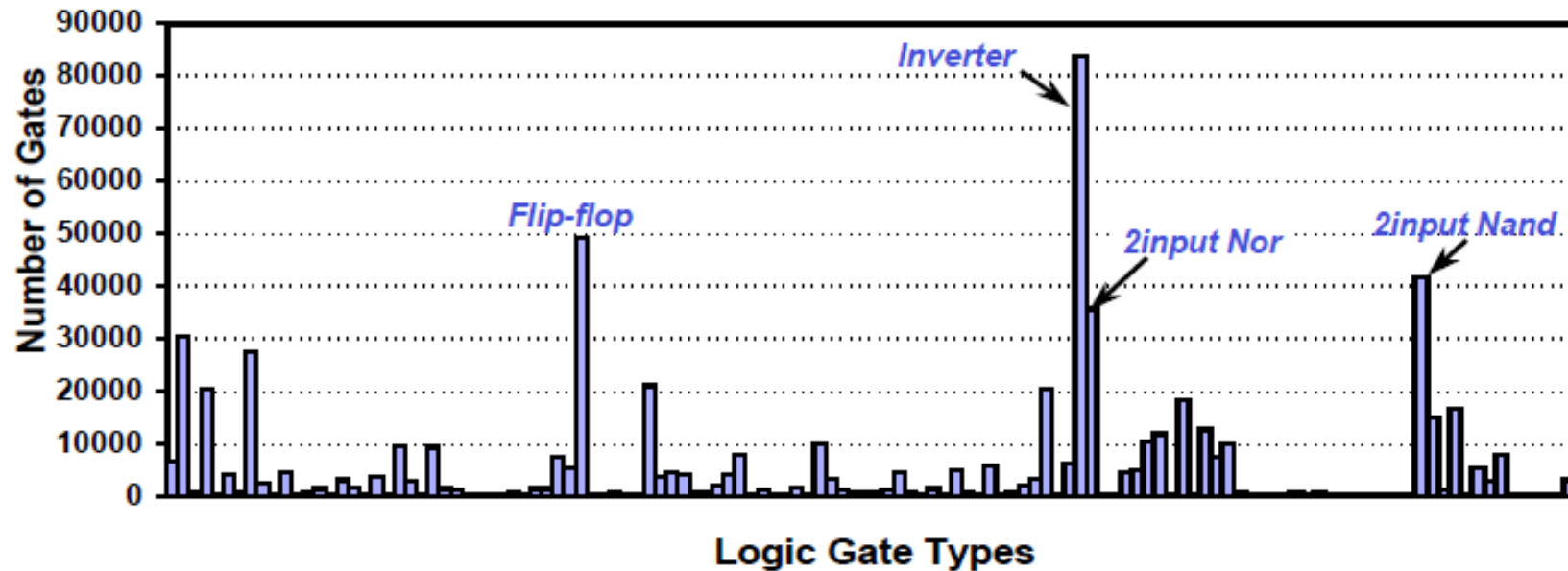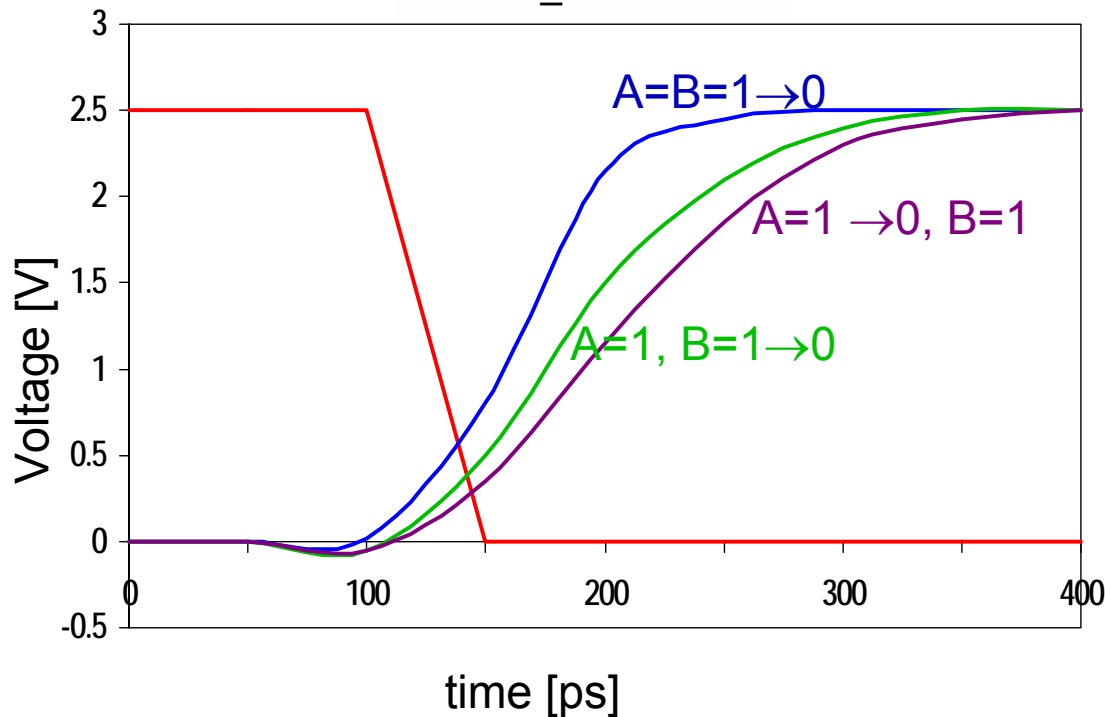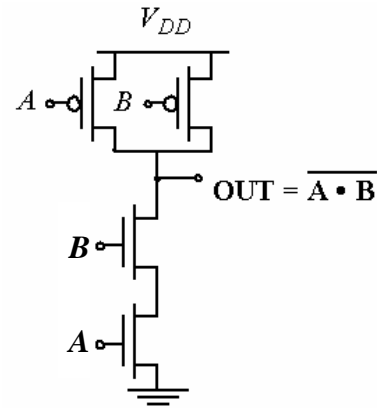
CMOS NAND Gate Structure

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

V_{DD}

$\text{OUT} = \overline{A \cdot B}$

PUN: $\overline{A} + \overline{B} = \overline{AB}$ (Conduction to VDD)

PDN: AB (Conduction to GND)

NAND Gate Dynamic Behavior
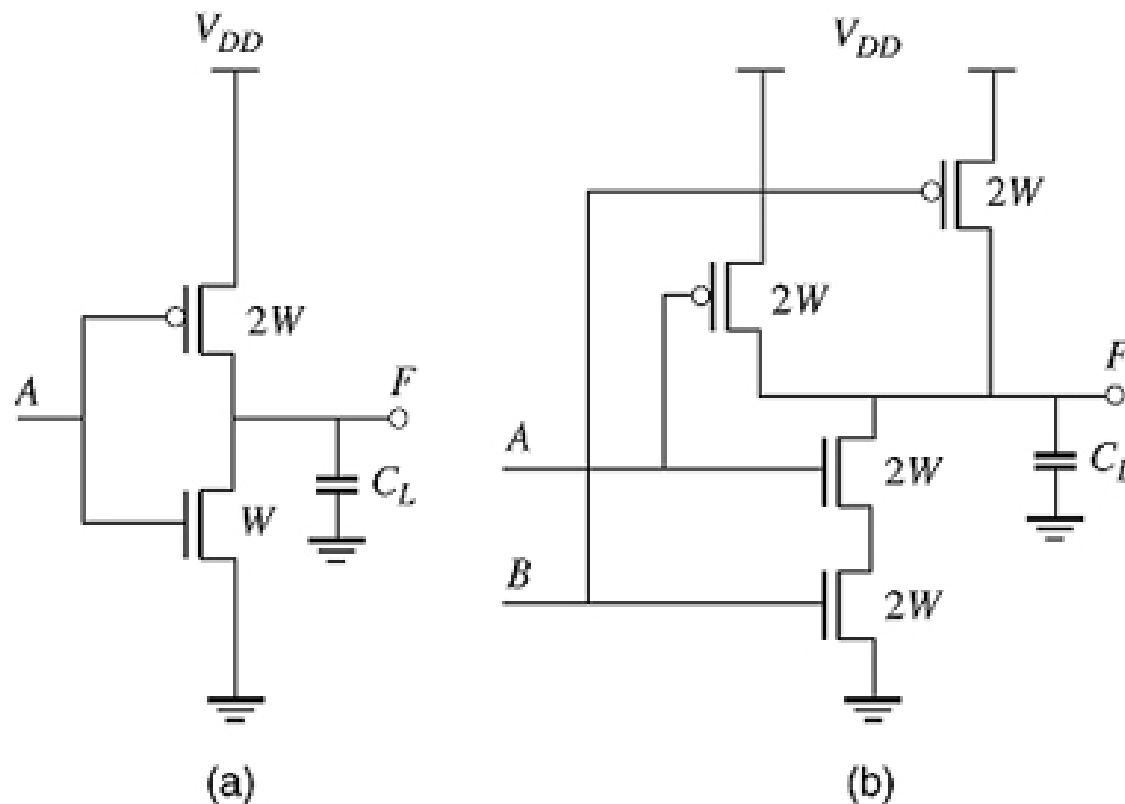

Input Data Pattern	Delay (psec)
A=B=0→1	67
A=1, B=0→1	64
A= 0→1, B=1	61
A=B=1→0	45
A=1, B=1→0	80
A= 1→0, B=1	81

NMOS = 0.5μm/0.25 μm
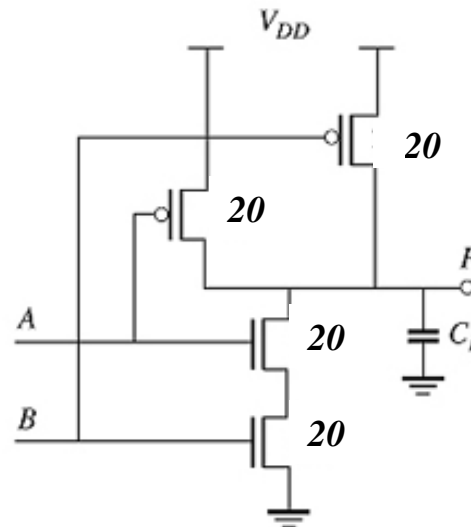PMOS = 0.75μm/0.25 μm
C_L = 100 fF

NAND versus Inverter Equivalency

❑ **Use the series and parallel transistor model to normalize the worst case delay**
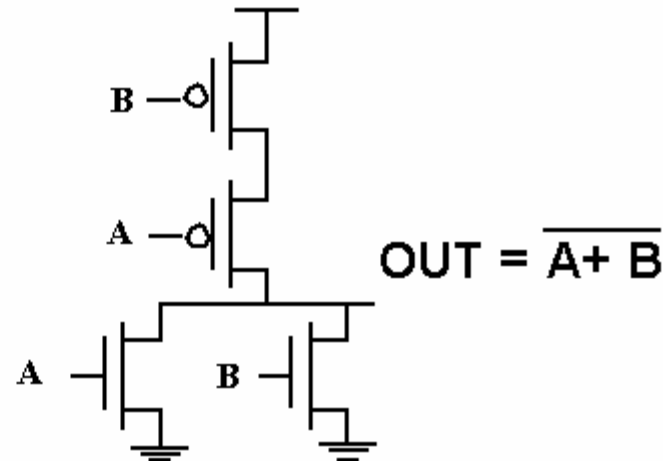

(a)

(b)

Circuit Analysis for NAND Gate

❑ To analyze NAND gate for delay, power, and VTC, use the same concepts you have learned for inverter.

❑ Example: A CMOS NAND gate with V_{DD}=5V is designed such that $(W/L)_n$= $(W/L)_p$=20. Assume that V_{Tn}=0.7, V_{Tp}=-0.6, K'_n=100 uA/V^2, K'_p=-60 uA/V^2, and the load capacitance is 100fF. Use the constant current source model to find:

1) t_{pHL}, when A=B=0→1

2) t_{pLH}, when A=B=1→0

3) t_{pLH}, when A=1 and B=1→0

CMOS NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate
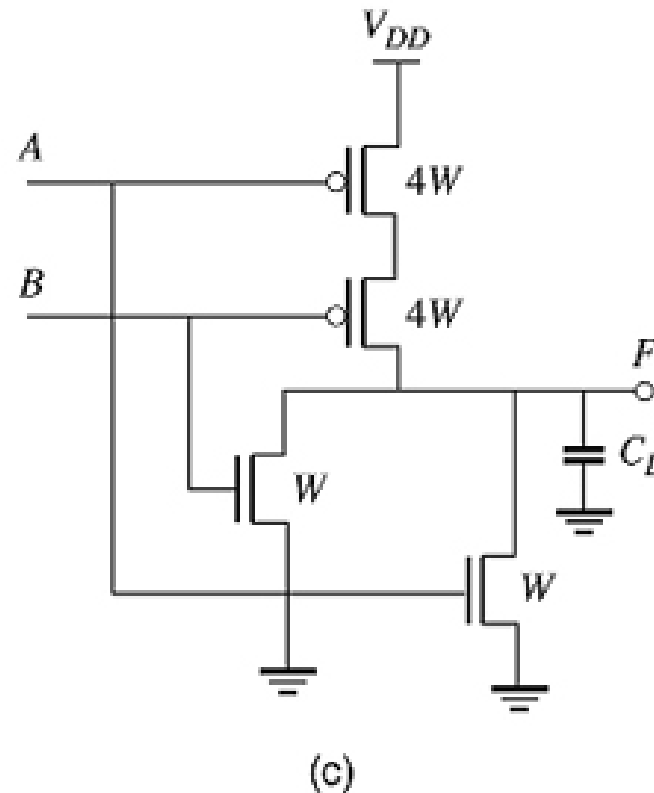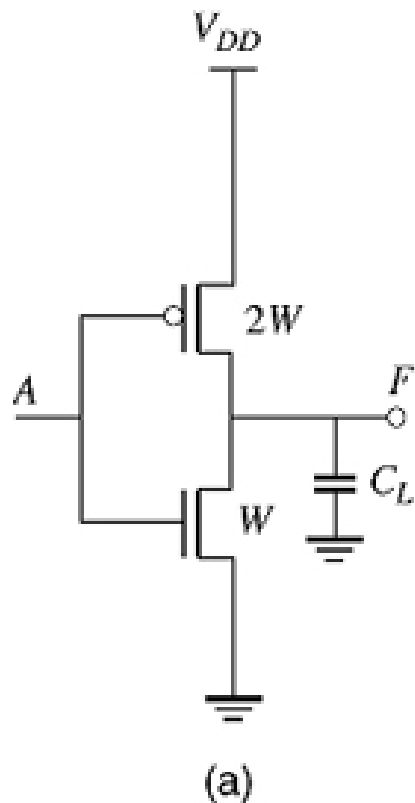
$$OUT = \overline{A+B}$$

PUN: $\overline{A} \cdot \overline{B} = \overline{A+B}$ (Conduction to VDD)

PDN: A+B   (Conduction to GND)

❑ **How do you size transistors to have approximately the same delay as an inverter?**

❑ **Which one is better to use often: NOR or NAND?**

NOR versus Inverter Equivalency

❑ **Use the series and parallel transistor model to normalize the worst case delay**

(a)

(c)

Circuit Analysis for NOR Gate

❑ To analyze NOR gate for delay, power, and VTC, use the same concepts you have learned for inverter.

❑ Example: A CMOS NOR gate with V_{DD}=5V is designed such that $(W/L)_n$= 10 and $(W/L)_p$=40. Assume that V_{Tn}=0.7, V_{Tp}=-0.6, K'_n=100 uA/V^2, and K'_p=-60 uA/V^2.

1) Find the switching threshold voltage, when A and B are tied together

2) Find maximum I_{DD} for this NOR gate

(c)
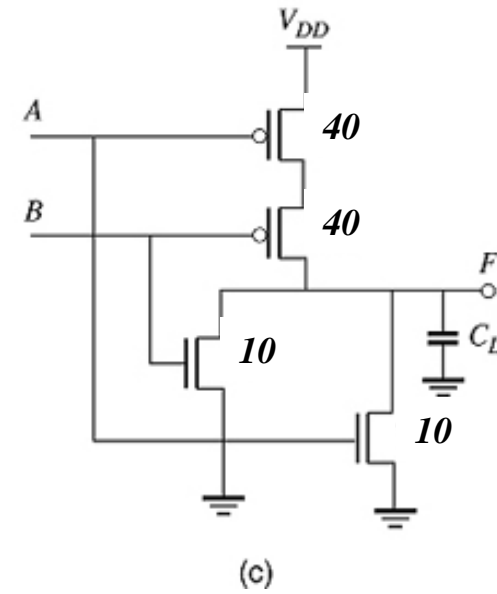
Circuit Configuration

❏ To analyze a logic circuit, you may need to set other inputs (vectors) to be able to pass a transition.

❏ This is the main approach for testing a digital circuit.

❏ Example:

Write the binary sequence for $AB\ CD\ E$ that will

(a) Make $F = f(D)$

(b) Make $F = f(A)$