ECE321 – Electronics I

Lecture 8: MOSFET Threshold Voltage and Parasitic Capacitances

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Review of Last Lecture

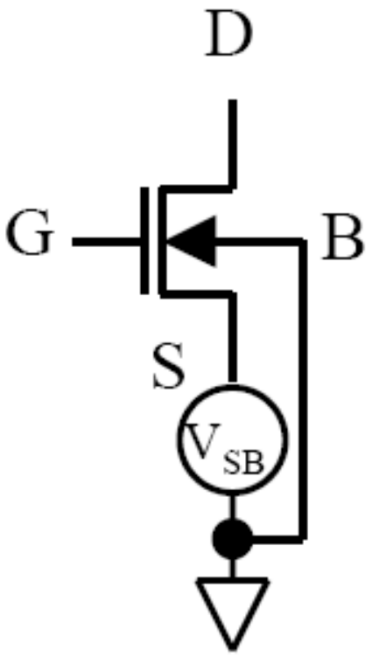
- Device Model for Linear Region
- Device Model for Saturation Region
- Channel Length Modulation

Today's Lecture

- **Threshold Voltage Equation**
- **"Dynamic Parameters of Long Channel MOSFET"**
- **MOSFET Parasitic Capacitances**
  - **Overlap capacitances**
  - **Channel capacitances**
  - **Junction capacitances**

Threshold Voltage Equation

- MOSFET is a four terminal device; Gate, Source, Drain, and Bulk.
- The Bulk may not be always connected to the Source.



Threshold Voltage Equation

- We normally assume that the bulk of the MOSFET is connected to source. However, sometimes the bulk and source are in different potentials ($V_{SB} \neq 0$). V_{SB} is called "body bias".
- The applied V_{SB} changes the threshold voltage as shown below:

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|2\varphi_F + V_{SB}\right|} - \sqrt{\left|2\varphi_F\right|}\right)$$

- In this equation, V_{T0} is the zero bias threshold voltage, γ is the body bias coefficient, and φ_F is:

$$\varphi_F = \frac{KT}{q} Ln\left(\frac{N_A}{n_i}\right)$$

- Where N_A is the doping concentration in the substrate.

Example: Threshold Voltage & Body Bias

- Assume that V_{T0}=0.8V, γ=0.6 $V^{1/2}$, φ_F= 0.4 V. Find V_T if V_{SB}= 2.5 V

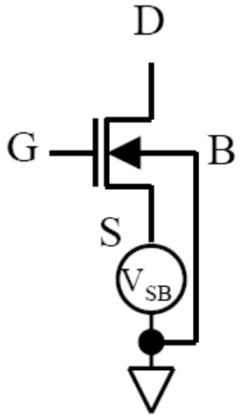
$$V_T = V_{T0} + \gamma\left(\sqrt{\left|2\varphi_F + V_{SB}\right|} - \sqrt{\left|2\varphi_F\right|}\right)$$

$$V_T = 0.8 + 0.6 \times \left(\sqrt{\left|2 \times 0.4 + 2.5\right|} - \sqrt{\left|2 \times 0.4\right|}\right) = 0.8 + 0.55 = 1.35$$

Observations:

1) Body bias is normally reverse bias. (why?)

2) More reverse body bias increases the threshold voltage.



MOSFET Threshold Voltage

- The gate potential at which the channel inverts is called the threshold voltage (V_T)
- V_T is always referenced in relation to the gate to source potential V_{GS} (this is because the surface potential needs to exceed the source to "lure" electrons away into the channel)
- V_T is comprised of four main components:
  - Work function difference between the gate and substrate $\phi_F(\text{substrate}) - \phi_F(\text{gate})$
  - V_{GS} component required to change the surface potential of $2\phi_F$
  - V_{GS} needed to offset the depletion region charge
  - V_{GS} needed to offset charges trapped in the gate oxide

More Detail on MOSFET Threshold Voltage

Zero body bias threshold voltage:

$$V_{T0} = \varphi_{ms} + 2\varphi_F + \frac{\sqrt{2qN_A\varepsilon_{si}|2\varphi_F|}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Where: $\varphi_F = \frac{KT}{q} Ln\left(\frac{N_A}{n_i}\right)$ and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Threshold voltage with body bias:

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}\right)$$

Where: $\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$

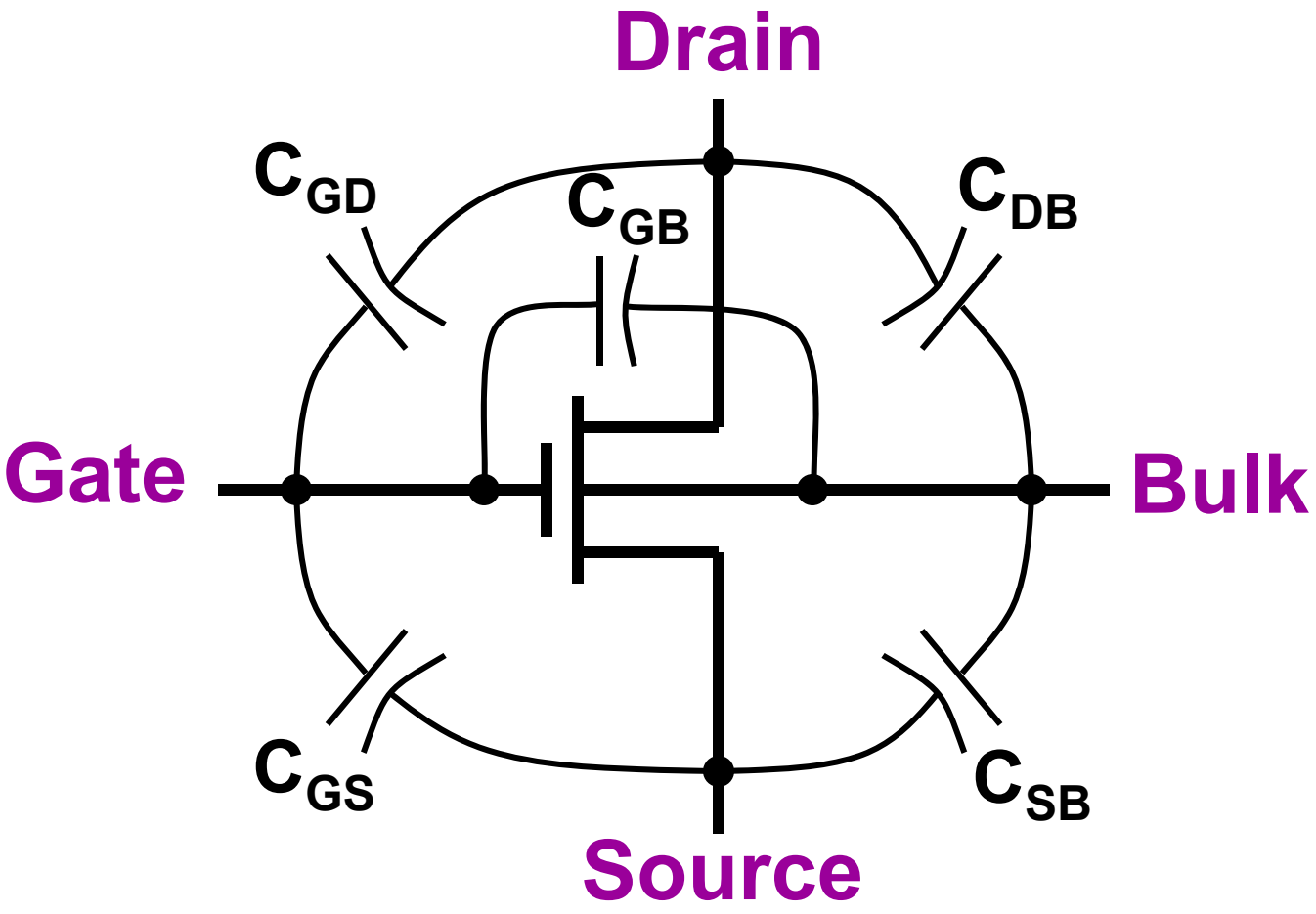
Important Facts:

- Body bias increases threshold voltage
- Threshold voltage is positive for normal NMOS
- Threshold voltage is negative for normal PMOS

MOS Capacitance

- Delay of digital CMOS circuits depends of capacitance of MOS device
- There is a trade off between parasitic capacitance and drive strength of MOS device
  - Larger C_{ox} increases the drive strength (I_{DS} equation)
  - However, larger C_{ox} increases the device parasitic capacitance
- MOS parasitic capacitance includes
  - Overlap capacitances
  - Channel capacitances
  - Junction capacitances
- Between almost every two terminals of MOS device, there is a source of parasitic capacitance

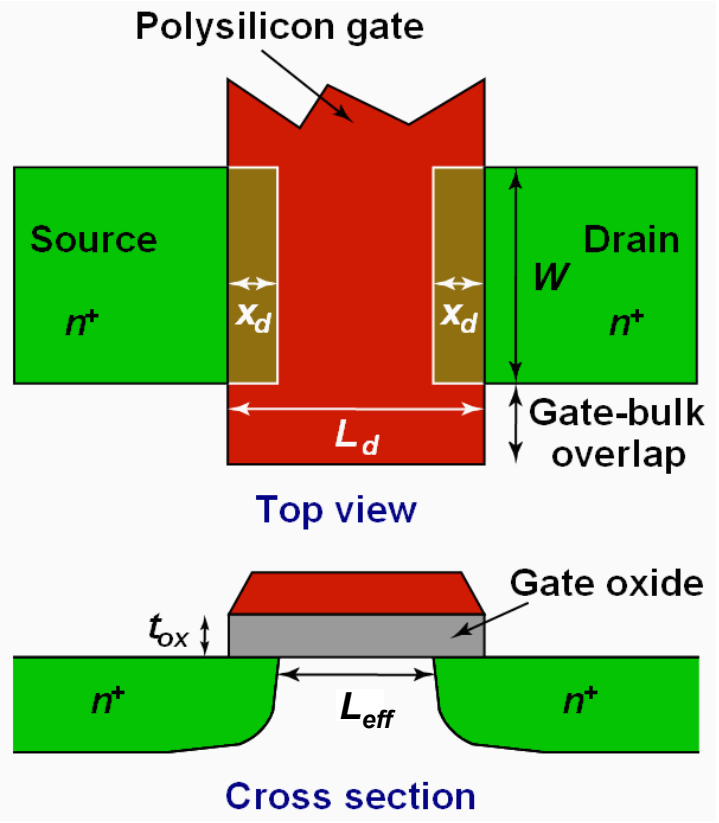
MOS Parasitic Capacitances



Overlap Capacitances

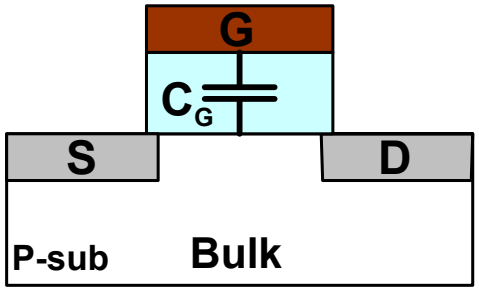
- Because of the lateral S/D diffusion, there is an overlap between gate and S/D junctions
- This overlap capacitance is a constant linear capacitance

$$C_{GSOV} = C_{GDOV} = WC_{ox}X_d$$

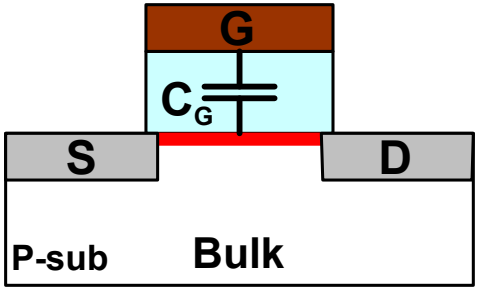


Channel Capacitances

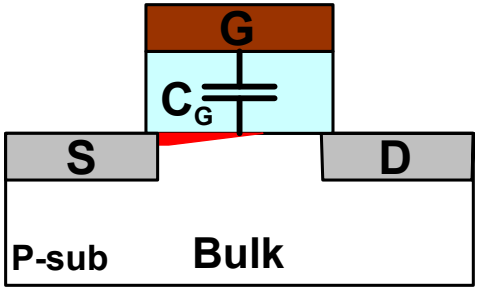
- Channel capacitance is a voltage dependent and non-linear capacitance



Cutoff Region



Linear Region

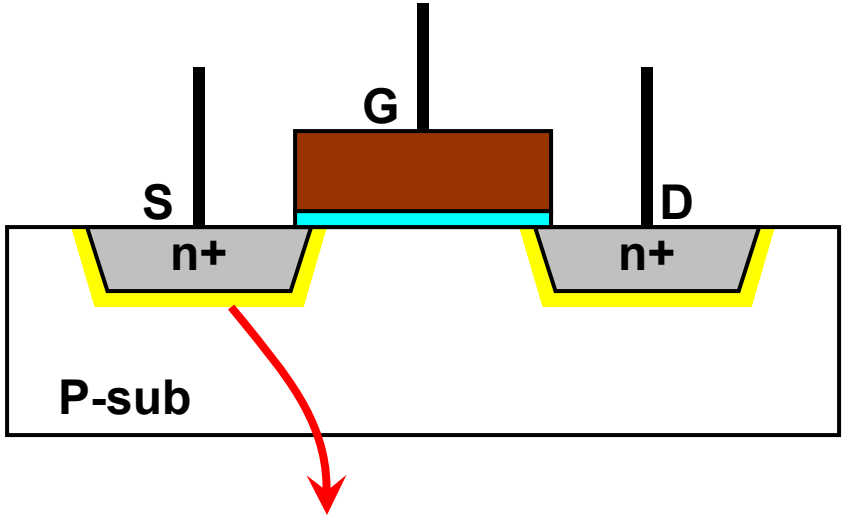


Saturation Region

Operation Region	C_{GBCH}	C_{GSCH}	C_{GDCH}
Cutoff	$C_{OX}WL_{eff}$	0	0
Linear	0	$\frac{1}{2}C_{OX}WL_{eff}$	$\frac{1}{2}C_{OX}WL_{eff}$
Saturation	0	$\frac{2}{3}C_{OX}WL_{eff}$	0

Junction Capacitances

- Junction capacitance is the *depletion region* capacitance of S/D
- It is a voltage dependent capacitance (remember reverse biased diode)

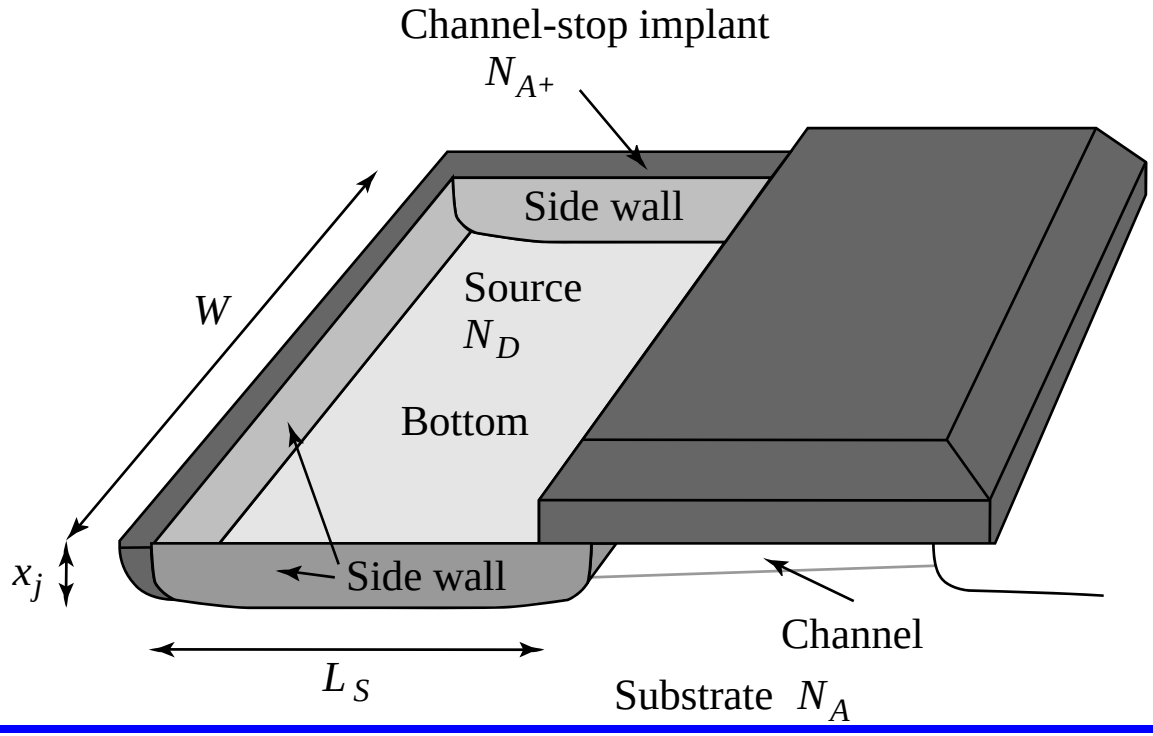


$$C_j = \frac{C_{j0}}{\left(1 - V_{SB}/\varphi_0\right)^m}$$

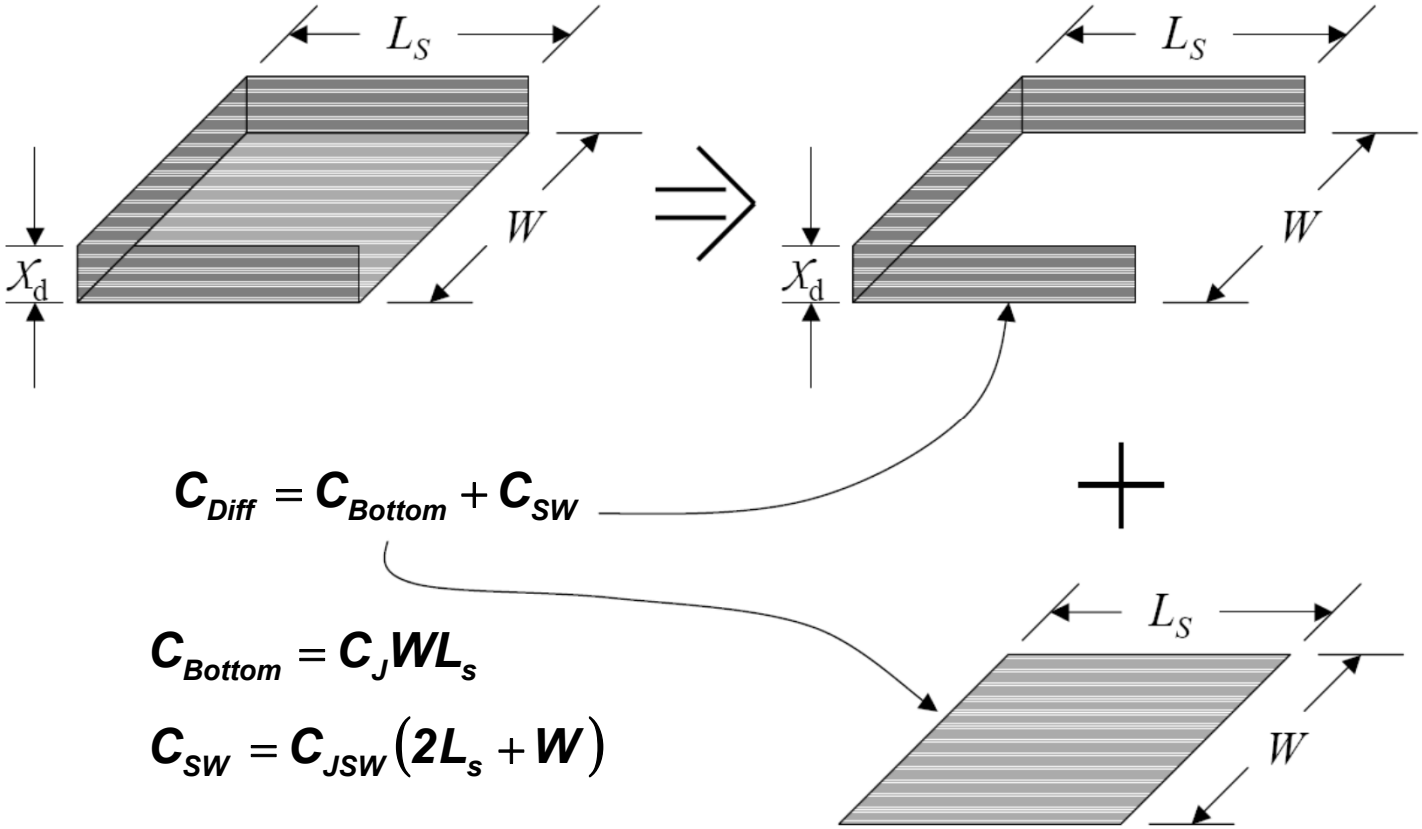
$$C_{j0} = A_D \sqrt{\left(\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}\right) \varphi_0^{-1}} \qquad \varphi_0 = \frac{KT}{q} Ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Junction Capacitance Components

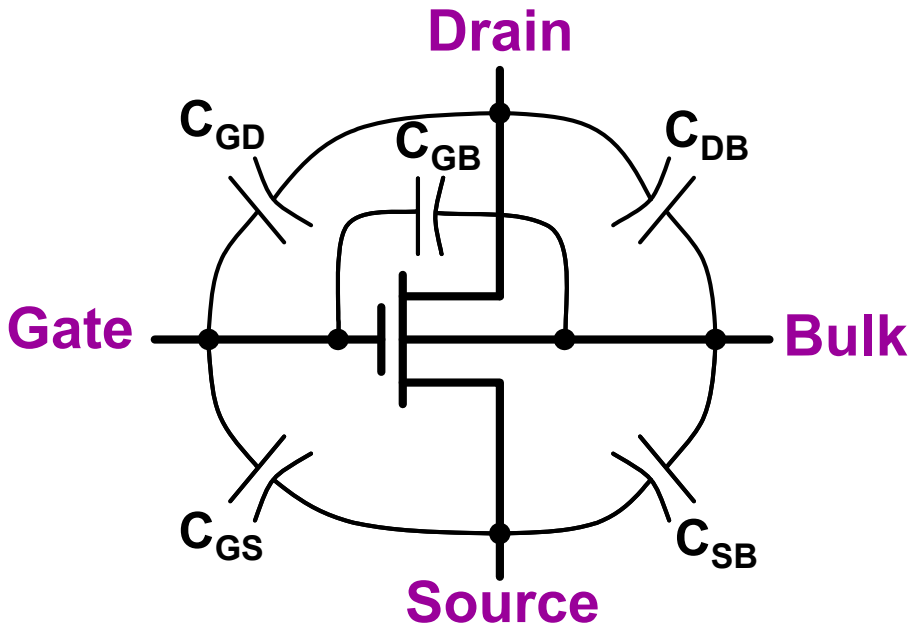
- The Junction capacitance of bottom plate is treated separately from the three non-gate edges
- The gate edge is often ignored since it is part of the conducting channel
- The bottom plate is usually step graded with m=0.5
- The sidewall are step graded with m=0.33 and face the ***channel-stop implant*** which has much higher doping than substrate



Junction Capacitance Components



MOS Parasitic Capacitances



$$C_{GS} = C_{GSCH} + C_{GSOV}$$

$$C_{GD} = C_{GDCH} + C_{GDOV}$$

$$C_{GB} = C_{GBCH}$$

$$C_{SB} = C_{Sdiff}$$

$$C_{DB} = C_{Ddiff}$$