

SCMOS Layout Rule – Well

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9 ¹	18 ²	18
1.3	Minimum spacing between wells at same potential	6 ³	6 ⁴	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0

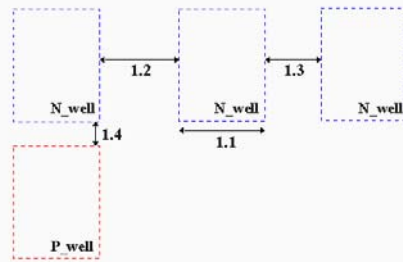
Exceptions for AMIS C30 0.35 micron process:

¹ Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME

² Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM

³ Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME

⁴ Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM

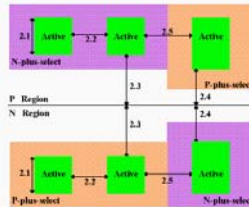


SCMOS Layout Rule – Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3*	3*	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules .	4	4	4

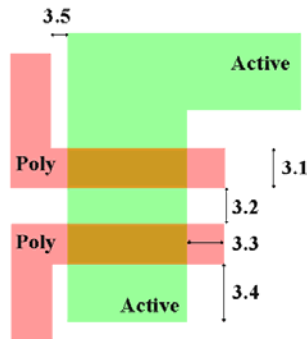
* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

Process	Design Technology	Design Lambda (micrometers)	Minimum Width (lambda)
AMI_ABN	SCNA, SCNE	0.80	5
AML_CSF/N	SCN3M, SCN3ME	0.35	9
AML_CSF/N	SCN3M_SUBM, SCN3ME_SUBM	0.20	10



SCMOS Layout Rule – Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1

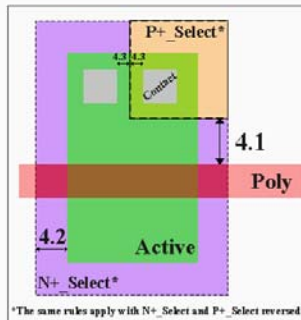


SCMOS Layout Rule – n+ Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must not overlap) (not illustrated)	2	2 ¹	4

Exception for AMIS C30 0.35 micron process:

¹ Use lambda=3 for rule 4.4 only when using SCN4M_SUBM or SCN4ME_SUBM



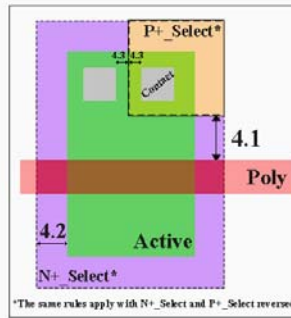
*The same rules apply with N+ Select and P+ Select reversed.

SCMOS Layout Rule – p+ Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must not overlap) (not illustrated)	2	2 ¹	4

Exception for AM16 C90 0.35 micron process:

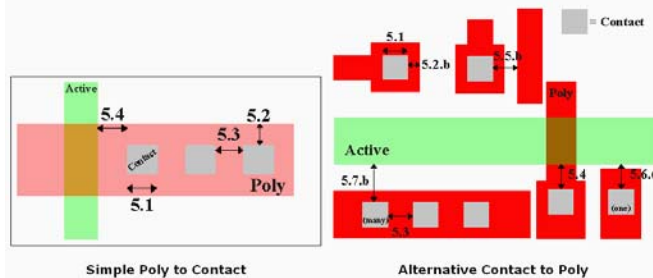
¹ Use lambda=3 for rule 4.4 only when using SCN4M_SUBM or SCN4ME_SUBM



SCMOS Layout Rule – Contact (Poly)

Simple Contact to Poly

Rule	Description	Lambda			Rule	Description	Lambda		
		SCMOS	SUBM	DEEP			SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2	5.2.b	Minimum poly overlap	1	1	1
5.2	Minimum poly overlap	1.5	1.5	1.5	5.5.b	Minimum spacing to other poly	4	5	5
5.3	Minimum contact spacing	2	3	4	5.6.b	Minimum spacing to active (one contact)	2	2	2
5.4	Minimum spacing to gate of transistor	2	2	2	5.7.b	Minimum spacing to active (many contacts)	3	3	3



SCMOS Layout Rule – Contact (Active)

Simple Contact to Active				Alternative Contact to Active					
Rule	Description	Lambda			Rule	Description	Lambda		
		SCMOS	SUBM	DEEP			SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2	6.2.b	Minimum active overlap	1	1	1
6.2	Minimum active overlap	1.5	1.5	1.5	6.5.b	Minimum spacing to diffusion active	5	5	5
6.3	Minimum contact spacing	2	3	4	6.6.b	Minimum spacing to field poly (one contact)	2	2	2
6.4	Minimum spacing to gate of transistor	2	2	2	6.7.b	Minimum spacing to field poly (many contacts)	3	3	3
					6.8.b	Minimum spacing to poly contact	4	4	4

Simple Contact to Active Alternative Contact to Active

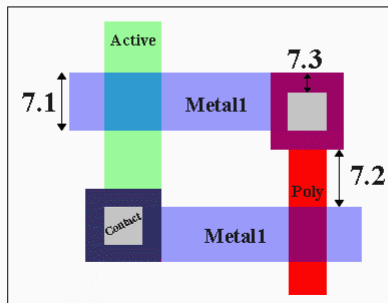
ECE520 – AMI Design Rules

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SCMOS Layout Rule – Metal 1

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
7.1	Minimum width	3	3	3
7.2	Minimum spacing	2	3	3
7.3	Minimum overlap of any contact	1	1	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	4	6	6



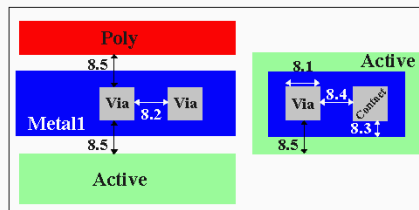
ECE520 – AMI Design Rules

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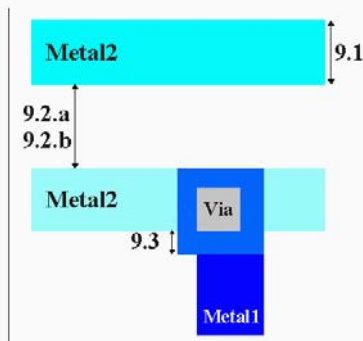
SCMOS Layout Rule – Via 1

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
8.1	Exact size	2 x 2	n/a	n/a	2 x 2	2 x 2	3 x 3
8.2	Minimum via1 spacing	3	n/a	n/a	3	3	3
8.3	Minimum overlap by metal1	1	n/a	n/a	1	1	1
8.4	Minimum spacing to contact for technology codes mapped to processes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3MLC)	2	n/a	n/a	2	2	n/a
8.5	Minimum spacing to poly or active edge for technology codes mapped to processes that do not allow stacked vias (NOTE: list is not same as for 8.4)	2	n/a	n/a	2	2	n/a



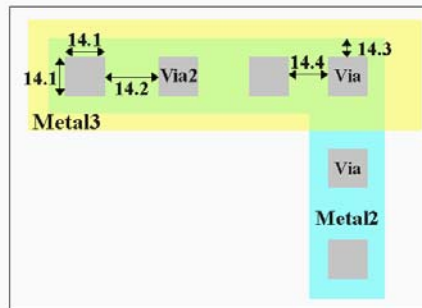
SCMOS Layout Rule – Metal 2

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
9.1	Minimum width	3	n/a	n/a	3	3	3
9.2	Minimum spacing	3	n/a	n/a	3	3	4
9.3	Minimum overlap of via1	1	n/a	n/a	1	1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	n/a	n/a	6	6	8



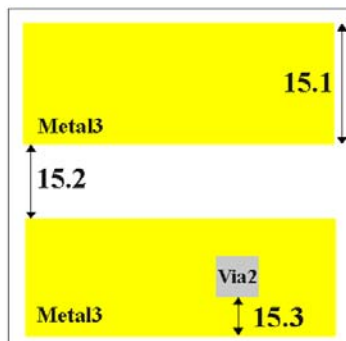
SCMOS Layout Rule – Via 2

Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
14.1	Exact size	2x2	2x2	n/a	2x2	2x2	3x3
14.2	Minimum spacing	3	3	n/a	3	3	3
14.3	Minimum overlap by metal2	1	1	n/a	1	1	1
14.4	Minimum spacing to via1 for technology codes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3ME, SCN3MLC)	2	2	n/a	2	2	n/a
14.5	Via2 may be placed over contact						



SCMOS Layout Rule – Metal 3

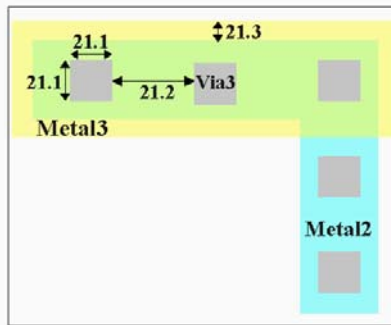
Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
15.1	Minimum width	6	5	n/a	3	3	3
15.2	Minimum spacing to metal3	4	3	n/a	3	3	4
15.3	Minimum overlap of via2	2	2	n/a	1	1	1
15.4	Minimum spacing when either metal line is wider than 10 lambda	8	6	n/a	6	6	8



SCMOS Layout Rule – Via 3

Rule	Description	Lambda					
		4 metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
21.1	Exact size	2x2	2x2	n/a	n/a	2x2	3x3
21.2	Minimum spacing	3	3*	n/a	n/a	3	3
21.3	Minimum overlap by Metal3	1	1	n/a	n/a	1	1

* Exception: Use lambda=4 for rule 21.2 only when using SCN4M_SUBM for Agilent/HP GMOS10QA 0.35 micron process



SCMOS Layout Rule – Metal 4

Rule	Description	Lambda					
		4 Metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
22.1	METAL-4 width	6	6	n/a	n/a	3	3
22.2	METAL-4 space	6	6	n/a	n/a	3	4
22.3	METAL-4 overlap of VIAS	2	2	n/a	n/a	1	1
22.4	Minimum spacing when either metal line is wider than 10 lambda	12	12	n/a	n/a	6	8

