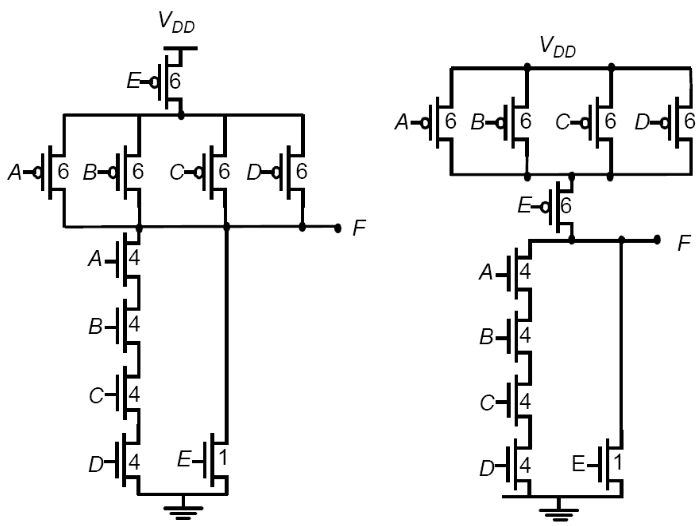
University of New Mexico
Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2026) Homework #10

Bonus Homework – Due on Friday May 8

1. Consider the following two logic circuits.



a. Do these two circuits implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b. Will these two circuits' output resistances always be equal to each other?

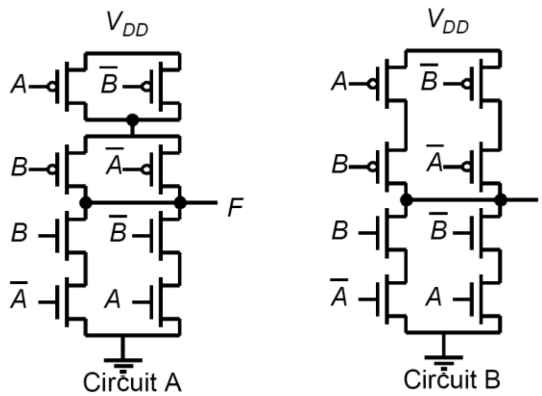
c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?

2. The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13 kΩ for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.

a. What input patterns (A–E) give the lowest output resistance when the output is low? What is the value of that resistance?

b. What input patterns (A–E) give the lowest output resistance when the output is high? What is the value of that resistance?

3. What is the logic function of circuits A and B in the following circuits? Which one is a dual network and which one is not? Is the non-dual network still a valid static logic gate? Explain. List any advantages of one configuration over the other.

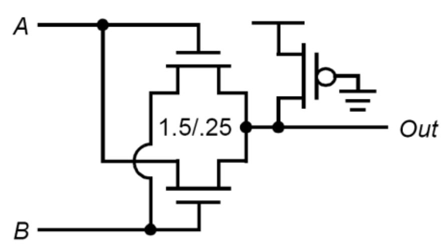


4. The following figure contains a pass-gate logic network.

a. Determine the truth table for the circuit. What logic function does it implement?

b. If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?

c. Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a V_{OL} = 0.3 V. Assume K'_n = 100 μA/V^2 , K'_p = 40 μA/V^2 , V_{Tn} = 0.4, and V_{Tp} = -0.4. Does body effect change your result?



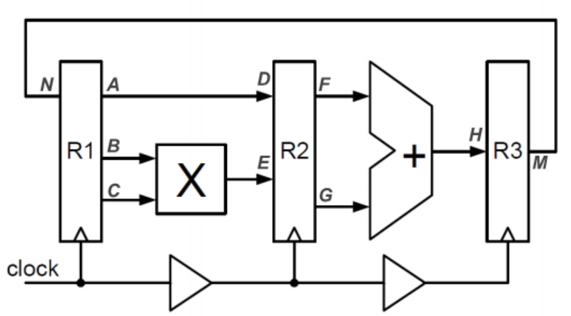
5. Consider the following sequential circuit with 3 edge-triggered registers, a multiplier, and an adder.

(a) Identify all possible paths from the output to the input of any flip -flop in this circuit.

(b) For the delays given in the table below, identify the critical path. Include flip -flop and clock buffer delays and the required flip -flop setup time.

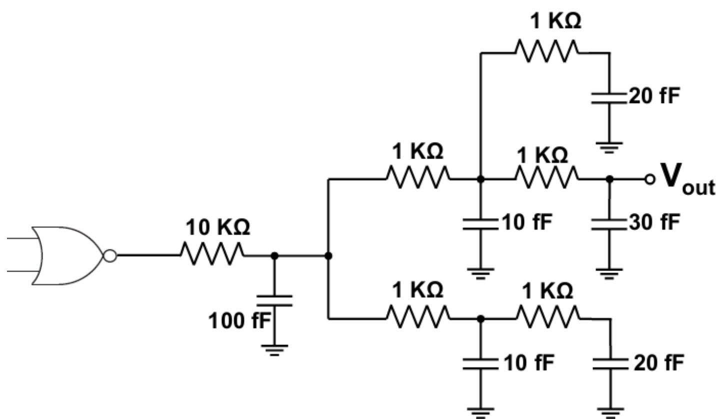
(c) What is the maximum clock frequency at which the circuit can operate correctly?

(d) Does this circuit satisfy the hold time constraint? Why?

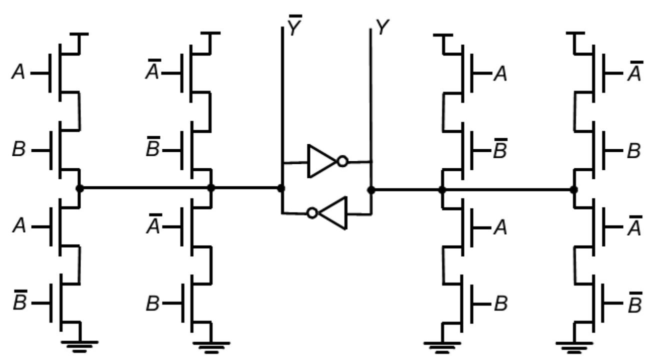


Cell	Delay [ns]
Multiplier (critical path)	40
Multiplier (contamination-delay)	20
Adder (Critical path)	50
Adder (contamination-delay)	10
Flip-Flip (clk-q delay)	20
Flip-Flop (setup time)	10
Flip-Flop (hold-time)	5
Clock Buffer	20

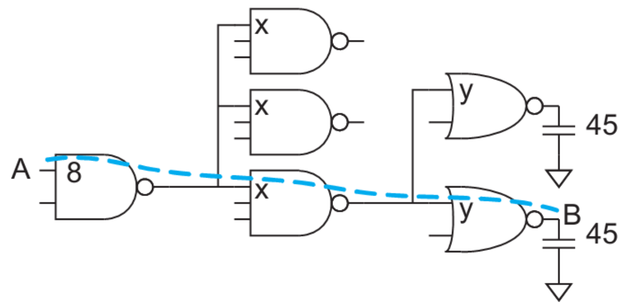
6. We would like to design the following circuit such that the worst case propagation delays (t_{pHL} and t_{pLH}) are limited to 2.14 ns. Use Elmore delay equation to determine the W/L for PMOS and NMOS used in the 2-input NOR gate. Assume that VDD =1.2V, K'n=90uA/V^2, Vtn=0.4V, K'p=50 uA/V^2, and Vtp=-0.5V in the 100nm technology node. Also assume that the transistors stay in saturation region for the length of the transition.



7. Describe the logic function computed by the following circuit. Note that all transistors (except for the middle inverters) are NMOS.



8. Estimate the minimum delay of the path from A to B in Figure below. Choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on the input and the output load is equivalent to 45λ of transistor width.



9. A 3-stage logic path is designed so that the effort by each stage is 12, 6, and 9 delay units, respectively. Can this design be improved? Why? What is the best number of stages for this path? What changes do you recommend to the existing design?

10. Sketch pseudo-nMOS 3-input NAND and NOR gates. Label the transistor widths. What are the rising, falling, and average logical efforts of each gate?

11. Analyze the CMOS ROM circuit below to determine the stored values.