Homework #10
ECE 520 - VLSI Design (Spring 2026)

Ques 1:

a. Yes they do implement same logic function.

$$F = \overline{ABCD + E}$$

b. R_{OL} of both Circuits are Equal But R_{OH} is different.

In Circuit A: Transistor A, B, CD are effected by Body bias
In Circuit B: Transistor E only effected by Body bias.

c. No. They are not equal.

Circuit B: It has lower output Capacitance compared to Circuit A.
So Circuit B is faster Compared to Circuit A.

Ques 2:

a. The lowest output resistance is obtained when all inputs (A-E) are 1.
Both parallel path in NMOS gives equal R so,

$$R_{eq} = \frac{13}{2}\,k\Omega = 6.5\,k\Omega.$$

b. The worst case output Resistance of 13 kΩ is obtained when there are 2 series PMOS. So Each PMOS has

$$R_{PMOS} = \frac{13}{2} = 6.5\,k\Omega.$$

for lowest output resistance during Pull up. all PMOS are with input ZERO.

$$\therefore R_{Eq} = \left(6.5 + \frac{6.5}{4}\right)k = \underline{8.125\,k\Omega}$$

Ques. 3:-

Both Circuits implement XOR function.
Circuit A is dual network - pull up and pull down are dual of each other.

Non-dual Circuit B is still valid static logic as it gives the same logic output for inputs through low resistance path to V_{DD} or Ground.

Circuit B is faster than Circuit A as it can share internal node and the Capacitance is low for Circuit B. Moreover based on switching only one node is ~~connect~~ connected to output in B so it has low Capacitance to discharge & hence faster.

Ques. 4:

a.

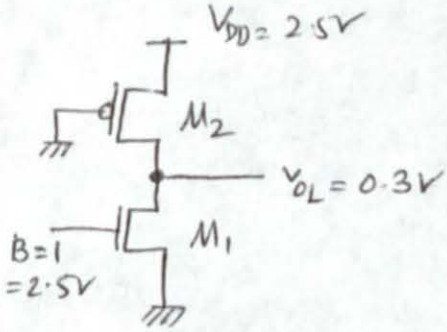
A	B	out
0	0	1
0	1	0
1	0	0
1	1	1

The Circuit implement XNOR

b. No, It will not.

If PMOS is removed, the output node will remain to "0" when A = B = 0 and that node will remain floating. The PMOS device pulls up the output node high during high impedance state.

C.



Assume $A = 0$, $B = 1$

M_1: $V_{ds} < V_{gs} - V_t \Rightarrow$ Linear Region.
(0.3) (2.1)

M_2: $V_{ds} > |V_{gs} - V_t| \Rightarrow$ Saturation.
(2.2) (2.1)

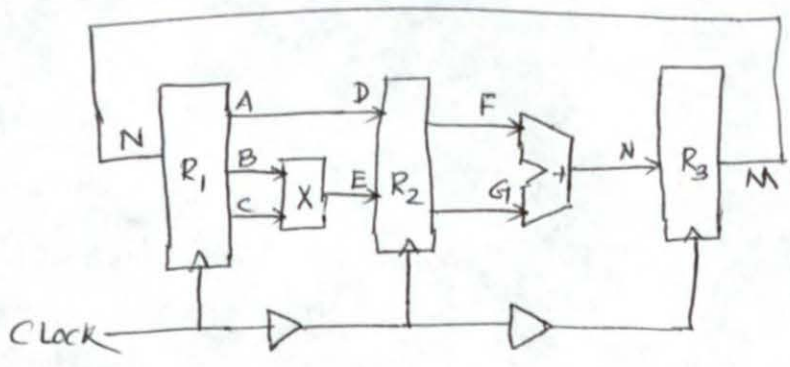
$$I_1 = I_2$$

$$\Rightarrow k_n' \left(\frac{W}{L}\right)_n \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right] = \frac{k_p'}{2} \left(\frac{W}{L}\right)_p (V_{gs} - V_t)^2$$

$$\Rightarrow \left(\frac{W}{L}\right)_p = 3.98 \simeq 4.$$

Body effect doesn't change the result since NMOS source is grounded and PMOS source is connected to V_{DD}.

Ques 5:- a.



Paths:

A → D	F → N
B → E	G_1 → N
C → E	M → N

b.

Path AD: @ setup time: $t_{c-q} + t_{pd} + t_{su} + t_{buffer/skew}$

$= 20 + 0 + 10 + 20 = 50$ ns.

~~@ hold time:~~

Path BE: @ setup time: $t_{c-q} + t_{pd} + t_{su} + t_{Buffer/skew}$

$= 20 + 40 + 10 + 20 = 90$ ns.

Path CE: @ setup time: $t_{c-q} + t_{pd} + t_{su} + t_{Buffer/skew}$

$= 20 + 40 + 10 + 20 = 90$ ns.

Path FH: @ setup time: $t_{c-q} + t_{pd} + t_{su} + t_{Buffer/Skew}$

$= 20 + 50 + 10 + 20 = 100$ ns.

Path GH: @ setup time: $t_{c-q} + t_{pd} + t_{su} + t_{Buffer/Skew}$

$= 20 + 50 + 10 + 20 = 100$ ns.

} Critical path.

and Path MN: @ setup time: $t_{c-q} + t_{pd} + t_{su} + t_{Buffer/Skew}$

$= 20 + 0 + 10 - 40 = -10$ ns.

[∵ due to feedback flow is opposite direction]

Critical path is path FH & GH as they are with the longest delay.

c. Maximum clock frequency is determined by Critical path. delay.

$$f_{max} = \frac{1}{T_{min}} = \frac{1}{100ns} = \underline{10 \text{ MHz}}$$

d. Hold time Constraints —— t_{cd} ⇒ Contamination delay.

$$t_{cd} \geq t_{hold} - t_{c\text{-}q} + t_{skew/Buffer}.$$

For Path AD: (Shorted) @ Hold time.

$$0 \geq 5 - 20 + 20$$

$0 \geq 5$ ⟵ —— false so hold time violation.

Path BE: @ Hold time $20 \geq 5 - 20 + 20$

$\Rightarrow 20 \geq 5$ ⟵ —— TRUE ✓ No violation

Path CE: @ Hold time $20 \geq 5 - 20 + 20$

$\Rightarrow 20 \geq 5$ ⟵ —— TRUE ✓ No violation.

Path FH: @ Hold time $10 \geq 5 - 20 + 20$

$\Rightarrow 10 \geq 5$ ⟵ —— TRUE ✓ No violation.

Path GH: @ Hold time $10 \geq 5 - 20 + 20$

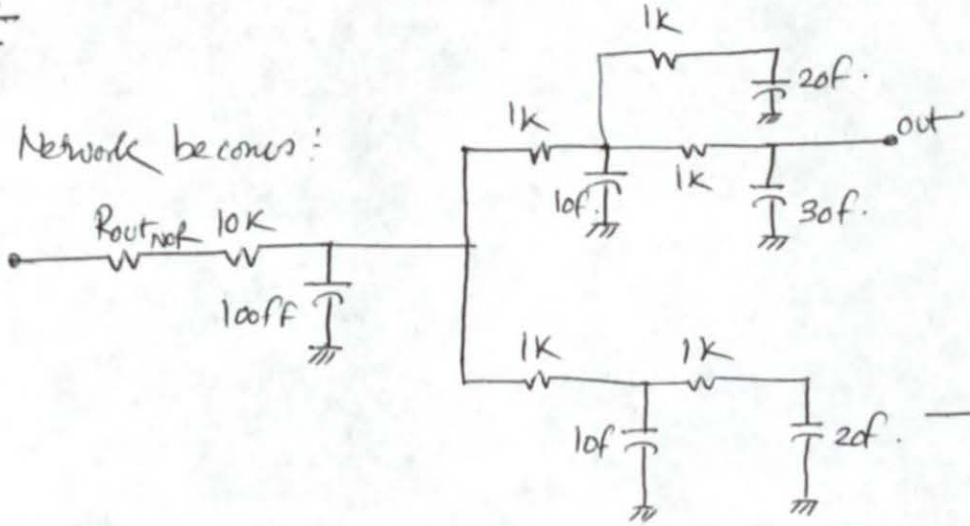
$\Rightarrow 10 \geq 5$ ⟵ —— TRUE ✓ No violation.

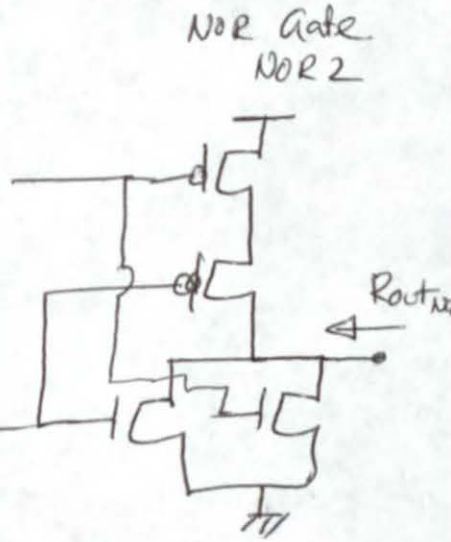
Path MN: @ Hold time $0 \geq 5 - 20 + (-40)$ ⟵ opposite flow of signal. Skew Negative

$\Rightarrow 0 \geq -55$ ⟵ —— TRUE ✓ No violation.

So the Circuit violates hold time Constraints due to Path AD. By inserting a delay path of 5 ns we can overcome the hold violation of the design.

Ques. 6:-





$$t_{PLH} = t_{PHL} = 2.14\,ns = 0.69\left[(R_{out_{NOR}} + 10k)*(100+10+20)*10^{-15} + (R_{out_{NOR}} + 10k + 1k)*(10+20)*10^{-15} + (R_{out_{NOR}} + 10k + 1k + 1k)*(30*10^{-15})\right]$$

$$\Rightarrow R_{out_{NOR}} \equiv 5.85\ k\Omega.$$

For worst case: $R_{NMOS_{NOR}} \equiv 5.85\ k\Omega$ $\qquad R_{PMOS_{NOR}} = \frac{5.85k}{2} = 2.92k\Omega$

$$\therefore R_{NMOS_{NOR}} = 5.85k = \frac{V_{DD}/2}{0.69 * \frac{k_n'}{2}(W/L)_n (V_{DD} - V_{tn})^2}$$

$$\Rightarrow 5.85*1000 = \frac{0.6}{0.69 * 45*10^{-6} *(W/L)_n * (0.8)^2}$$

$$\therefore (W/L)_n = 5.161 \approx 6$$

$$R_{PMOS_{NOR}} = 2.92k = \frac{V_{DD}/2}{0.69 * \frac{k_p'}{2} * (W/L)_p * (V_{DD} - |V_{tp}|)^2}$$

$$\Rightarrow 2920 = \frac{0.6}{0.69 * 25*10^{-6} * (W/L)_p * (0.7)^2}$$

$$\therefore (W/L)_p = 24.31 \approx 25$$

Ques 7:

$$Y = \overline{\bar{A}\bar{B} + AB}$$

$$\bar{Y} = \overline{\bar{A}B + A\bar{B}}$$

$$\Rightarrow Y = \bar{A}B + A\bar{B}$$

$$= \overline{\bar{A}\bar{B}} \cdot \overline{A\bar{B}}$$

$$= (\bar{\bar{A}} + \bar{\bar{B}}) \cdot (\bar{A} + \bar{B})$$

$$= (A + B)(\bar{A} + \bar{B})$$

$$= A\bar{A} + \bar{A}B + B\bar{B} + A\bar{B}$$

$$= \bar{A}B + A\bar{B} \qquad [\because B\bar{B} = A\bar{A} = 0]$$

∴ Logic function is a Differential XOR gate. $Y = A \oplus B$

Ques 8:-

Here, Logical effort, $G = (4/3) * (5/3) * (5/3) = 100/27$

Electrical effort, $H = \frac{45}{8}$

Branching effort, $B = 3 * 2 = 6.$

∴ Path effort, $F = G \cdot B \cdot H = \frac{100}{27} * \frac{45}{8} * 6 = 125$

∴ Best stage effort, $f = (F)^{1/3} = 5$

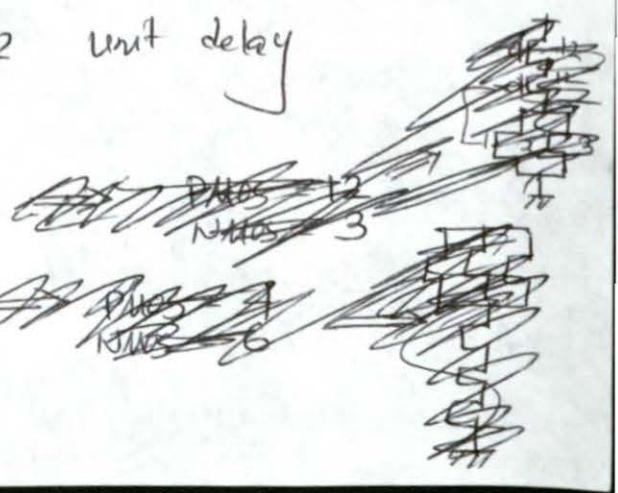
Parasitic delay, $P = 2+3+2 = 7.$

∴ Delay, $D = 3 * 5 + 7 = 22$ unit delay

Sizing :- $y = (45 * \frac{5}{3})/5 = 15$ Ω

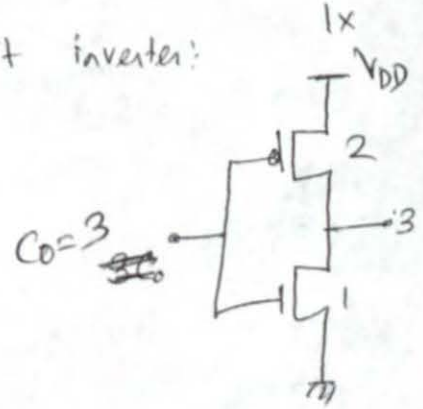
$x = ((15 * 2) * \frac{5}{3})/5 = 10$ Ω

First stage : 8 Ω

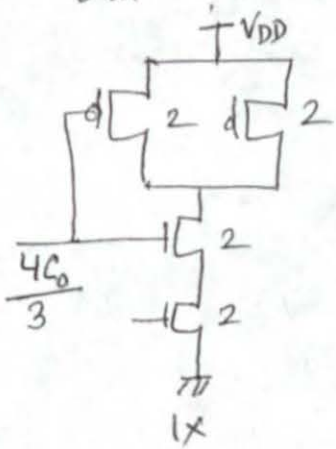


8)

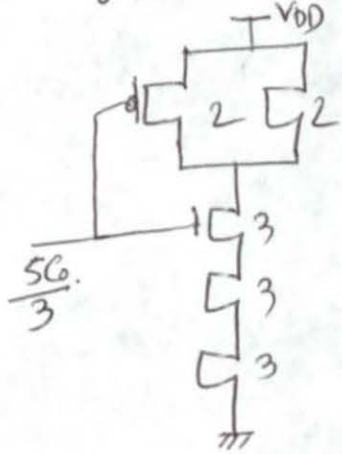
Unit inverter:



Unit NAND2 : (1x)



Unit NAND3 : (1x)

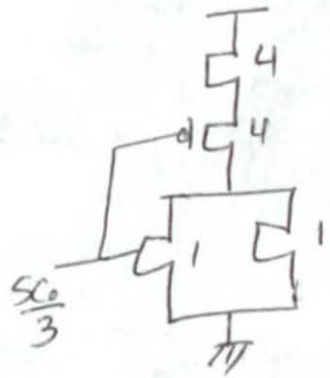


So, NAND 2 Sizing :- $\frac{8C_0}{\frac{4C_0}{3}} = 6X$

NAND 3 Sizing : $\frac{10C_0}{\frac{5C_0}{3}} = 6X$

and NOR 2 Sizing : $\frac{15C_0}{\frac{5C_0}{3}} = 9X$

Unit NOR 2 :



QUES. 9:- # YES, It Can be improved as $f_1 \neq f_2 \neq f_3$

For optimum design $f_1 = f_2 = f_3$

Here $F = f_1 * f_2 * f_3 = 648$

∴ Optimum / Best number of stage $\Rightarrow n = \ln(F)$

$= \ln(648)$

$\cong 6.4$

If 6 stage, $f = (648)^{1/6} = 2.94$

delay $\cong 2.94 * 6 \cong 17.65$ unit.

If 7 stage, $f = (648)^{1/7} = 2.52$

delay $\equiv 2.52 * 7 = 17.65$ unit.

So, 6 stage is best

Logic Restructuring to 6 stage.

Ques. 10 :-

ADDRESS.		Active Line.	output. MSB					LSB
A_1	A_0		Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	L_0	0	1	0	1	0	1
0	1	L_1	0	1	1	0	0	1
1	0	L_2	1	0	0	1	0	1
1	1	L_3	1	0	1	0	1	0