

#1

$$\text{Yield} = \frac{\# \text{ of good chips per wafer}}{\text{Total \# of chips per wafer}}$$

$$(I) \text{ Wastage \%} = [1 - \text{Yield}] \times 100 \%$$

$$= \left[1 - \left[\frac{\text{die per wafer} \times \text{die area}}{\text{area of the wafer}} \right] \right] \times 100 \%$$

$$(1) \text{ die per wafer} = \frac{\pi \times \left(\frac{\text{wafer diameter}}{2} \right)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

$$(2) \text{ die area} = (\text{die size})^2$$

$$(3) \text{ area of the wafer} = \pi \left(\frac{\text{wafer diameter}}{2} \right)^2$$

⇒ Plug eq 1, 2 & 3 in (I) to solve for wastage area as a function of die size.

★ See Matlab code / Results

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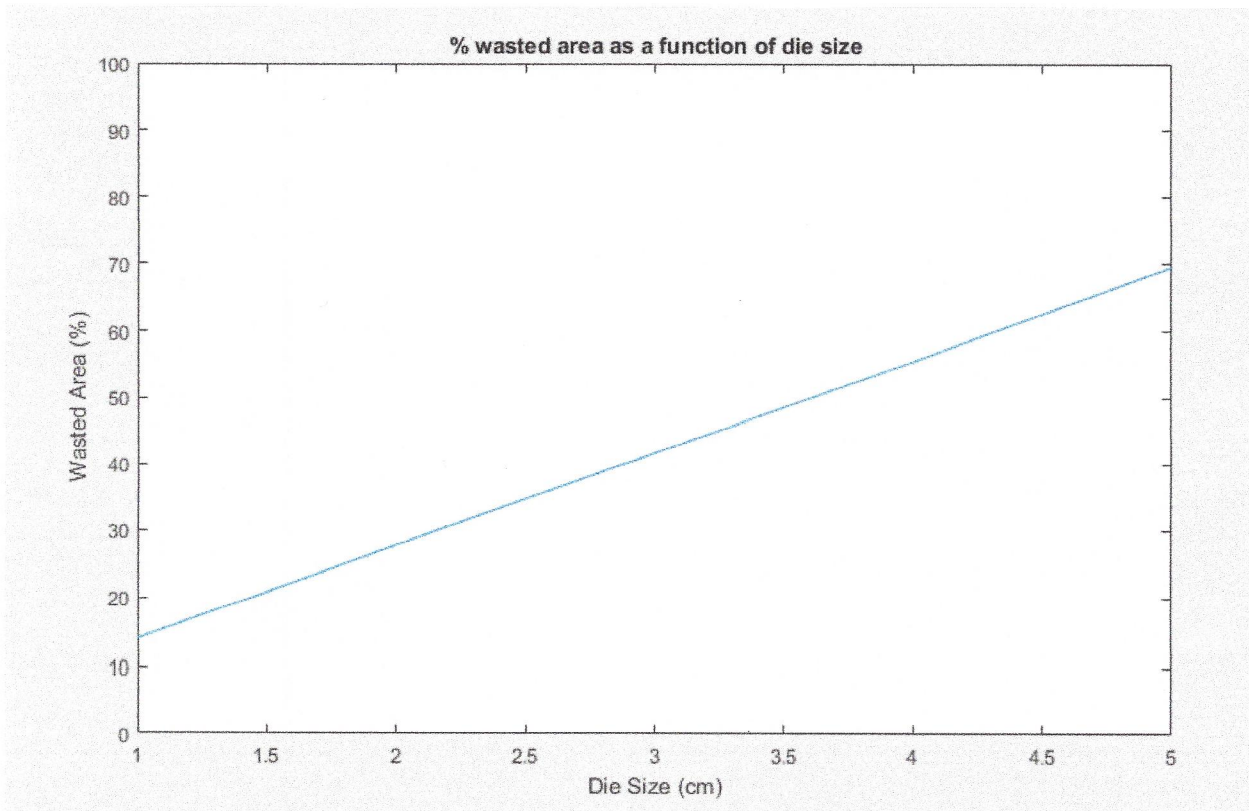
clear all;
close all;
clc;
syms ds wd dpw pw

ds = 1:0.1:5 ; % die size from 1 to 5 cm
wd = 20.32; % wafer diameter 8 in = 20.32 cm
dA = ds.^2; % die area
wA = pi*(wd/2)^2 ; % wafer area

dpw = wA./(dA - (pi*wd)./(sqrt(2*dA))); % die per wafer
pw = (1-(dpw.*dA)/wA) * 100; % percent of wasted area

figure; plot(ds,pw) % plot die size vs percent of wasted area
title('% wasted area as a function of die size'), xlabel('Die Size (cm)'), ylabel('Wasted Area (%)')
axis([1 5 0 100])

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#2

- Show how $I_D = \frac{k'n}{2} \frac{W}{L} (V_{GS} - V_T)^2$ becomes

$I_D = I_D' (1 + \lambda V_{DS})$ when channel length modulation is included. Assume $\frac{\Delta L}{L} = \lambda V_{DS}$

⇒ Channel length modulation reduced length

$$L = L - \Delta L$$

$$\text{So, } I_D = \frac{k'n}{2} \left(\frac{W}{L - \Delta L} \right) (V_{GS} - V_T)^2$$

$$= \frac{k'n}{2} \left[\frac{W}{L \left(1 - \frac{\Delta L}{L} \right)} \right] (V_{GS} - V_T)^2$$

$$\Downarrow \approx \frac{W}{L} \left(1 + \frac{\Delta L}{L} \right)$$

$$= \frac{k'n}{2} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \left(1 + \frac{\Delta L}{L} \right)$$

↑ sub-in the given assumption

$$I_D = \frac{k'n}{2} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$\Rightarrow I_D = I_D' (1 + \lambda V_{DS})$$