University of New Mexico

Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2026) Homework #2

Due in class: Thursday Feb. 5, 2026

1. An NMOS transistor has a threshold V_T of 0.5 V when its source-to-substrate voltage is zero, given that the substrate is uniformly doped at 2E17 acceptor dopant atm/cm^3 and the gate oxide capacitance is 3.5 fF/μm^2.

a. Determine an expression for the threshold voltage as a function of source-to-substrate voltage.

b. It is desired to obtain a threshold voltage of 1.0 volt at 0 volts source potential (with respect to ground). One method suggested by engineering team is to provide a separate bias supply for the substrate, in order to increase the source-to-substrate voltage. What value of Vx supply is needed?

c. Rather than use of a separate substrate bias generator, another group in engineering is suggesting to use a threshold adjustment implant is the fabrication. Assuming the implant acts as a sheet charge in the oxide-silicon interface (via the term Q_{fc}), what dose is needed to obtain V_{TN}=1 volt at V_{SB}=0? Would you use acceptor (N_A) or donor (N_D) atoms?