

**ECE 520 - VLSI Design (spring 2026)**

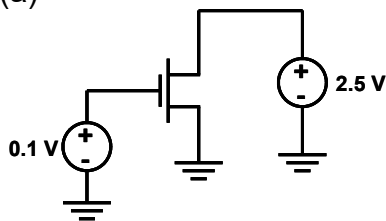
**Homework #3**

*Due in class: Thursday Feb. 12, 2026*

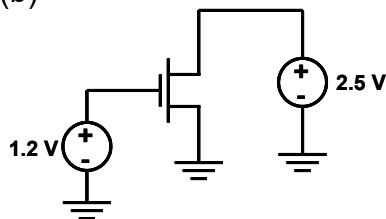
1. In each circuit configuration below:
- 1) Identify Drain and Source terminals assuming the device is an NMOS
  - 2) Identify operating region of each transistor (cutoff, linear, saturation, or velocity saturation)
  - 3) Determine the drain current

Assume  $V_{DSat} = 1\text{ V}$ ,  $V_{Tn} = 0.5\text{ V}$ , and  $K'_n(W/L) = 1\text{ mA/V}^2$ . Ignore the body effect.

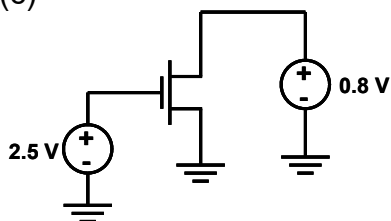
(a)



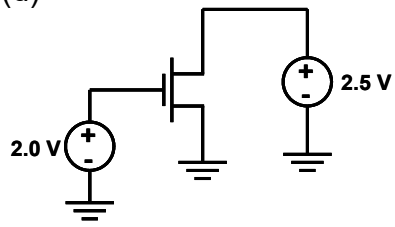
(b)



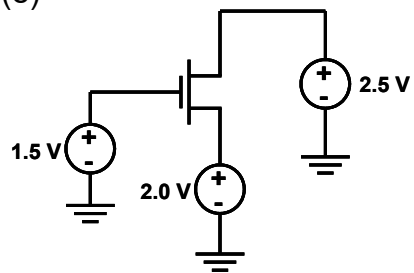
(c)



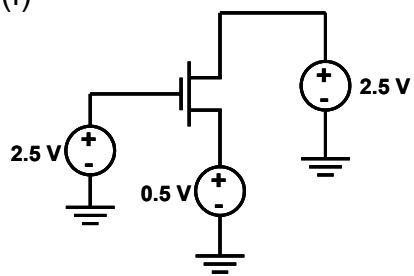
(d)



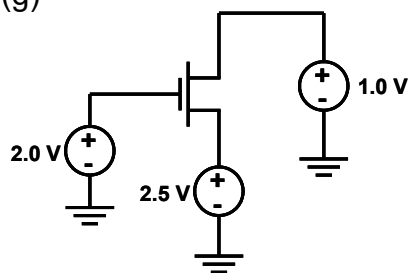
(e)



(f)



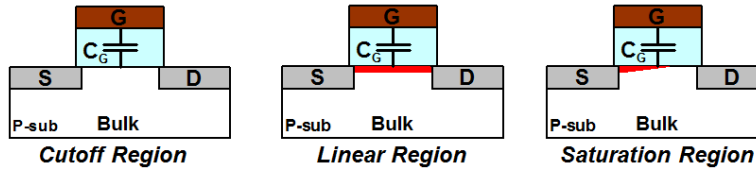
(g)



2. We discussed in class how the channel capacitance can be modeled in different region of operations in MOSFETs. For your reference, the slide is shown below. Explain how you think the model would look like if a transistor is in velocity saturation region?

## Channel Capacitances

- Channel capacitance is a voltage dependent and non-linear capacitance



Operation Region	$C_{GBCH}$	$C_{GSCH}$	$C_{GDCH}$
Cutoff	$C_{OX}WL_{eff}$	0	0
Linear	0	$\frac{1}{2}C_{OX}WL_{eff}$	$\frac{1}{2}C_{OX}WL_{eff}$
Saturation	0	$\frac{2}{3}C_{OX}WL_{eff}$	0