University of New Mexico

Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2026) Homework #7

Due in class: Tuesday March 24, 2026

1. The following is the layout of an inverter with dimensions. Assume that V_{DD}=2.5V, K'_n=100uA/V^2, V_{tn}=0.4V, K'_p=60uA/V^2, V_{tp}=-0.5V, t_{ox}=12nm, ε_{ox}=3.9, X_d=42nm (overlap distance under the gate), C_j=0.74fF/um^2, C_{jsw}=0.43fF/um for both NMOS and PMOS devices at zero bias.

a. Estimate the effective input capacitance of the inverter, C_{in}.

b. Estimate the effective output capacitance of the inverter, C_{out}. For simplicity find effective C_{out} at zero bias.

c. If the output of this inverter is connected to a similar inverter, estimate the t_{pHL} and t_{pLH}. Ignore the wire parasitic capacitance.