ECE520 – VLSI Design

Lecture 10: L-Edit Demo and Layout Techniques

Prof. Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

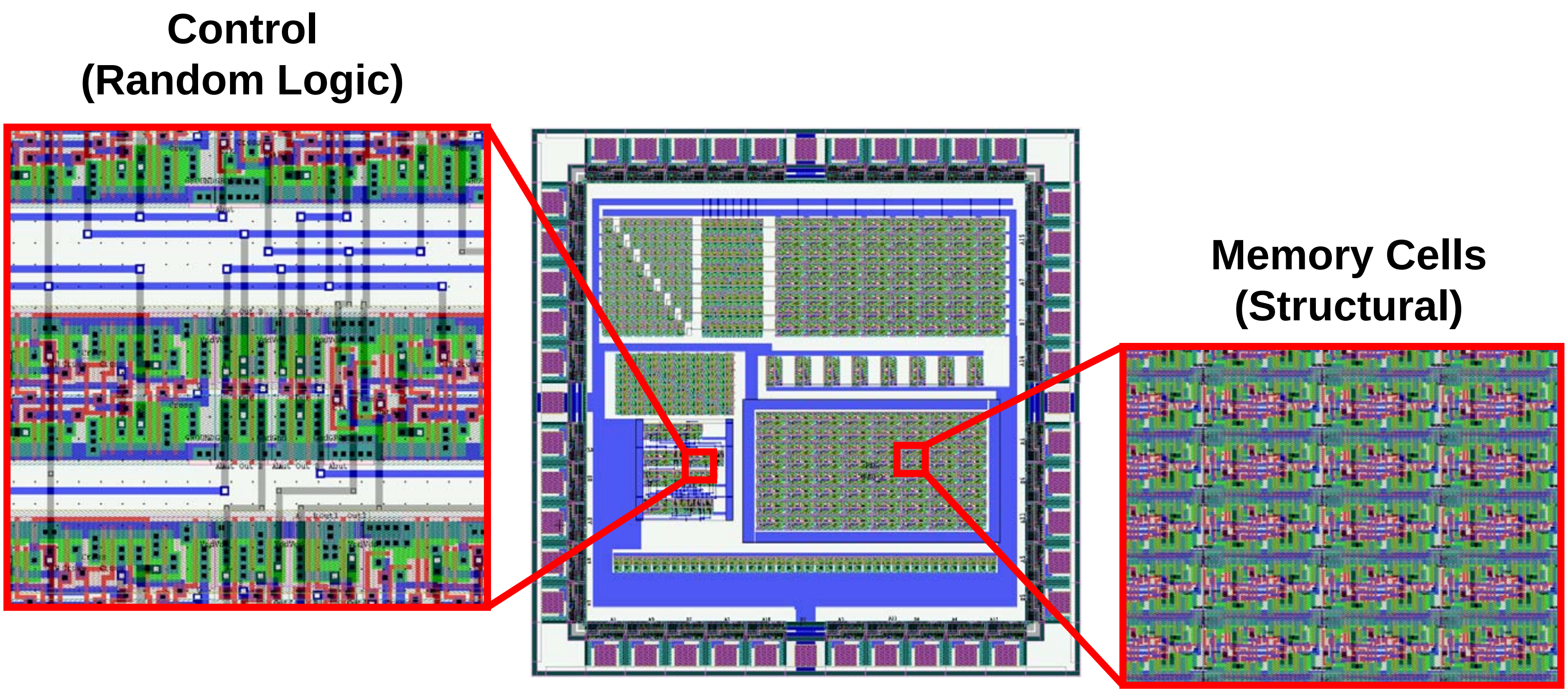
Review of Last Lecture

- **Overview of Design Rules**
  - **What are design rules?**
  - **Why have design rules?**
  - **Typical design rules**

Today's Lecture

- **L-Edit Demo**
- **Layout Techniques**
  - **Design for density**
  - **Design for performance**
  - **Design for reliability**

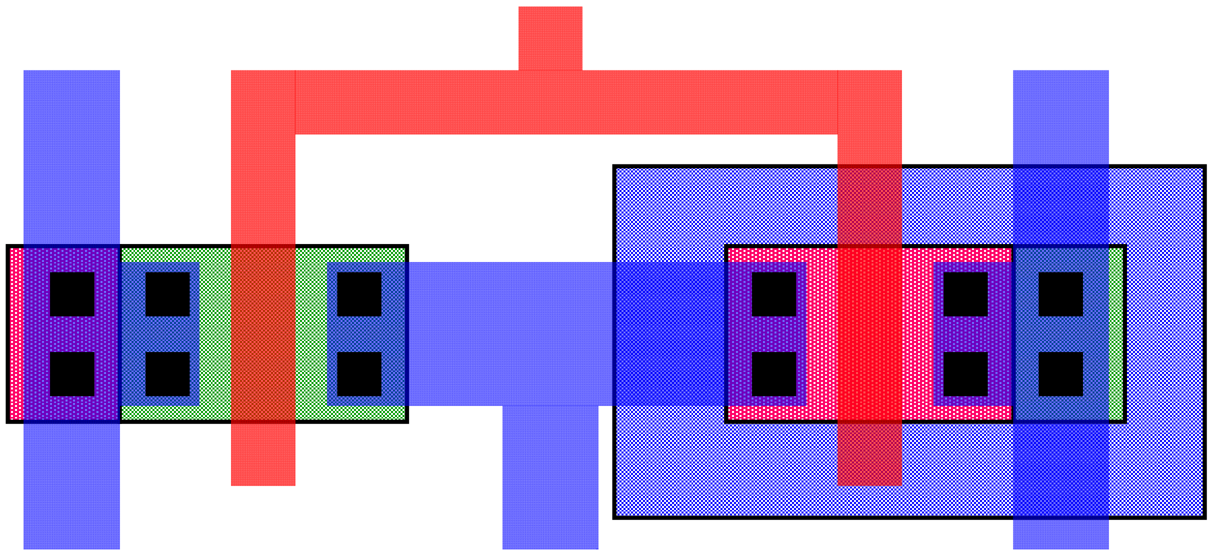
An Example of Layout



Good Layout Characteristics

- **Density**
  - **Cells pack together well**
  - **Cells are routable—think about how they will fit together before starting!**
  - **Start with paper diagram first**
- **Performance**
  - **Keep capacitances low (specially diffusion cap)**
  - **Keep interconnects short**
- **Reliability**
  - **Poor layout can greatly affect the circuit reliability**
  - **Use proper wire width for power rails (IR drop, electromigration)**
- **Final Checks**
  - **Layout must match the circuit being built (LVS)**
  - **Layout must meet the manufacturing design rules (DRC)**

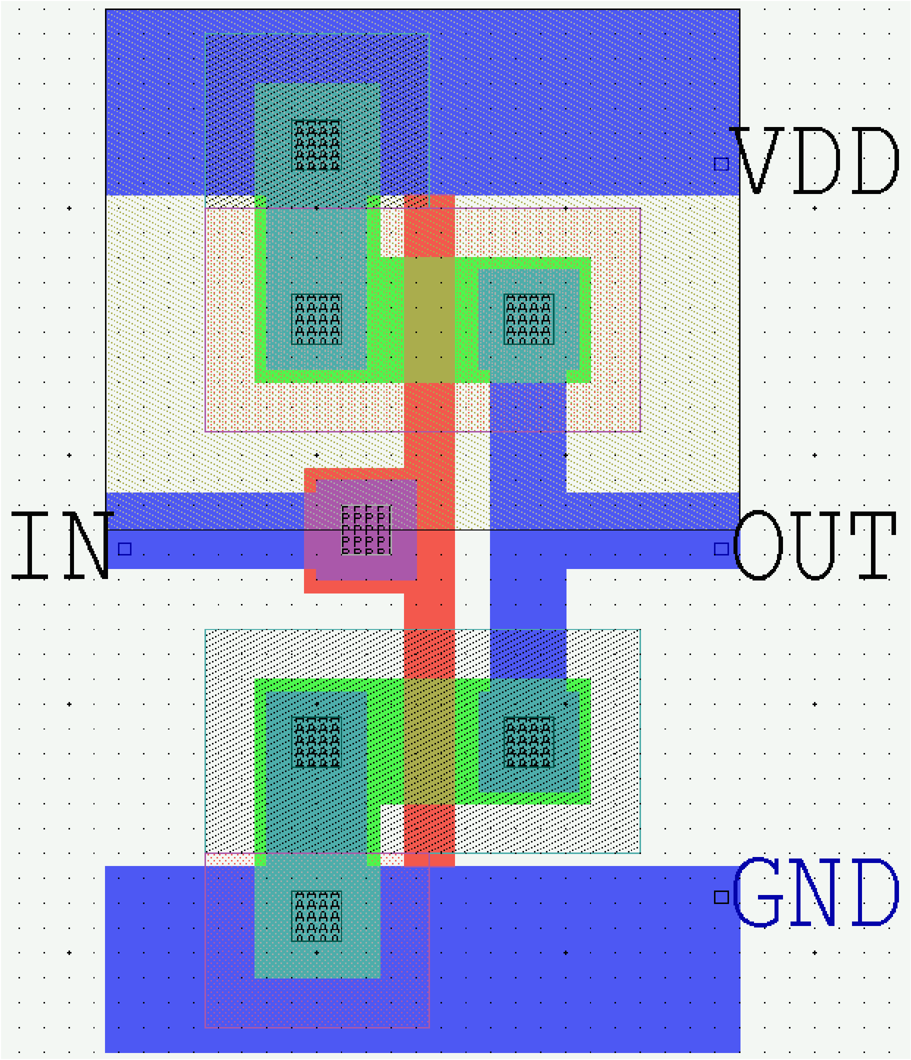
An Example of A Bad Layout



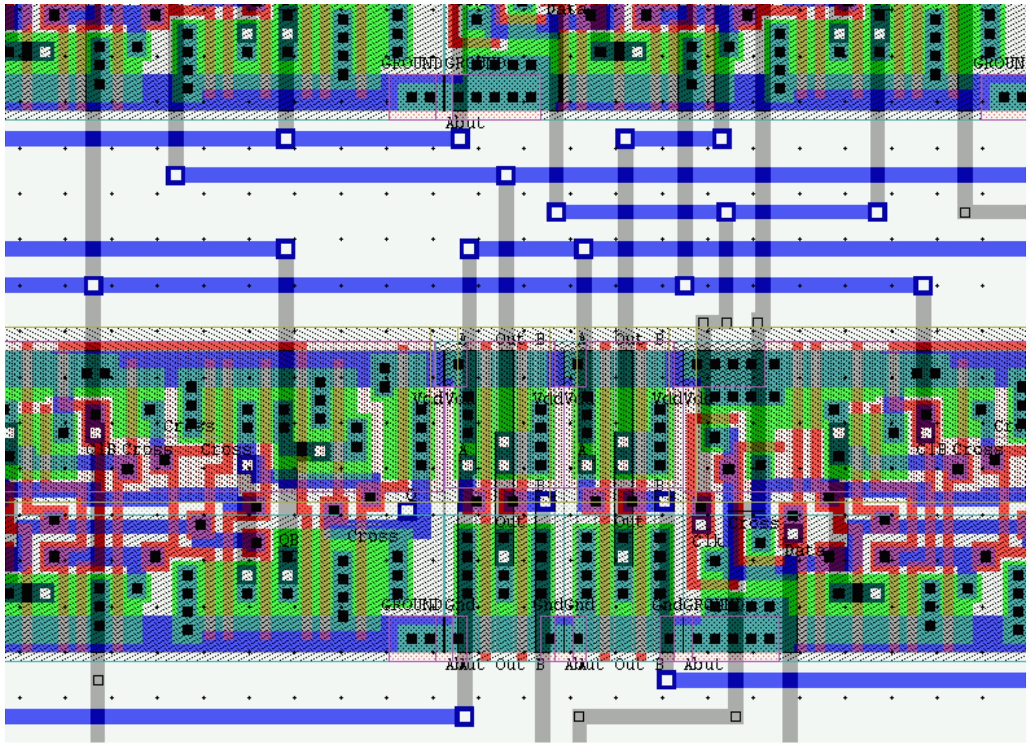
- Not dense
- Long poly route (large parasitic resistance)
- Narrow power rails

An Example of A Good Layout

- Very dense
- Short poly
- Wide power rails
- Both IN and OUT are in M1

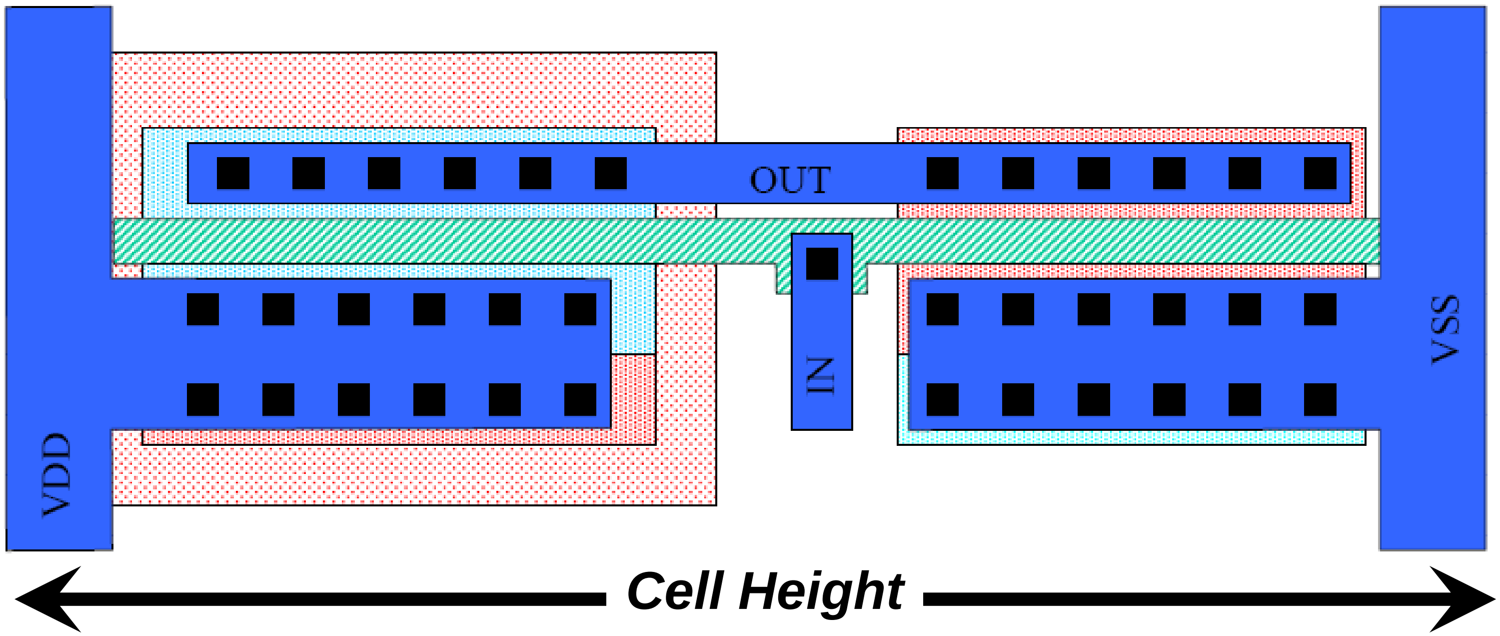


Channel Routing & Standard Cells



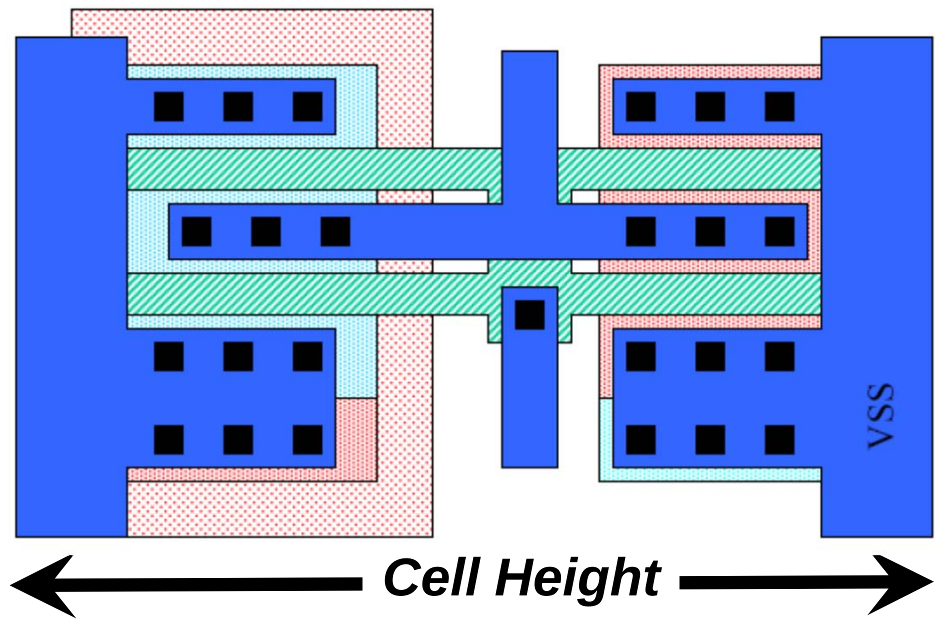
- ❑ **All power and ground are connected nicely**
  - **This require that all cell height be the same for every cell**
- ❑ **M1 is used for horizontal routing in the channel**
- ❑ **M2 is used for vertical routing**

Handling Large Device (Bad Layout)



- Long poly route (high resistance)
- Long source drain metal pickups (high resistance)
- Large cell height (mismatch with other cells)
- More component of diffusion cap then it needs to

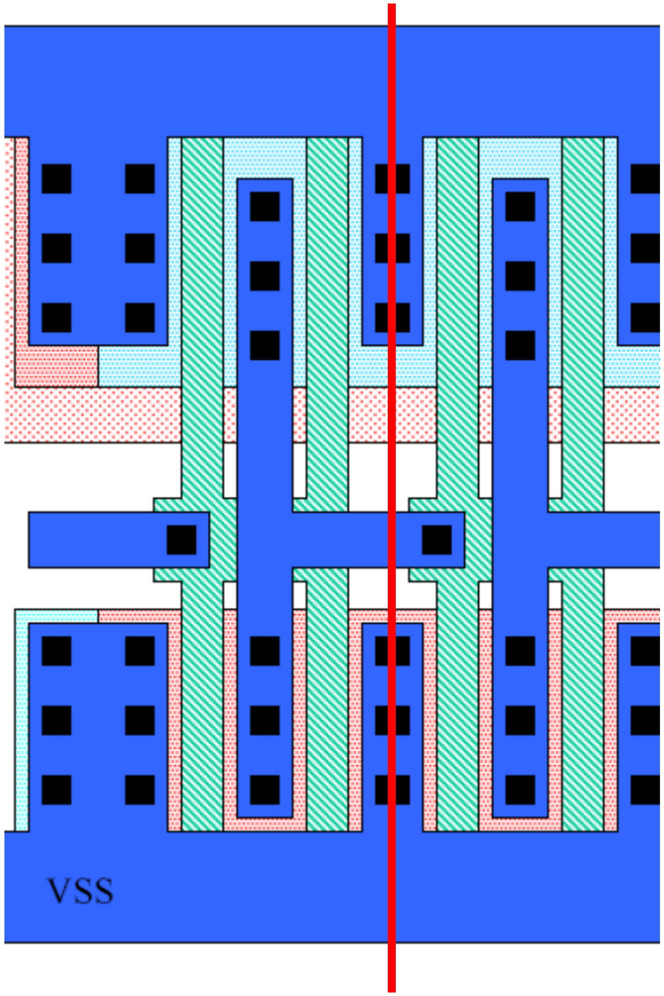
Handling Large Device (Good Layout)



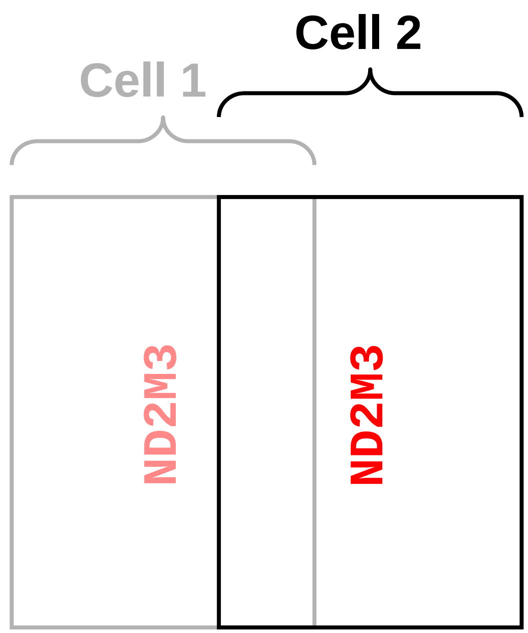
- The same drive strength (two folded transistor)
- Less diffusion capacitance (less P & A capacitance)
- Shorter poly route (lower resistance)
- Shorter source drain metal pickups (lower resistance)
- Smaller cell height (cab be matched with other cells)

Advantage of Folding Transistors

- **Less poly and metal length**
  - **Lower parasitic resistance**
  - **Lower parasitic capacitance**
- **Less Drain periphery and area**
  - **Less diffusion capacitance (less C_{out})**
- **Less cell aspect ratio**
  - **Better match with other cells**
  - **More compact and faster circuit**
- **Both ends are VDD or GND**
  - **Can easily share the ends with neighbors**

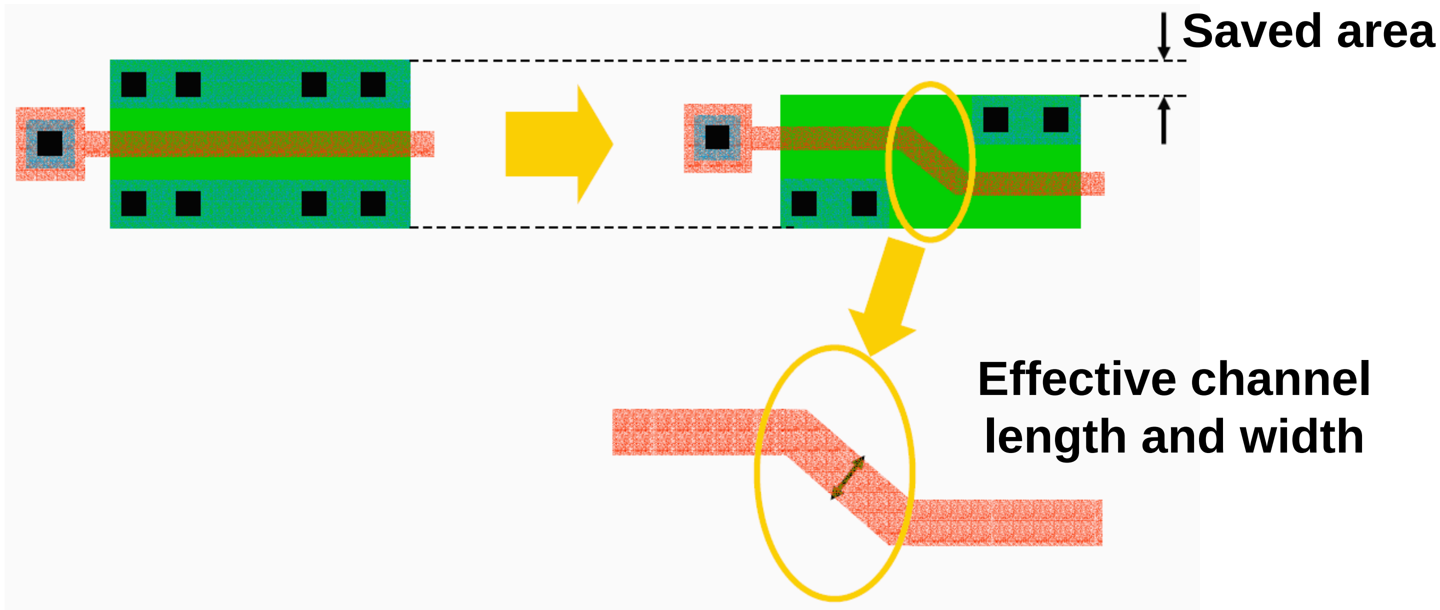


Overlapped Cells



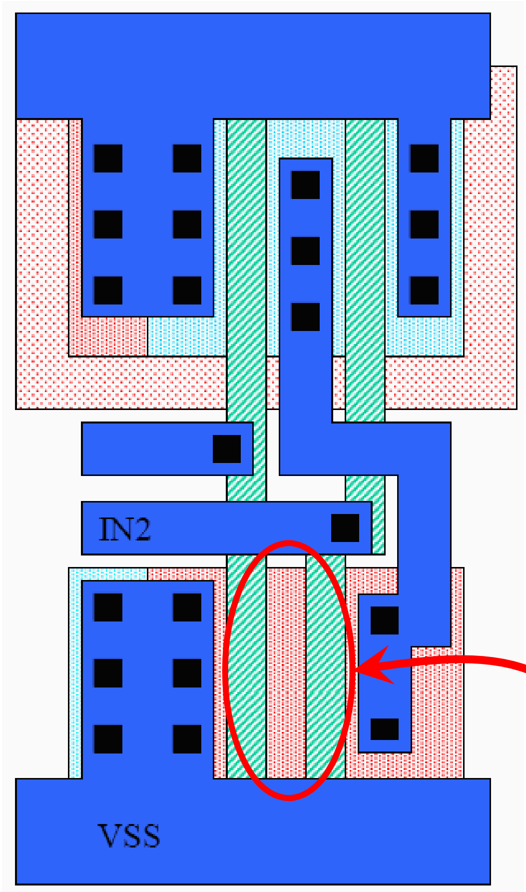
- **Our tools allow overlapping cells**
  - **This allows a cell to be complete and still share with the adjacent cell for better density**
- **This is why it is best to end cells on supplies**
  - **It is not possible to do always tough!**

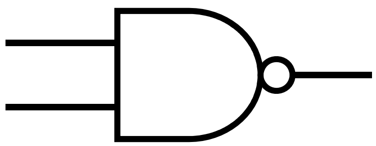
Bent Gate

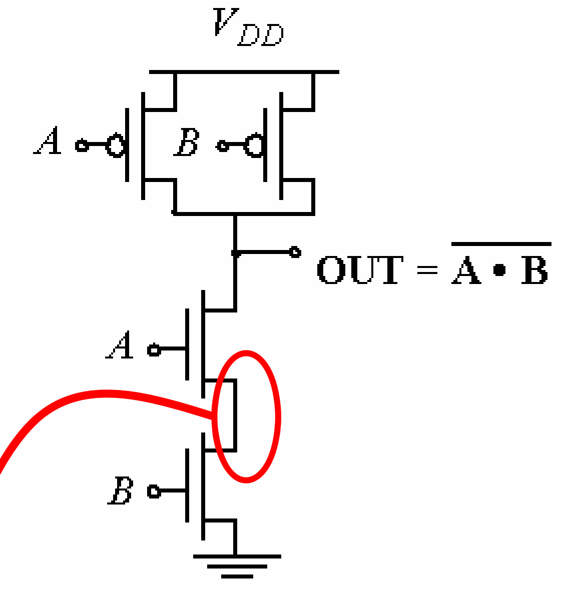


- If process permits, “bent gate” allows even denser layout
- Device modeling in this case requires more effort

Transistor Stacks

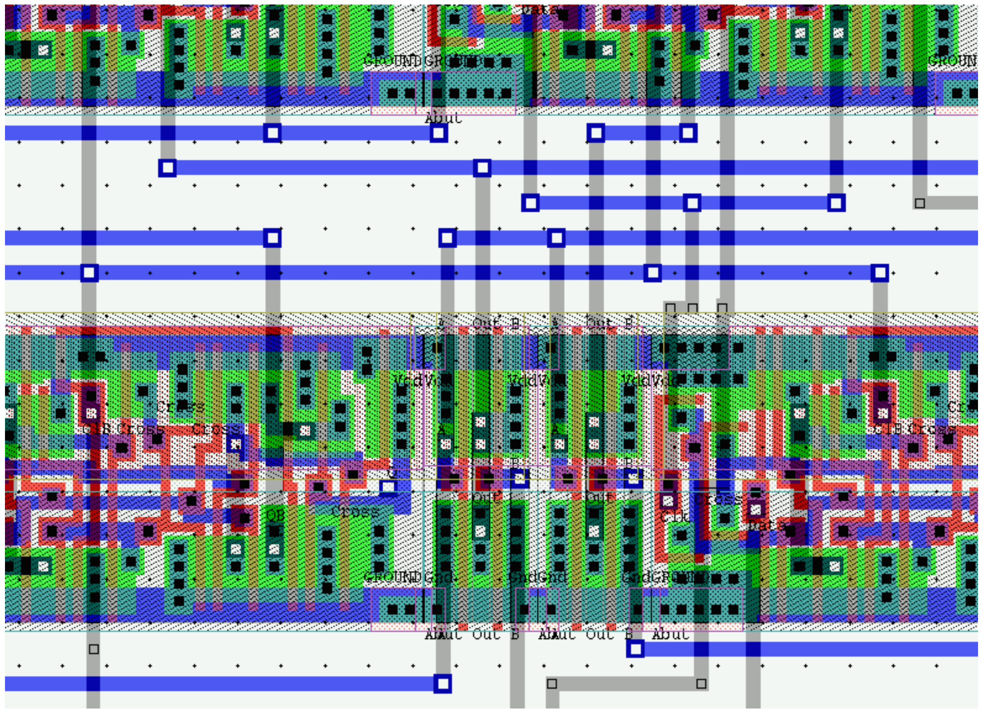






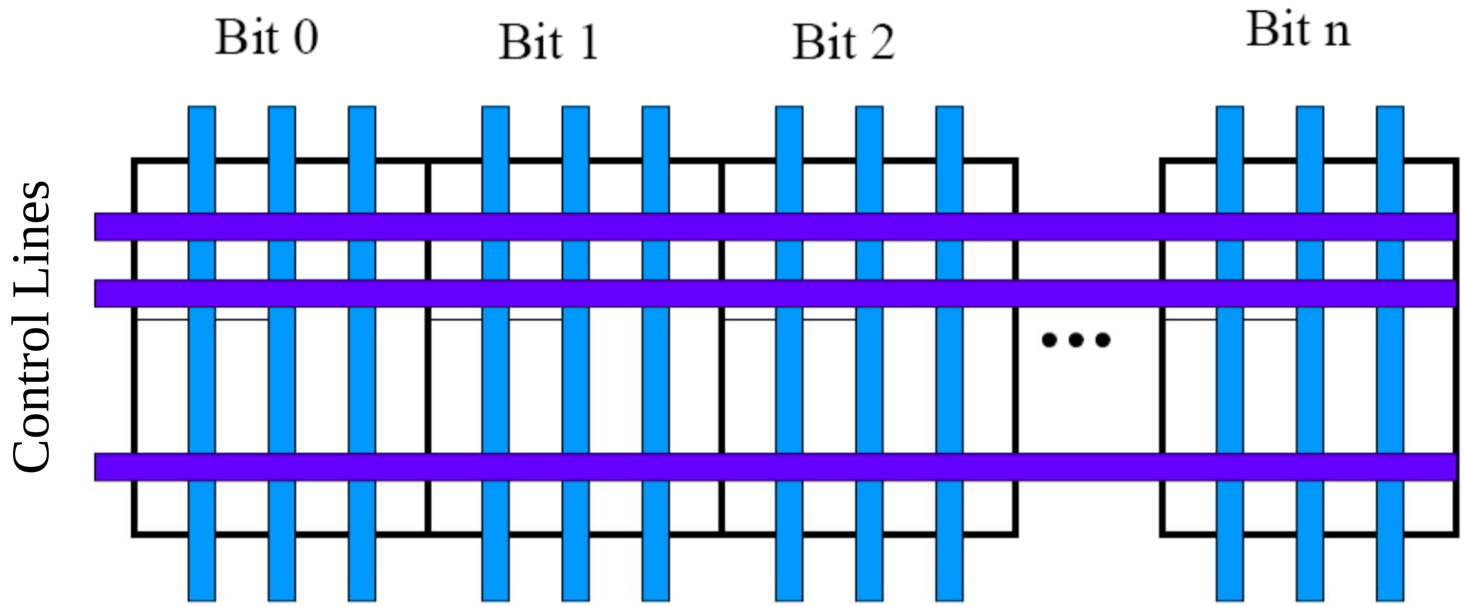
- ❑ **When there is no other connection between two series device, they can be stacked**
- ❑ **Poly can be placed closer in stacked devices (because of DRC), which results in less diffusion capacitance**

Random Logic Layout



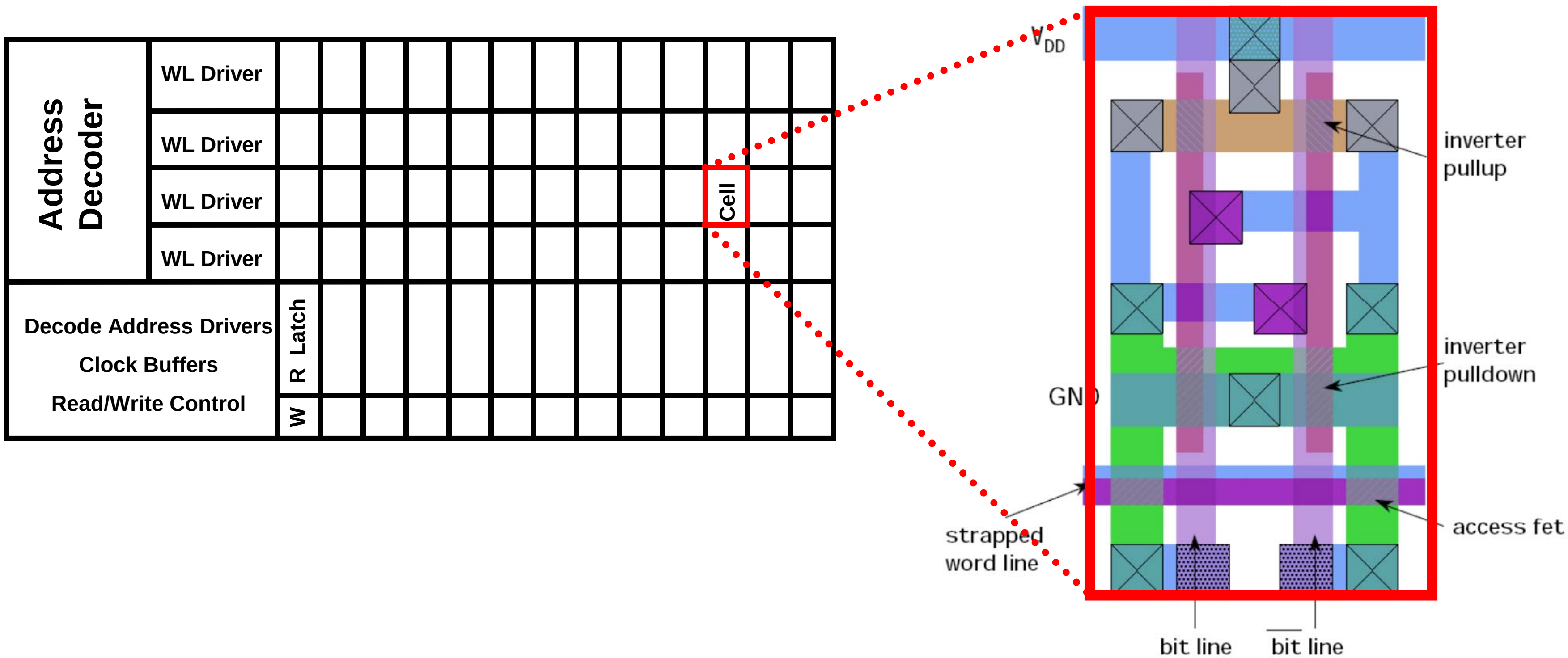
- Generally synthesized from an HDL description and automatically placed and routed (APR)
- Cells must be designed such that they line up nicely
- M1 is used for horizontal routing and M2 for vertical or vice versa

Data Path Layout



- All cells must lie on a fixed pitch
- Control lines cross and control all cells at once

SRAM Memory Layout



- All cells must lie on a fixed pitch (both directions)
- All lines "flow through" the cell and can be connected to adjacent cells by abutment
- The SRAM cells require no left right completion. Edge cells are required on top and bottom

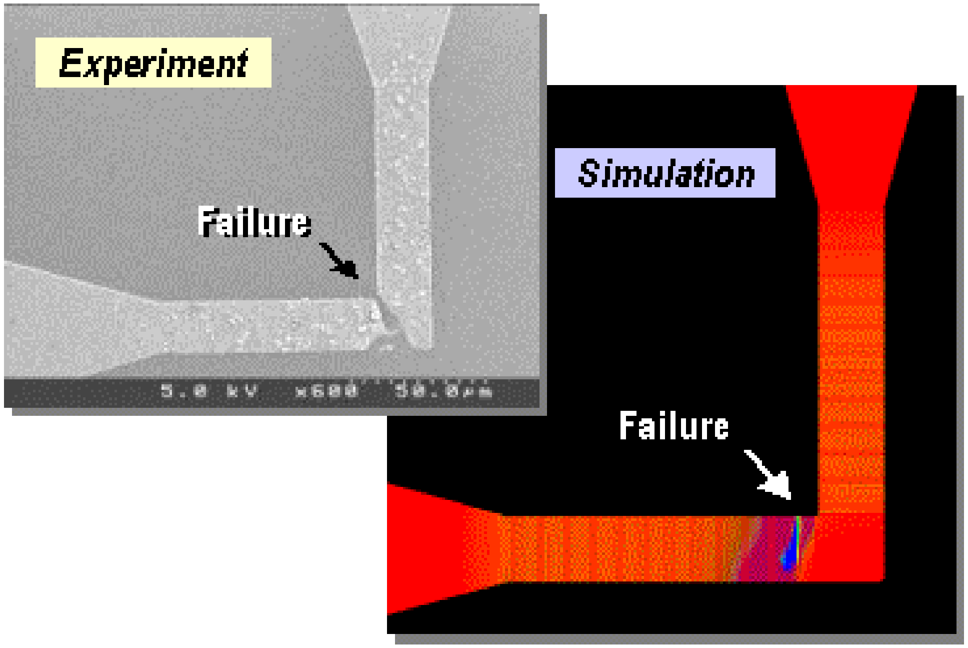
Layout Quality

- Electromigration (EM) and self-heating (SH) are the key reliability issues determined by layout
  - A quality layout will not limit the chip lifetime or speed

- Electromigration: Metal atoms swept out of position by "electron wind"
  - Only occurs on path where current flows in a single direction such as power supplies and between P and N devices
  - Depends on average current density
  - Highest at vias where the current crowds from the vias

- Self Heating: Long term failure of metal due to local IR heating
  - Occurs on wires with current flowing bidirectionally, eg, signal lines
  - Depends on I_{RMS}

Electromigration Modeling



- Using Physical models, we can predict where and when a failure can occurs
- By shrinking wire dimensions, electromigration is becoming more important
- Advanced VLSI technology will require checking the layout for electromigration as we do for DRC

Electromigration and Self-Heat

- **Electromigration**
  - Power Supply tracks
  - The track between PMOS and NMOS
  - Watch for “short circuit” current too
- **Self-Heat**
  - Output node wire
  - Can be large when C_L is large
- **If the transistors are large, pre-determine the wire size and number of contacts and vias to prevent EM and SH**