ECE520 – VLSI Design

Lecture 12: Gate Sizing (Inverter Chain)

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

Review of Last Lecture

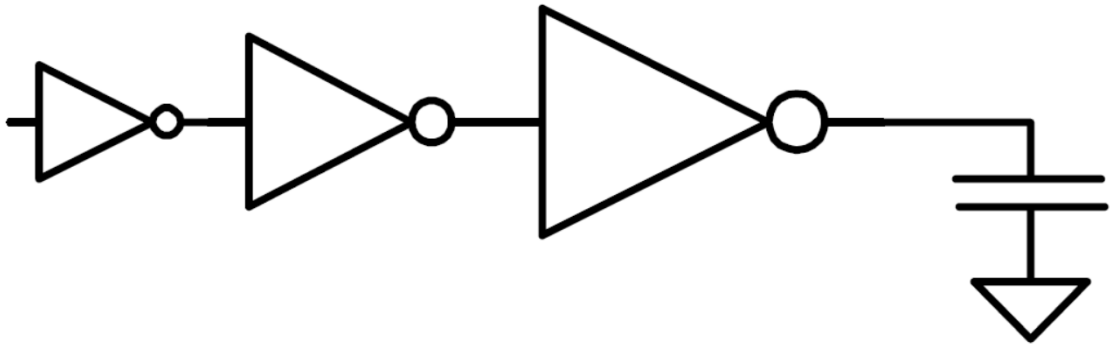
- **Combinational Logic**
  - Logic Design
  - Transistor Sizing
  - Delay Analysis

Today's Lecture

- **Quiz #2**
- **Gate Sizing (Inverter Chain)**

Sizing Logic Path for Speed

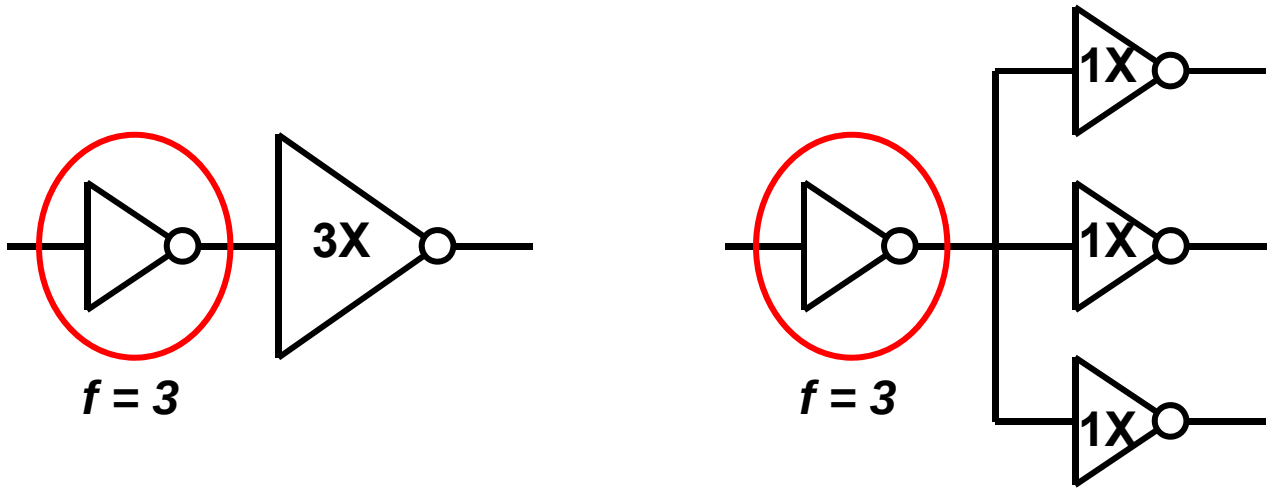
- Frequently, input capacitance of a logic path is constrained
- Logic also has to drive some capacitance
  - Example: ALU load in an Intel's microprocessor is 0.5pF
- How do we size the ALU data path to achieve maximum speed?



- Wide gate to drive a large load must be driven in turn
  - Large block inputs "push their load into the chip"

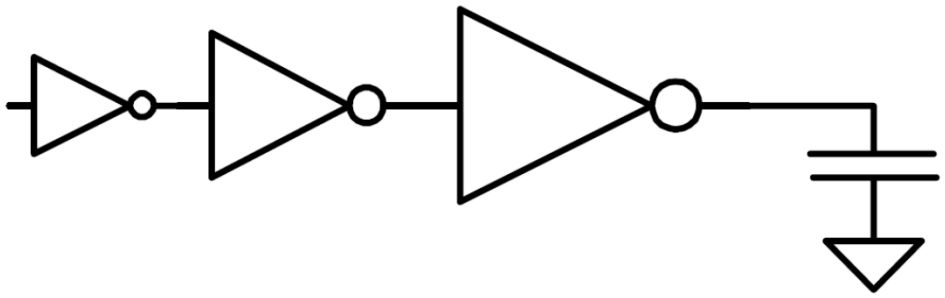
Definition: Fan-out

- Fan-out is the ratio between gate external load capacitance to its input capacitance, i.e. $f = C_{out} / C_{in}$.
- Another way: Fan-out is the "effective" number of gates that are connected to the output of the gate.
- Examples:

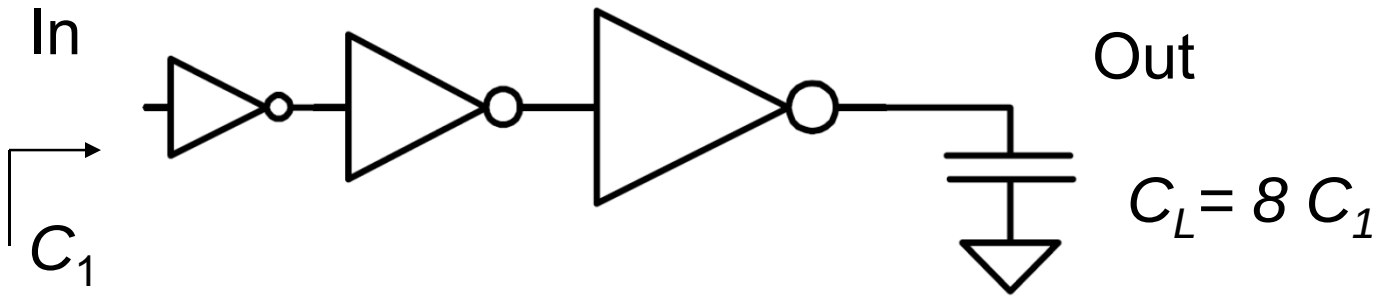


Inverter Chain Driving a Load Capacitance

- Assume inverter chain with fan-out factor of $f = C_{out} / C_{in}$
- Delay of i^{th} stage is $t_{p,i} \approx f_i \cdot t_{p0}$, where t_{p0} is intrinsic delay of an inverter
- Intuitively, for N stages the delay through each stage should be equal (this is true for most optimization problems)
- Therefore, delay and fan-out of every stage must be identical and equal to $t_p = f \cdot t_{p0}$



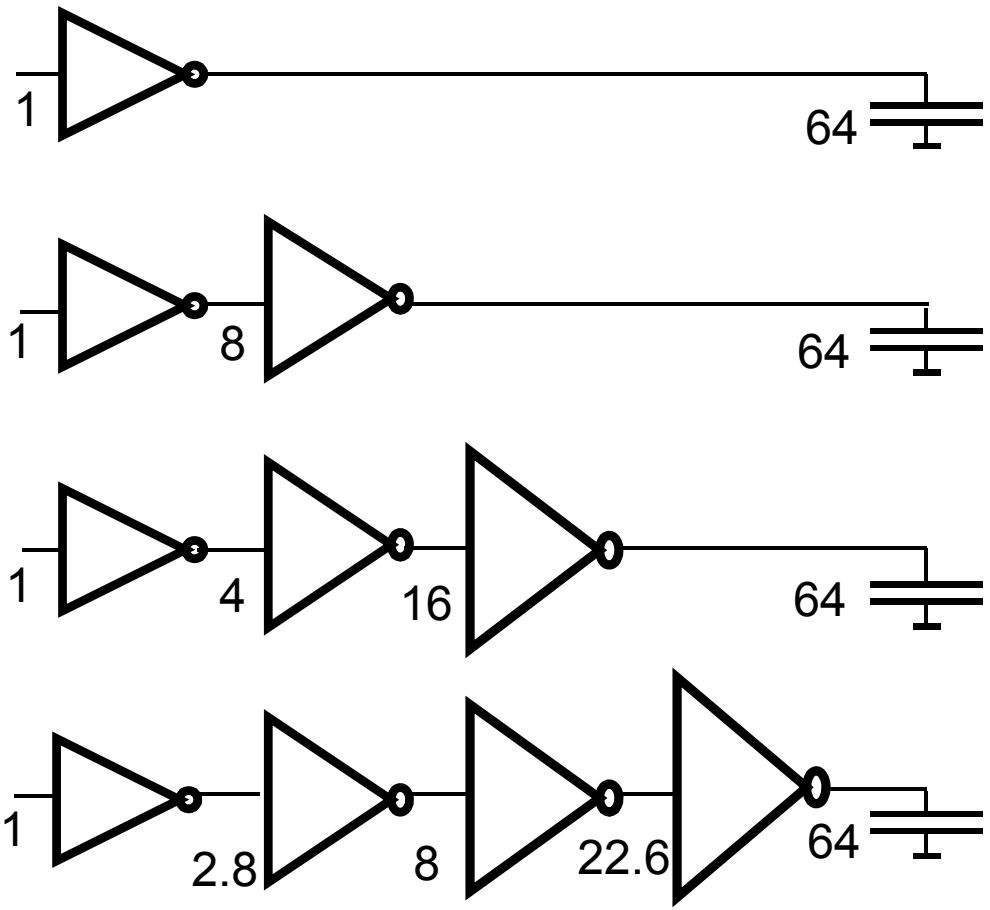
Example 1: Buffer Design



C_L/C_1 has to be evenly distributed across $N = 3$ stages:

$$f = \sqrt[3]{8} = 2$$

Example 2: Buffer Design



N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

How to Compute Optimum N?

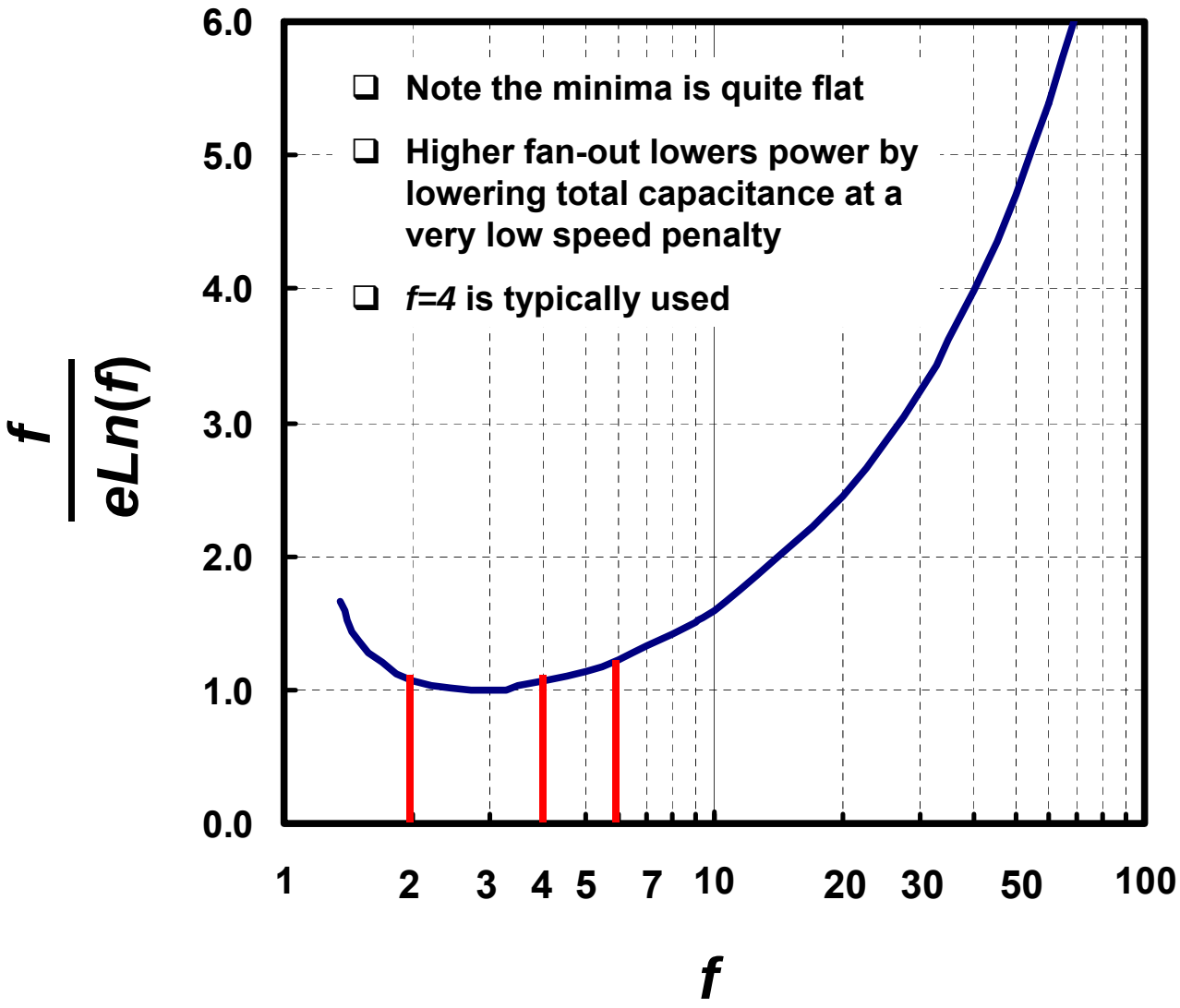
- Delay of a chain of N inverters is $t_p(chain) = N \cdot f \cdot t_{p0}$
- Define the ratio of load capacitance to input capacitance as $F=C_L/C_G$ (total for path, as opposed to f for each stage)
- C_L is the load driven, C_G is the load presented by the driving inverter
- Therefore, $F = f^N$
- Solving for $t_p(chain)$ gives:

$$t_p(chain) = Ln(F)\left(\frac{f}{Ln(f)}\right)t_{p0}$$

- When $f = e = 2.72$, minimum delay is:

$$t_p(chain) = eLn(F)t_{p0}$$

Normalized Delay versus f



Design Guideline

- Fan out should be approximately 4 unless path is very critical, i.e., limiting the entire chip speed
- This is so fundamental that speed is frequently discussed as the "fan out of 4 delay" as a figure of merit
- Start from the driven load and work backwards
- Driven load may be: Global or local routing load, clock distribution, and high fan-out net
- Take the time to size well, power and performance are the value added in custom design