

ECE520 – VLSI Design

Lecture 13: Logical Effort

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Review of Last Lecture

- Quiz
- Gate Sizing (Inverter Chain)

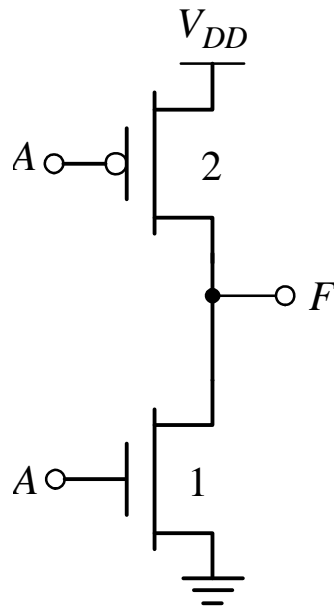
Today's Lecture

- Motivation
- Model the delay of one gate
- The delay of a chain of gates (multistage)
- Branching
- Minimum delay
- Best number of stages and gate sizing
- Examples
- Limitations

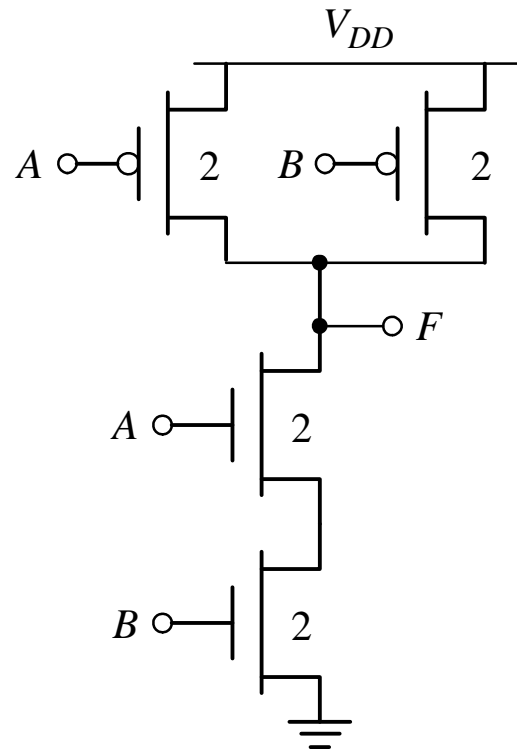
Logical Effort Motivation

- ❑ **Sizing of a chain of inverters**
 - Geometric progression
- ❑ **How about more complex logic?**
- ❑ **Logical Effort objectives:**
 - Quick and “back of the envelope” sizing
 - Make trade-off between circuits
- ❑ **Reference:**
 - I. Sutherland, B. Sproull, D. Harris, *Logic Effort - designing fast CMOS Circuits*, Academic Press, 1999

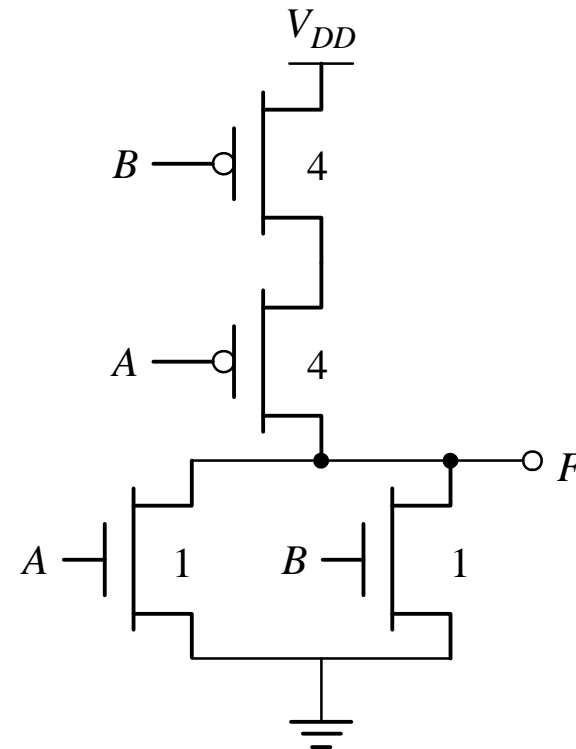
Why Do We Need Logical Effort?



Inverter



2-input NAND



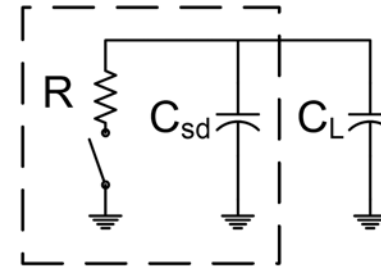
2-input NOR

- All three gates have the same drive strength. But, how about input capacitance?

Delay Scaling with Device Size

- Let's model an inverter with a resistor

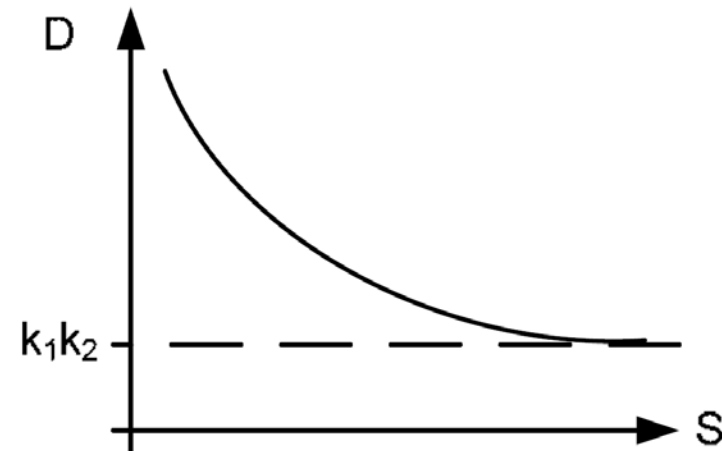
$$D \propto R(C_{sd} + C_L)$$



- If we scale the inverter by a ratio of S (i.e. $R=K_1/S$ and $C_{sd}=K_2S$), then

$$D \propto \frac{K_1}{S}(K_2S + C_L) \Rightarrow D \propto K_1K_2 + \frac{K_1}{S}C_L$$

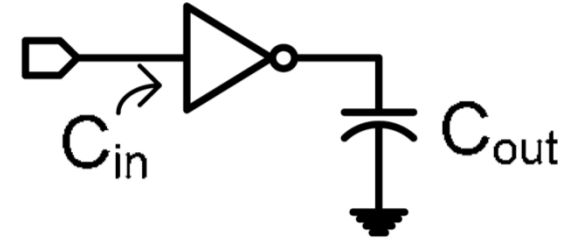
- The delay saturates to a value proportional to K_1K_2



Output / Input Load

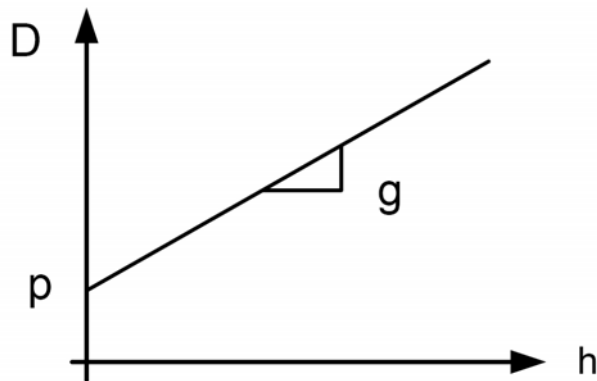
- Let's model the delay as a function of the output / input load

$$D \propto R(C_{sd} + C_L)$$



- If we scale the inverter by a ratio of S (i.e. $R=K_1/S$, $C_{sd}=K_2S$, and $C_{in}=K_3S$), then

$$D \propto \frac{K_1}{S} \left(K_2S + K_3S \frac{C_{out}}{C_{in}} \right) \Rightarrow D \propto \underbrace{K_1K_2}_p + \underbrace{K_1K_3}_g \underbrace{\frac{C_{out}}{C_{in}}}_h$$



$$\Rightarrow D \propto p + gh$$

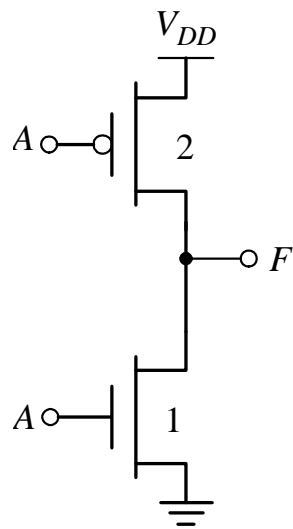
Definitions

- ❑ **p** is the “**intrinsic delay**” and is a function of the technology
 - Intrinsic delay of the gate due to its own internal capacitances (Unloaded delay of a gate)
- ❑ **g** is the “**logical effort**” and is a function of the complexity of a gate, not its size
 - characteristic of the gate type, and that gate’s ability to drive a given load
- ❑ **h** is the “**electrical effort**” and characterizes the load
 - The electrical effort is defined by $h = C_{out}/C_{in}$ and it represents the fan-out or load that a given gate is subjected to
- ❑ Reference is the inverter where $g=1$ and $p=0.6\sim 1$

$$D = t_{p0}(p + gh)$$

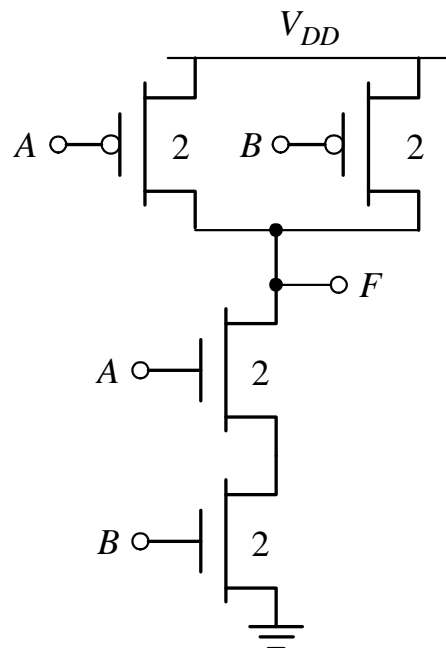
Logical Effort

- Logic effort is the size of a gate relative to an inverter to produce the same output current as an inverter with the same output load



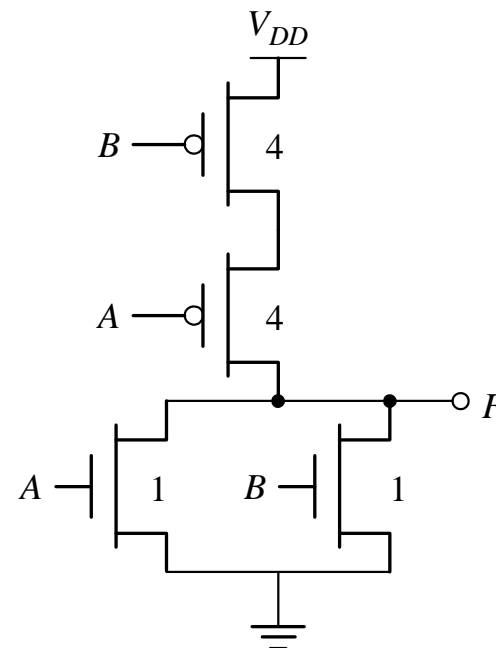
Inverter

$$g = 1$$



2-input NAND

$$g = 4/3$$



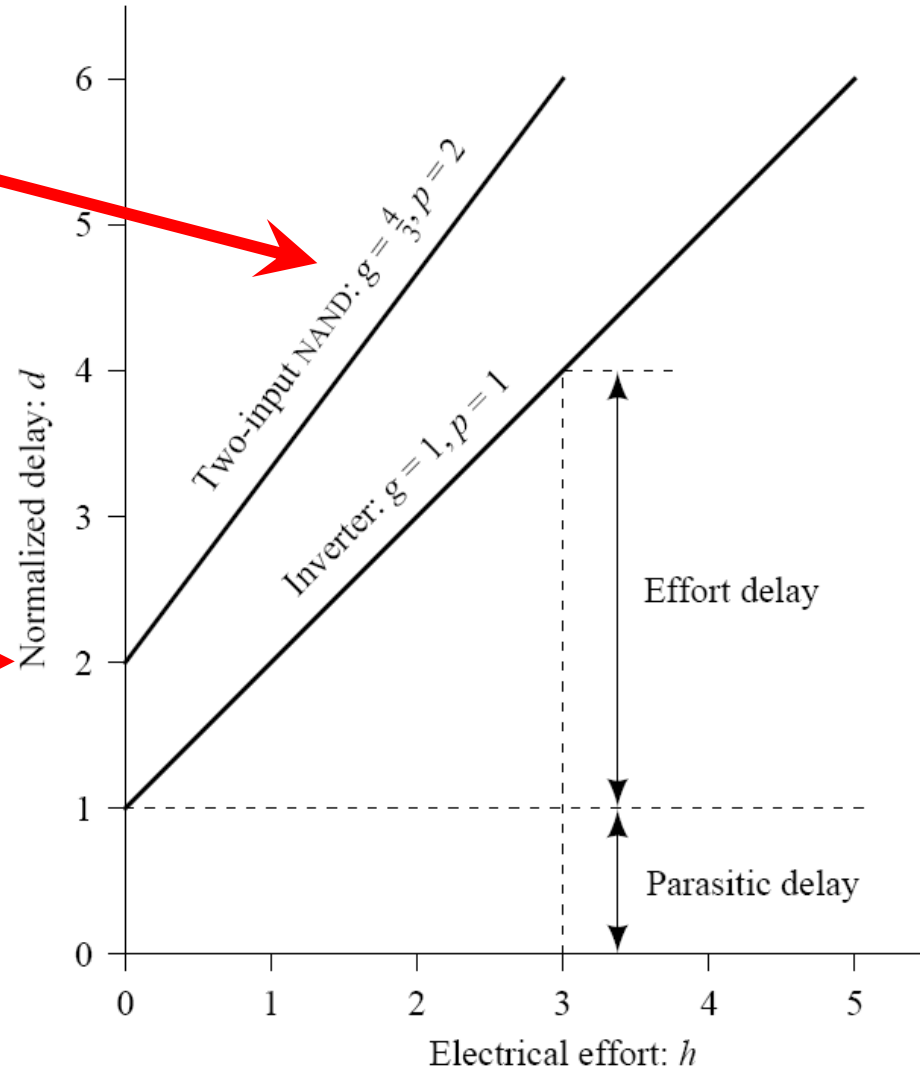
2-input NOR

$$g = 5/3$$

Delay Components

Slope rises faster, since given transistor sizes are less effective in the NAND2 configuration

Parasitic Delay is higher for NAND2



Parasitic Delay (p)

Gate type	Parasitic Delay
Inverter	p_{inv}
n -input NAND	$n \cdot p_{inv}$
n -input NOR	$n \cdot p_{inv}$
n -way multiplexer	$2n \cdot p_{inv}$
XOR, XNOR	$4 \cdot p_{inv}$

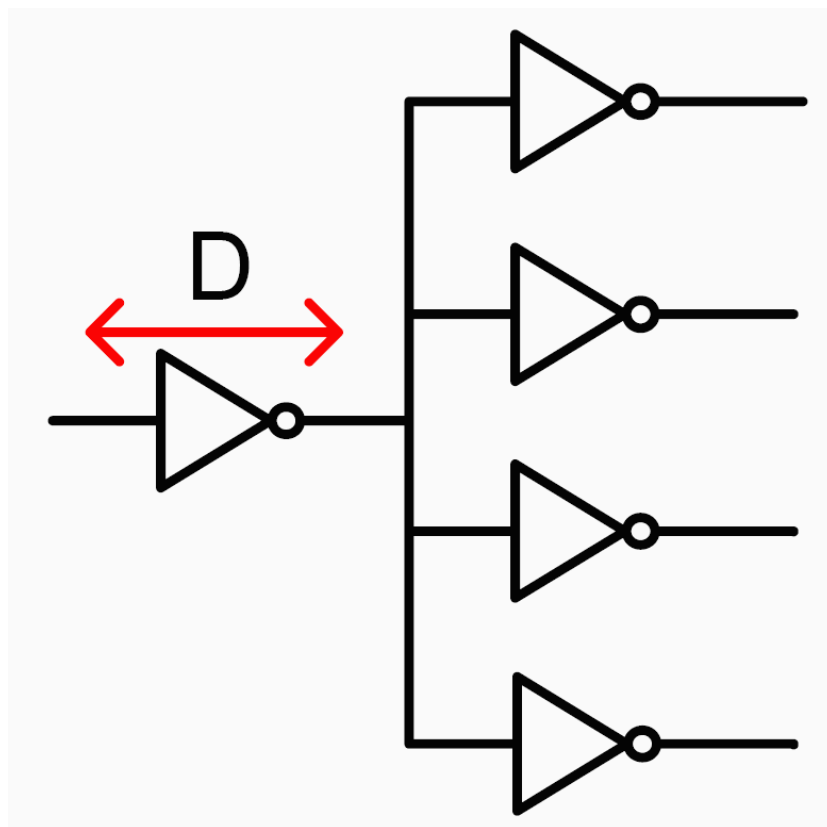
- ❑ Notice that inverter has the minimum intrinsic delay. Intrinsic delay increases for complex logic gates.
- ❑ Why n -input gates (fan-in = n) have n times parasitic delay of the same size inverter?

Logical effort (g)

Gate type	Number of inputs					
	1	2	3	4	5	n
Inverter	1					
NAND		4/3	5/3	6/3	7/3	$(n + 2)/3$
NOR		5/3	7/3	9/3	11/3	$(2n + 1)/3$
Multiplexer		2	2	2	2	2
XOR (parity)		4	12	32		

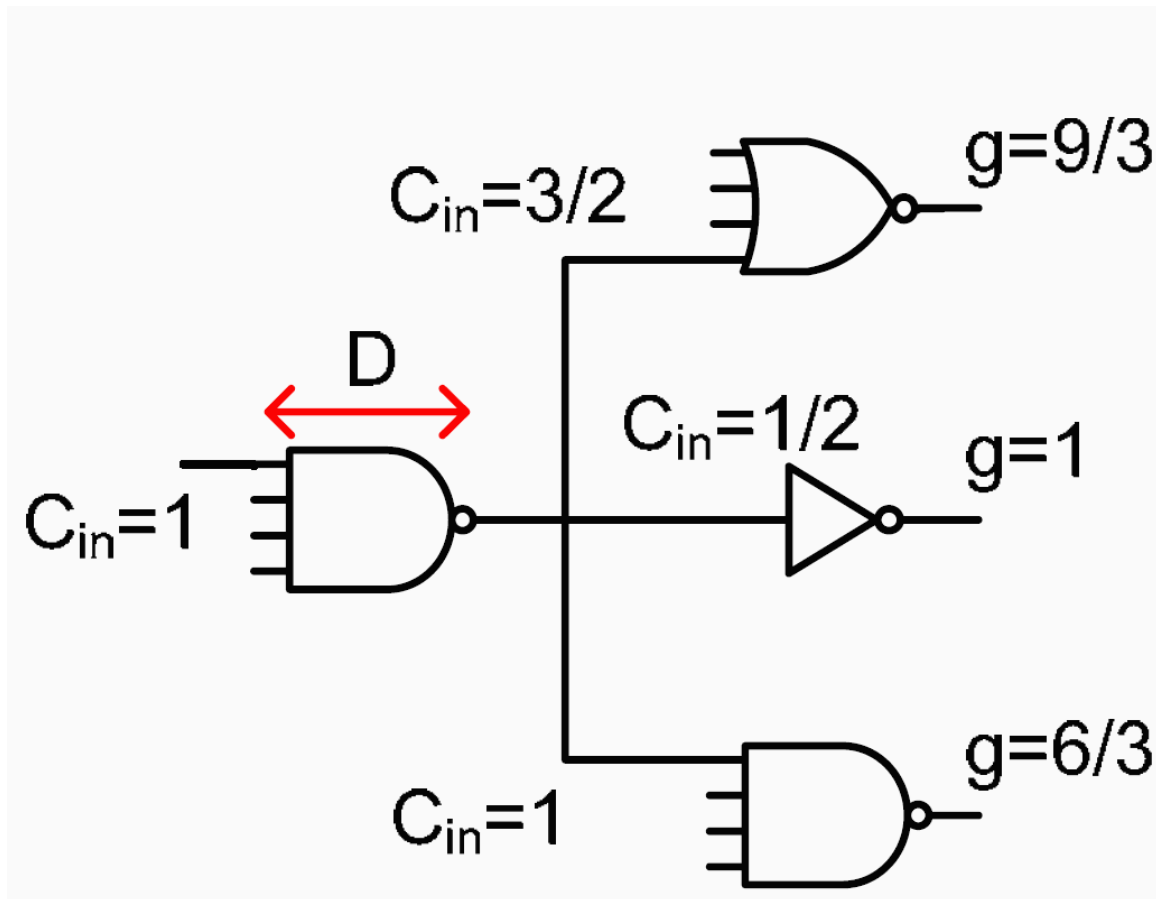
- Notice that inverter has the lowest logical effort. Logical effort increases for complex logic gates.

F04 Example



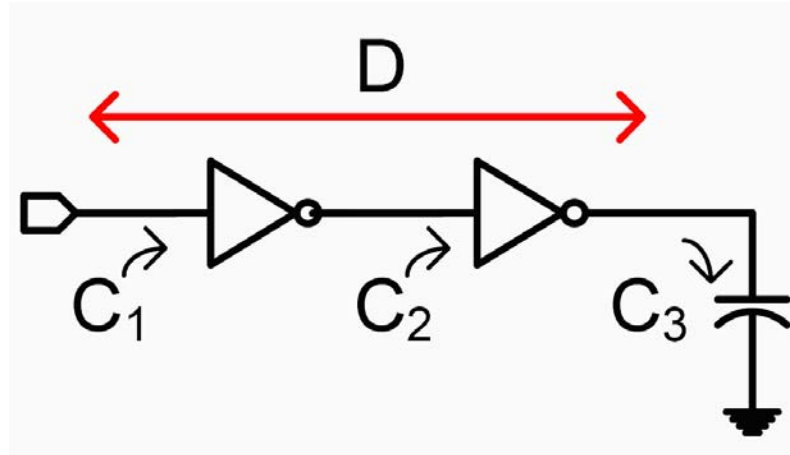
- What is the delay, D , in this logic circuit?

More Complex Example



□ What is the delay, D , in this logic circuit?

Multistage Effort

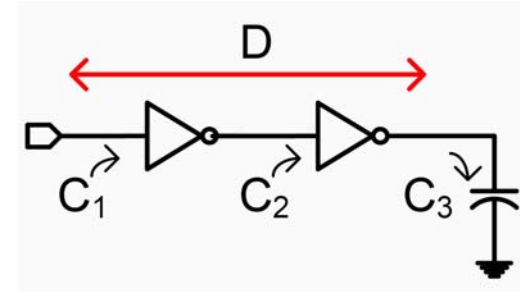


- Defining the “path effort” H as

$$H = \frac{C_3}{C_1} \quad \left\{ \begin{array}{l} h_1 = \frac{C_2}{C_1} \\ h_2 = \frac{C_3}{C_2} \end{array} \right. \quad \rightarrow \quad H = h_1 h_2$$

Minimum Delay

Total Delay: $D = \underbrace{(p_1 + g_1 h_1)}_{D_1} + \underbrace{(p_2 + g_2 h_2)}_{D_2}$



Substitute H: $D = p_1 + g_1 h_1 + p_2 + g_2 \frac{H}{h_1}$

$$\min\{D\} \Rightarrow \frac{\partial D}{\partial h_1} = g_1 - g_2 \frac{H}{h_1^2} = 0$$

Minimize the delay

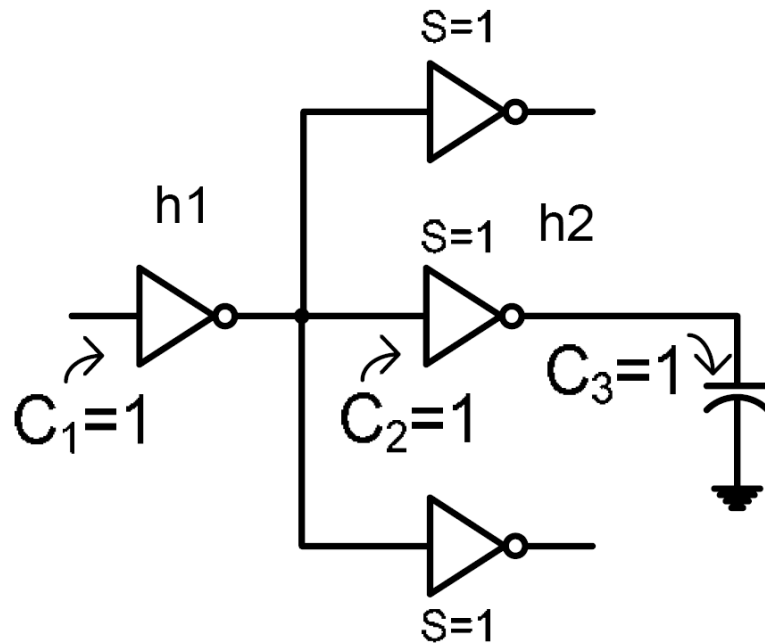
$$g_1 - g_2 \frac{h_2}{h_1} = 0$$

Solve for minimum delay

$$g_1 h_1 = g_2 h_2 \Rightarrow \textcircled{f_1 = f_2}$$

Delay is optimal when the stage efforts are equal

Branching



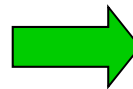
Without branching: $H = h_1 h_2$

With branching: $h_2 = \frac{C_3}{C_2}$

$$h_1 = \frac{3C_2}{C_1}$$

$$h_1 h_2 = 3H$$

$$b_i = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$



$$C_{on-path,2} = C_2$$

$$C_{off-path,2} = 2C_2$$

$$b_2 = \frac{3C_2}{C_2} = 3$$

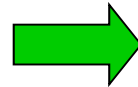
Equivalent Path Efforts

$$H = \frac{C_{out}}{C_{in}}$$

$$B = \prod b_i$$

$$\prod h_i = BH$$

$$G = \prod g_i$$



$$F = GBH = \prod g_i h_i$$

- ❑ Path effort does not change with added inverters
- ❑ Path effort does not depend on sizes, but on topology

Minimum Delay

$$F = GBH = \prod g_i h_i$$

Stage effort of stage i : f_i

$$g_i h_i = f_i$$

Optimal stage effort is:

$$\hat{f} = f_i$$

For N stages:

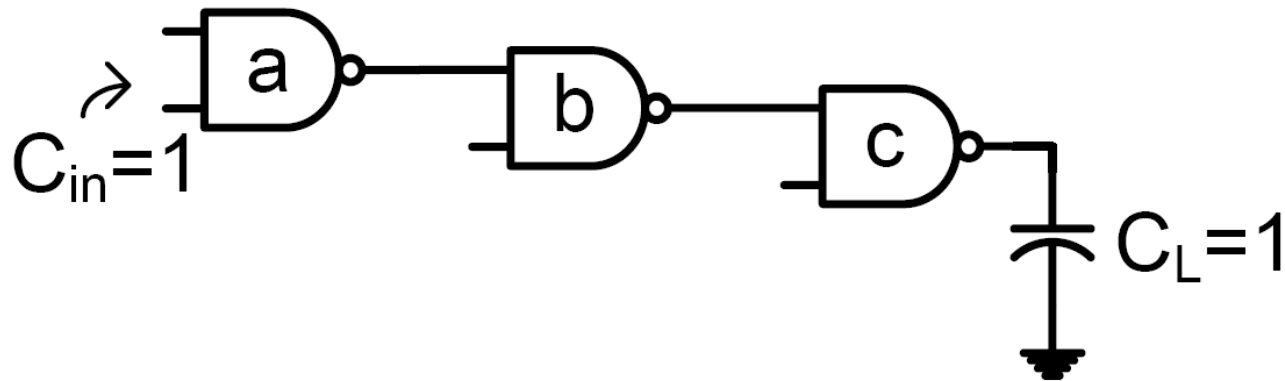
$$F = \hat{f}^N \Rightarrow \hat{f} = F^{1/N}$$

Minimum delay:

$$\hat{D} = \sum_i (p_i + g_i h_i)$$

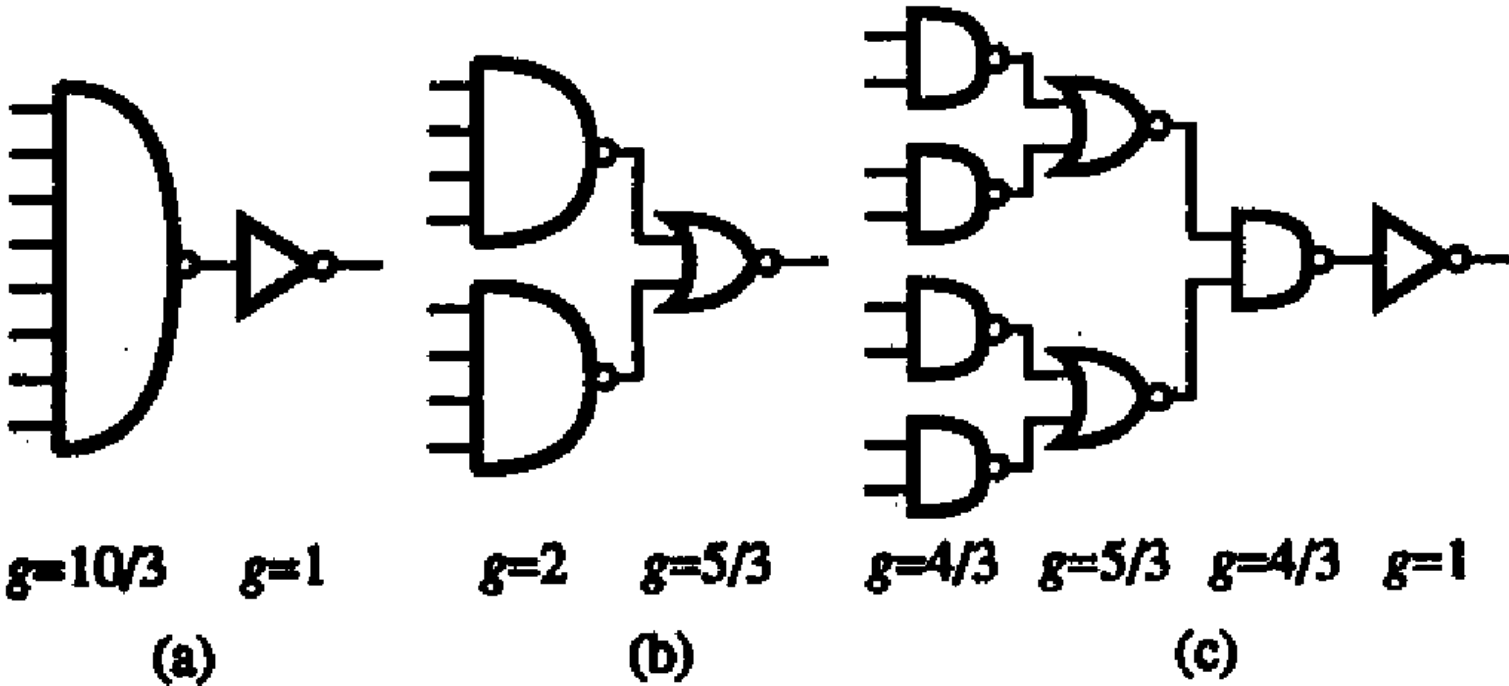
$$\hat{D} = \sum_i p_i + N\hat{f} = P + N\hat{f}$$

Example 1: Compute min Delay



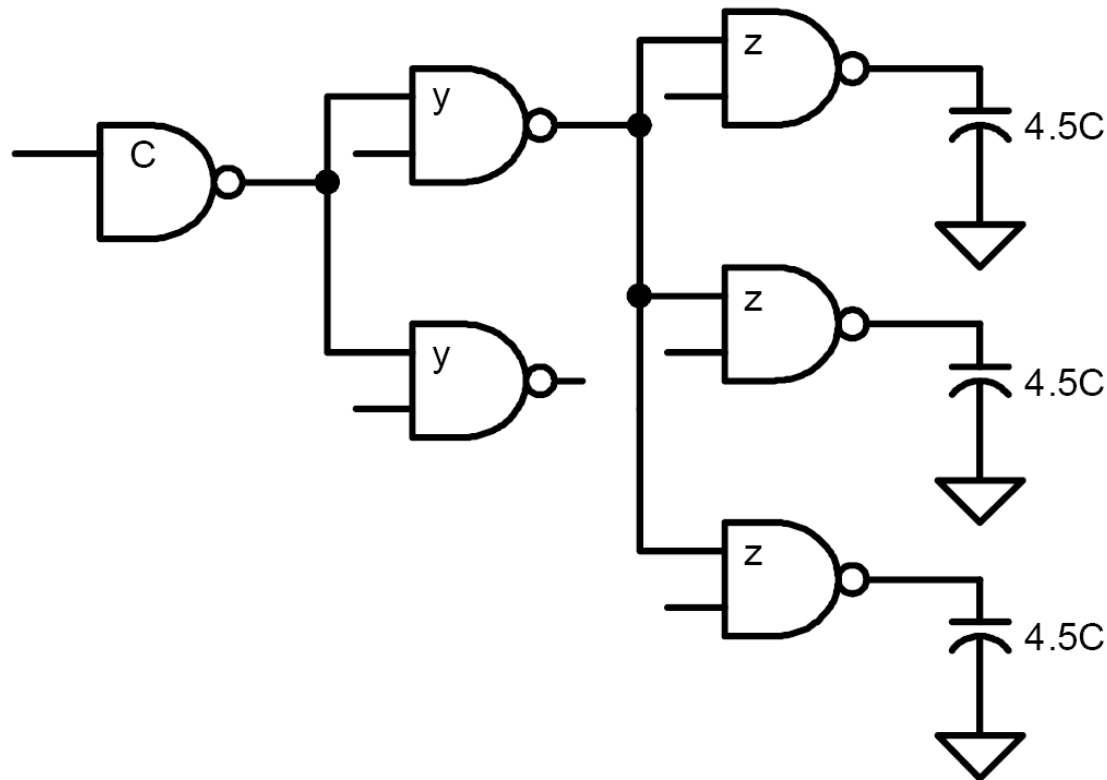
- What is the minimum delay in this circuit?

Example 2: Compute min Delay



□ Which circuit provides less delay?

Example 3: Optimum Gate Sizing



- How to size the gates to minimize the total delay?