ECE520 – VLSI Design

Lecture 14: Pseudo Logic and Pass-Transistor Logic

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Review of Last Lecture

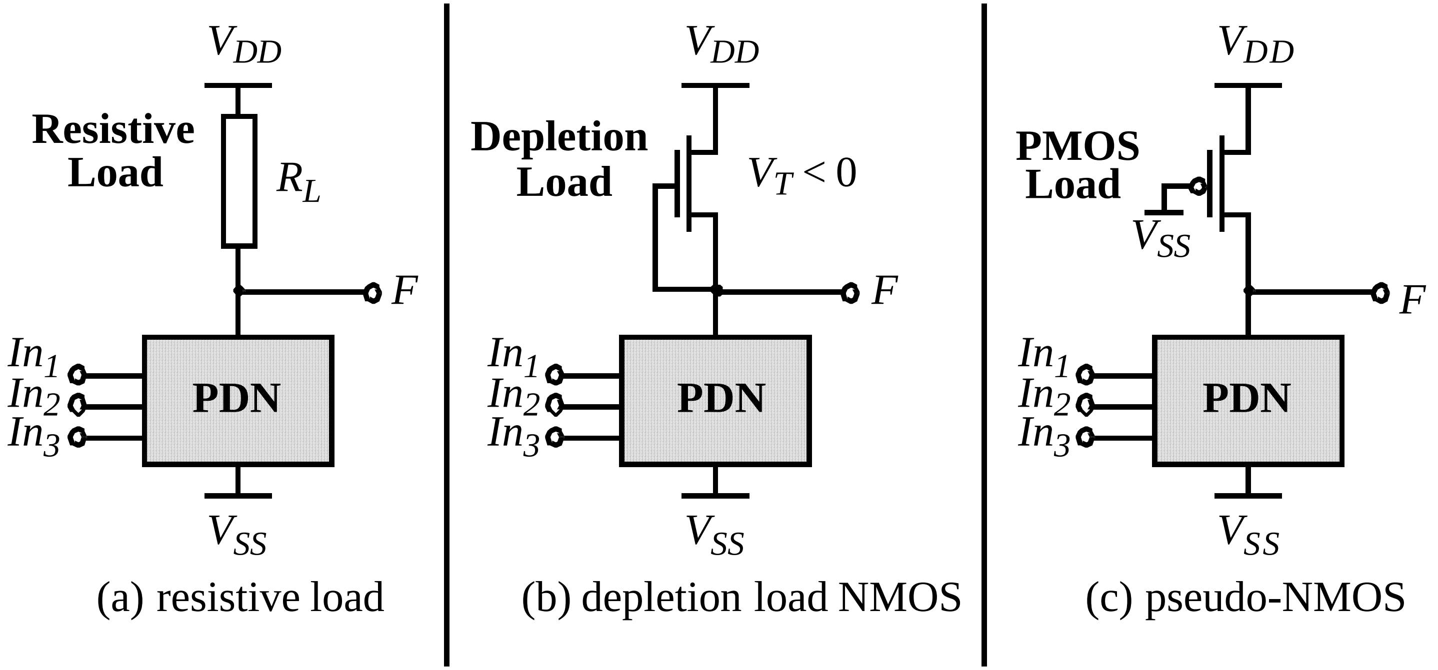
- Midterm Exam

Today's Lecture

- **Midterm Exam Review**
- **Other Types of Static Logic**
  - **Pseudo logic**
  - **Pass-transistor logic**

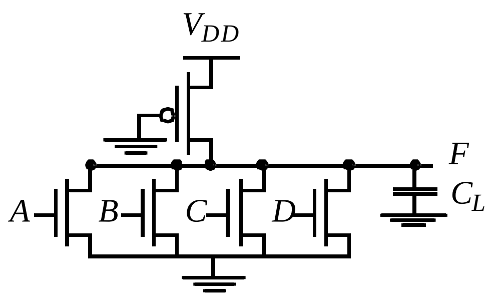
Ratioed Logic

- One way to reduce the number of transistors in complex logic gate is to replace pull up network (PUN) with a resistor.
- Here are some examples:



Pseudo-NMOS Logic

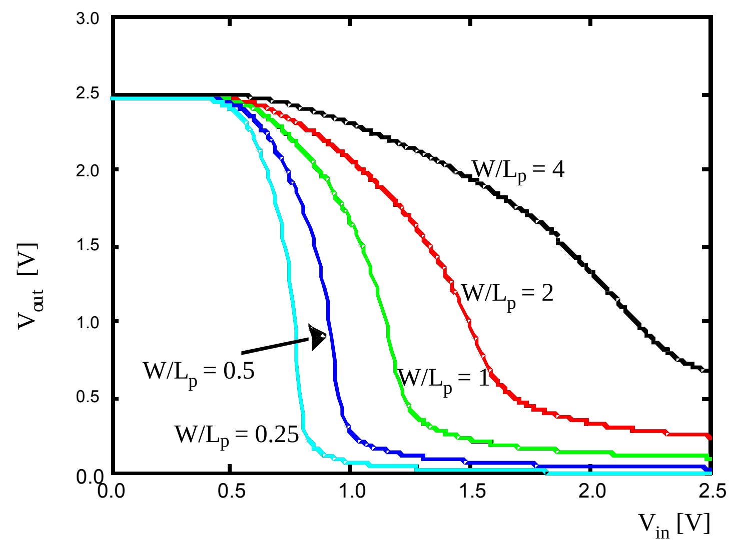
- The size of the pull-up PMOS transistor should must meet noise margin criteria (and V_{OL}).



$V_{OH} = V_{DD}$ *(similar to complementary CMOS)*

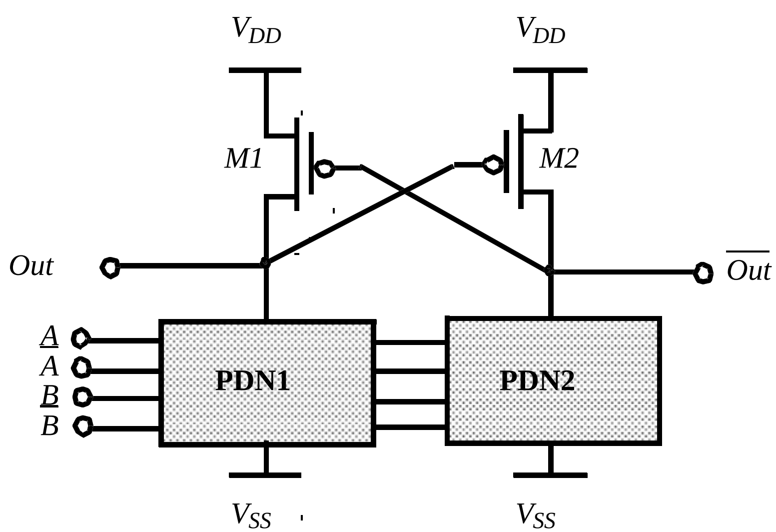
$$k_n\left((V_{DD} - V_{Tn})V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{k_p}{2}(V_{DD} - |V_{Tp}|)^2$$

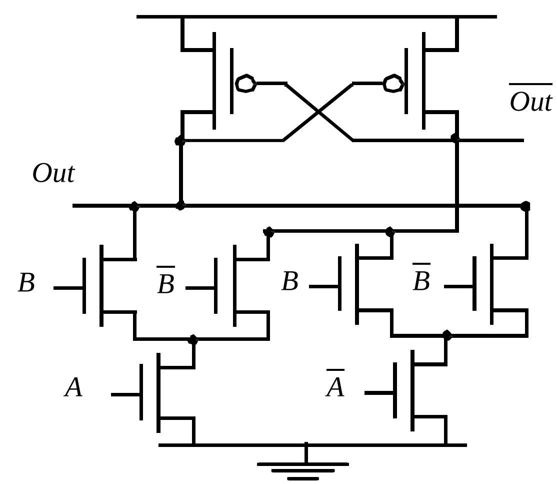
$$V_{OL} = (V_{DD} - V_T)\left[1 - \sqrt{1 - \frac{k_p}{k_n}}\right] \text{(assuming that } V_T = V_{Tn} = |V_{Tp}|\text{)}$$



Improved Pseudo Logic

- Static power dissipation is prohibitively large in Pseudo NMOS logic.
- Differential Cascode Voltage Switch Logic (DCVSL) can eliminate static power dissipation.
- Although it is more complicated and requires more transistors, it provides both complementary outputs.

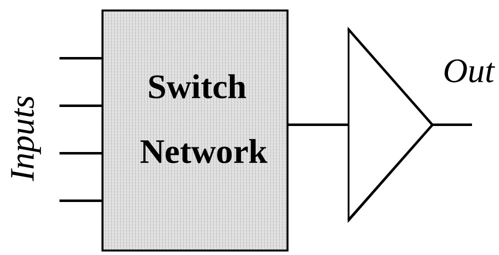


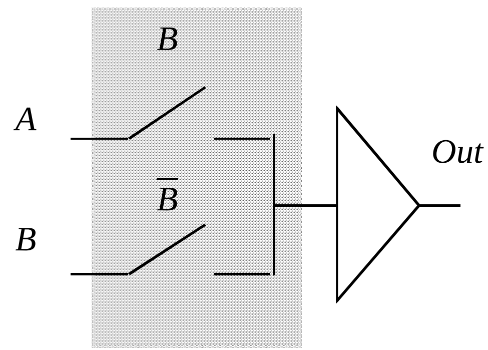


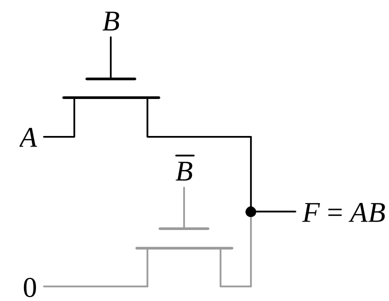
XOR-NXOR gate

Pass-Transistor Logic

- Another way of reducing the number of transistors in complex logic gate is to use switch network.
- For instance AND gate can be implemented by only 4 transistors (instead of 6 transistor in CMOS implementation)



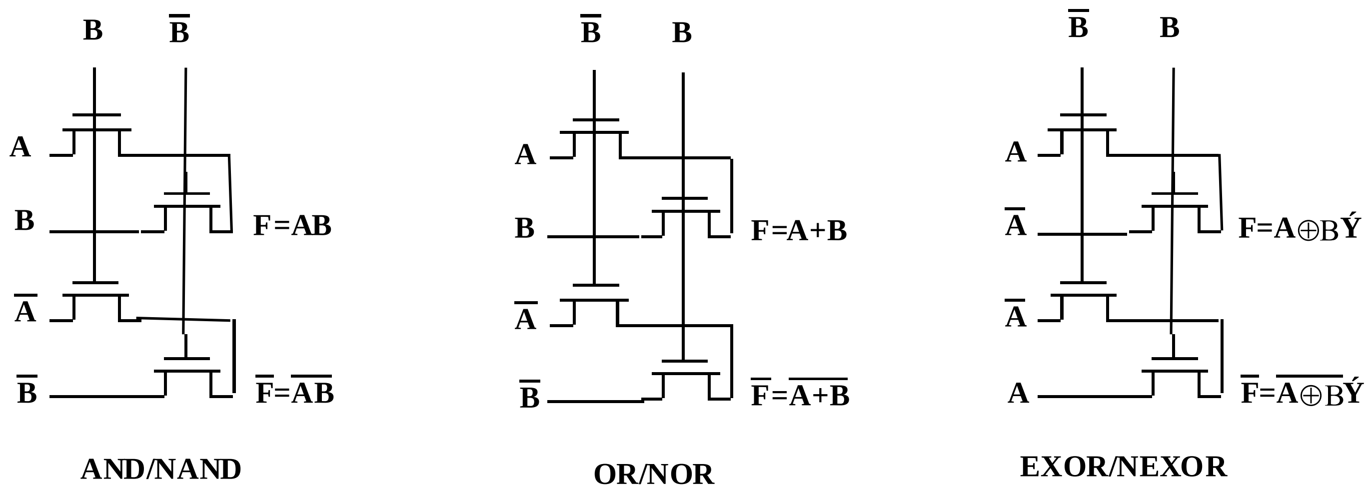




- N transistors
- No static consumption

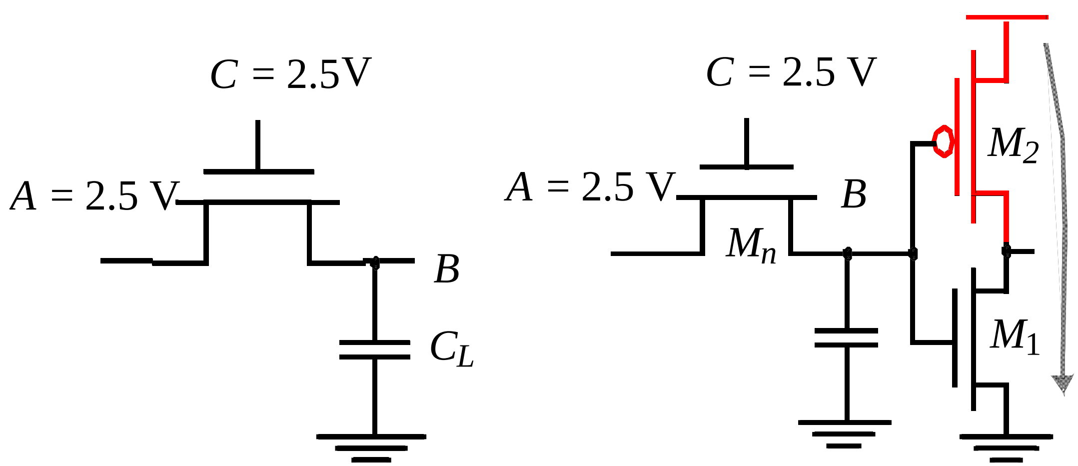
Examples: Pass Transistor Networks

- **Differential logics can be implemented using pass-transistor logic.**
- **These examples show that a complicated logic gate can be implemented with only few transistors**



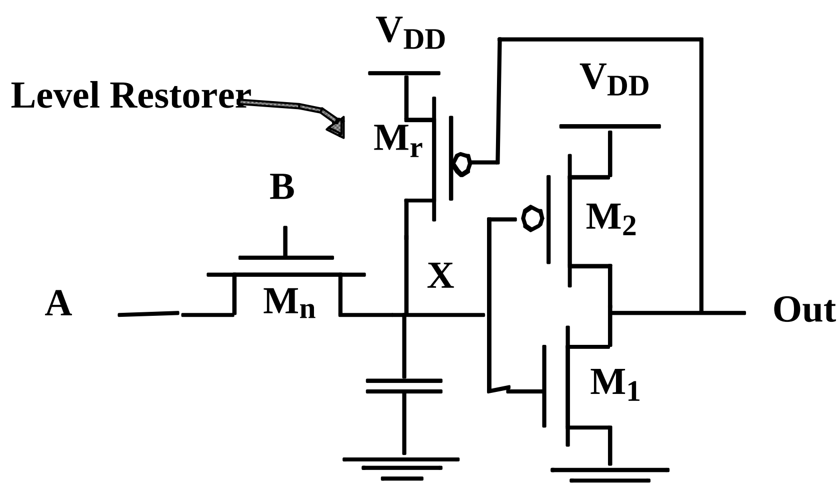
Pass-Transistor Logic Limitation

- Warning: pass-transistor gates cannot be cascaded due to threshold drop.
- Even one threshold drop can cause major problem:
  - V_B does not pull up to 2.5V, but to 2.5-V_{TN}
  - Threshold voltage loss causes static power consumption
  - Due to body effect NMOS has higher threshold than PMOS



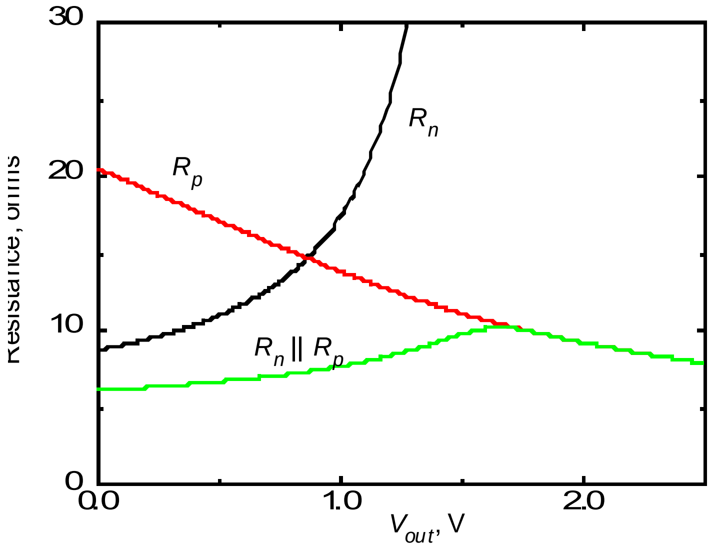
Solution 1: Level Restorer

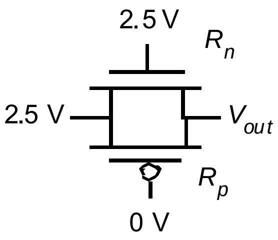
- Level restorer force V_X to have a full swing
- However, it add capacitance
- Also, it takes away pull down current at X, which creates “ratio” problem



Solution 2: Transmission Gate

- Combination of NMOS and PMOS provides strong transmission on both high and low levels.
- PMOS works when NMOS is weak (i.e. output high) and NMOS works when PMOS is weak (i.e. output low).
- However, this method requires more transistors.





Example: Transmission-Gate Multiplexer

- Transmission gates can be used to build some complex gates very efficiently.
- For instance a simple inverting two-input multiplexer below only uses 6 transistors.