ECE520 – VLSI Design

Lecture 15: Dynamic Logic

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Review of Last Lecture

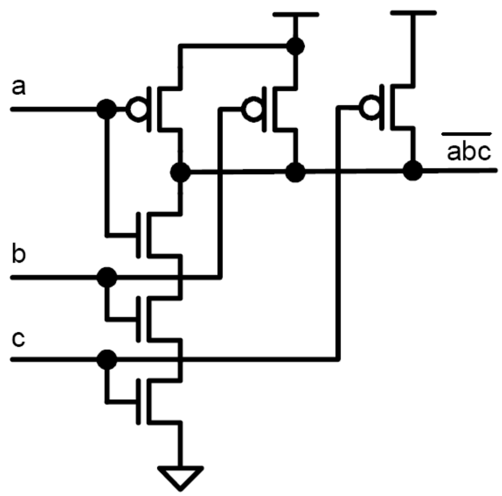
- **Other Types of Static Logic**
  - **Pseudo logic**
  - **Pass-transistor logic**

Today's Lecture

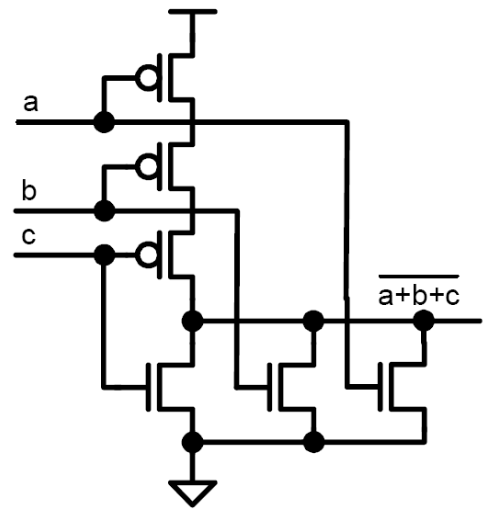
- **Dynamic Logic**
  - **Advantages of dynamic logic**
  - **Problems of dynamic logic**
  - **Fixes to problems in dynamic logic**

Issues with High Fan-in Static Logic

- Large number of devices (2x“fan-in”), which results in large C_L
- Large series stacks, which results in weak drive strength
- Wide devices, which results if large diffusion capacitance
- Large input capacitance, which is load to previous stage
- Large delay mostly due to large load capacitance



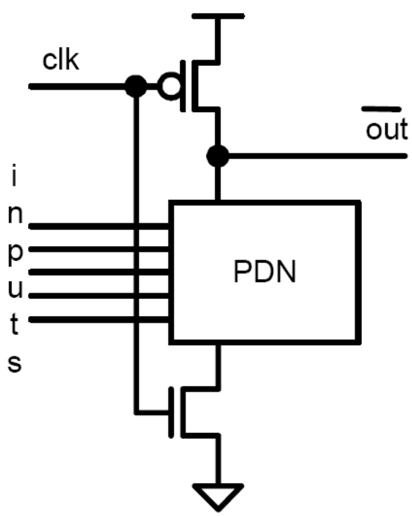
Example1: Static NAND3

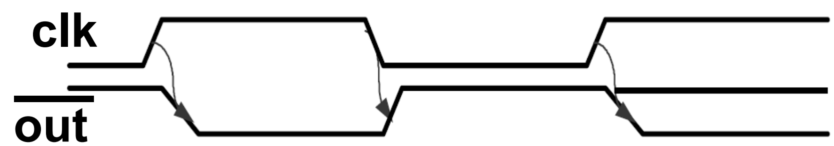


Example2: Static NOR3

Introducing Dynamic Logic

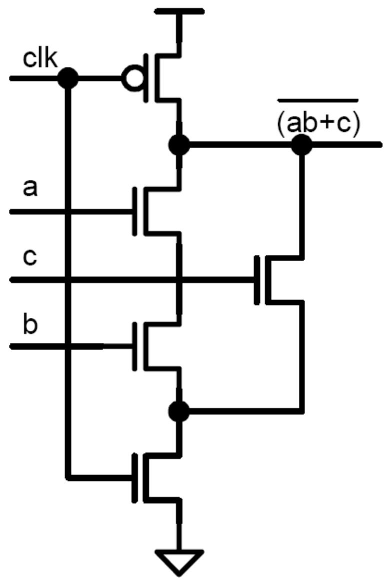
- **Fewer transistors ("fan-in"+2) since only PDN must be implemented**
- **PDN is comprised of NMOS, which is faster than PMOS**
- **t_{PHL} is essentially zero since the output is precharged**
- **Lower input capacitance since only NMOS is driven**
- **Low out put capacitance, which means very fast**





Example: Implementation of a Function

- **Example 1: Dynamic logic of $\overline{AB+C}$**

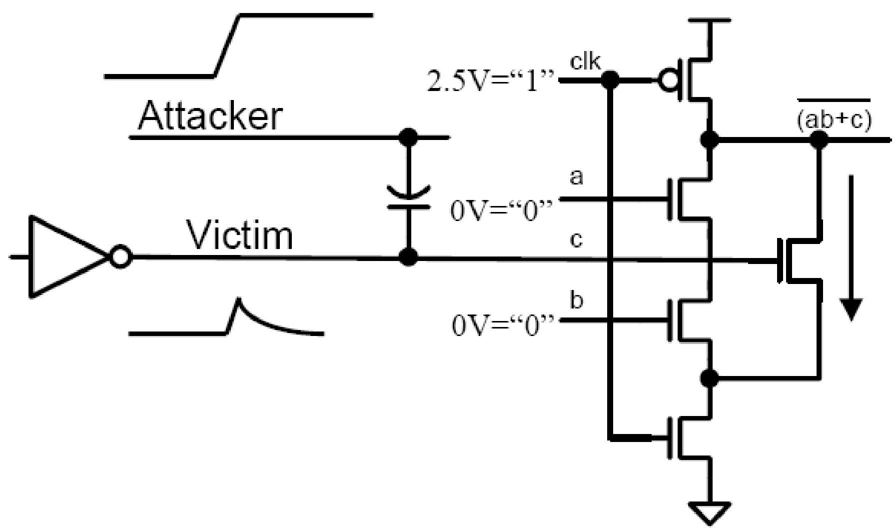


- **Example 2: Dynamic logic of $\overline{(A+B)(C+D)}$**

?

Input Noise (Problem 1)

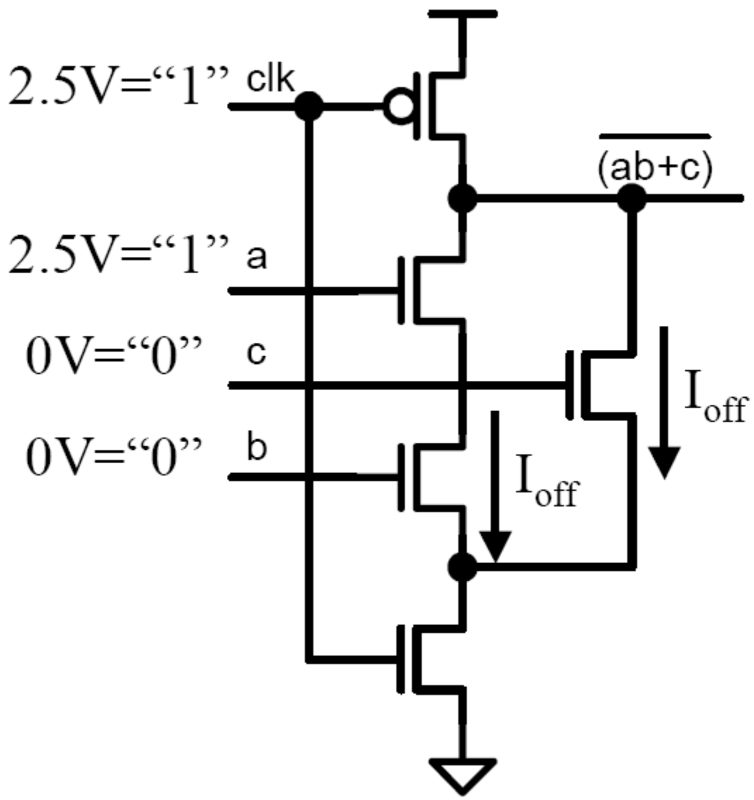
- **The noise margin is very small (V_{TN})**
- **Any glitch to the input can accidentally discharge the dynamic node capacitance**
- **This means input must be strictly stable, no glitch and no coupling noise**



Consider the case where the PDN is again not supposed to pull down. However the C input is subject to Cross-talk from an attacking signal (parallel route that has a $C_{coupling}$ that switches low to high during the evaluate Window).

Leakage (Problem 2)

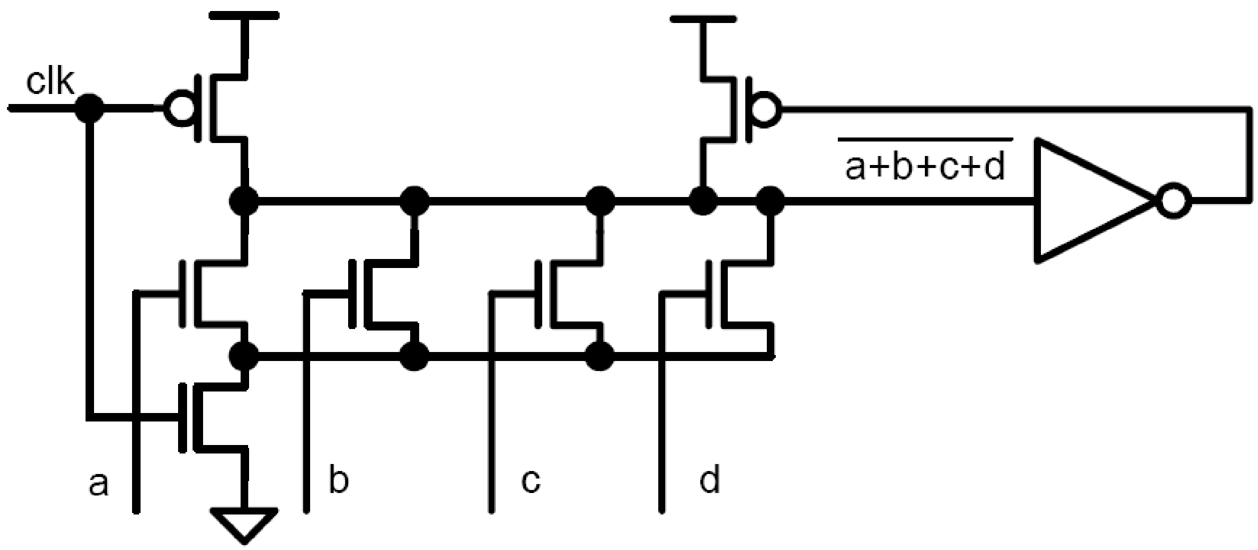
- Consider the case where the gate should not discharge but the clock is very slow (to save power)
- Leakage is even worst in high fan-in NOR



Take the case where we are running with a slow or stopped clock, and we are in the evaluate phase. The inputs to the PDN are such that it shouldn't discharge. However, the devices have sub-threshold current. Therefore, over time sub-threshold leakage in cutoff devices will discharge the output.

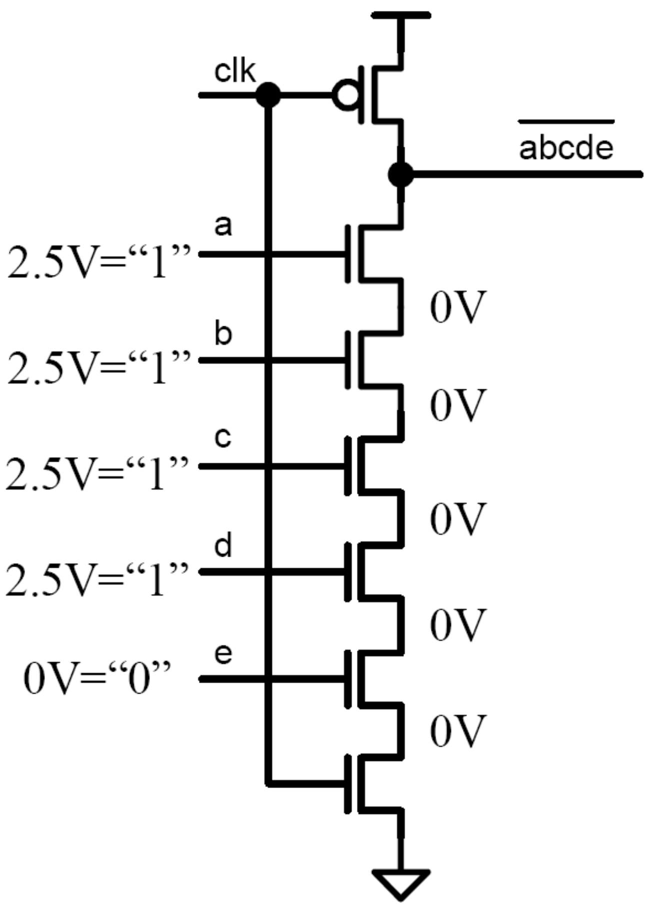
PMOS Keeper (Solution 1&2)

- Adding a PMOS keeper provides sufficient current to keep the I_{off} components from discharging the dynamic node
- This also increases the noise margin in general but slows down the gate



Charge Sharing (Problem 3)

- Charge sharing noise can discharge the output (dynamic) node

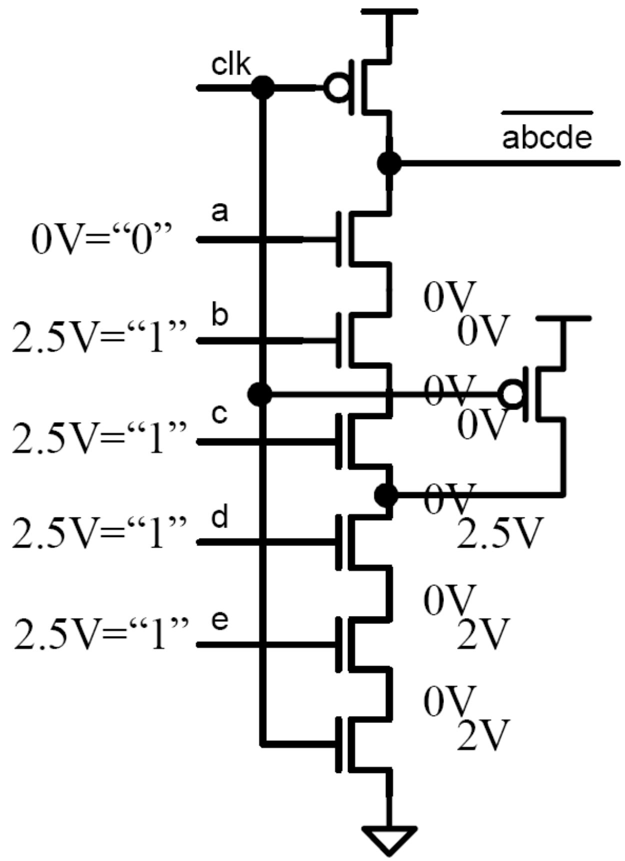


Previous inputs were such that the bottom of the stack was fully discharged. The next set of inputs were such that the output should be "1" but the inputs expose the output to enough diffusion capacitance that the charge sharing allows the output node to discharge anyways (at least to the V_{TH} of the following gate).

How to compute ΔV due to charge sharing?

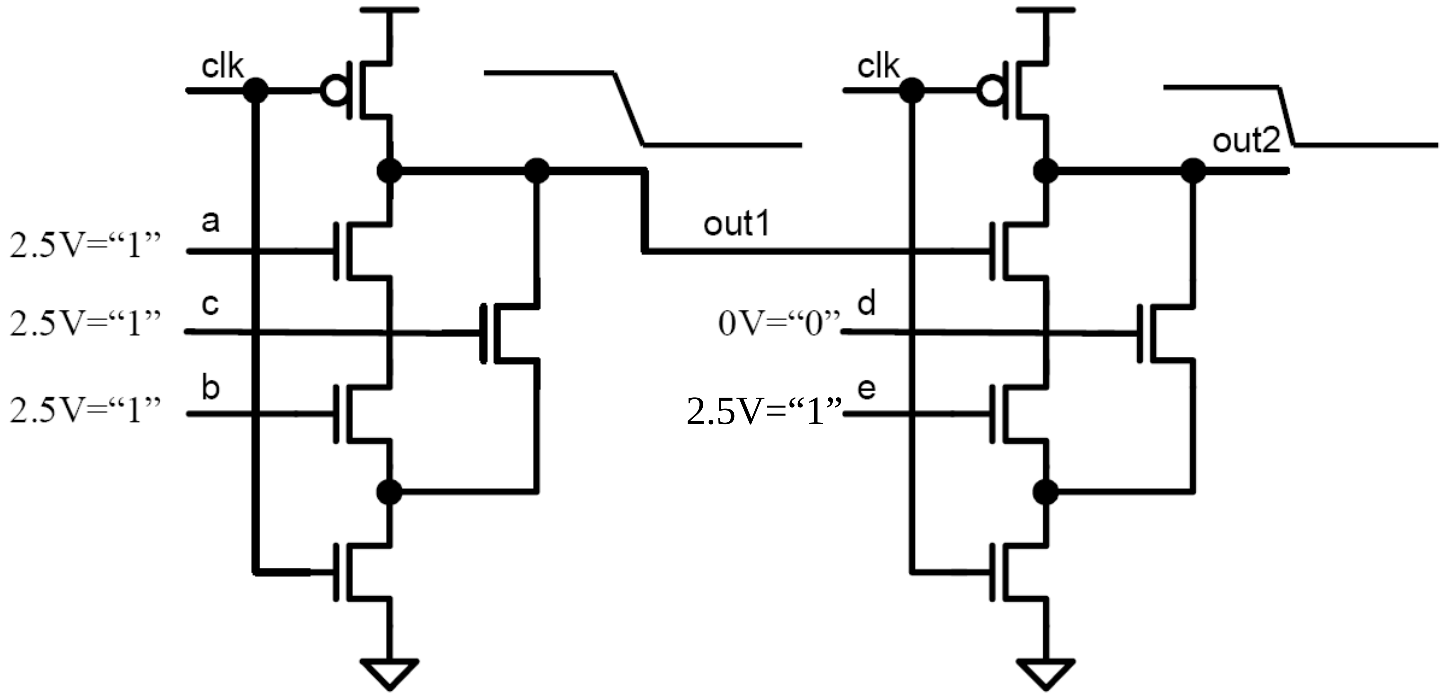
Intermediate Pre-charger (Solution 3)

- **Charge sharing noise can be fixed by intermediate pre-charger**
- **Intermediate pre-chargers are not needed on all of the stack nodes, just enough to allow a favorable capacitance ratio**



Cascading Gates (Problem 4)

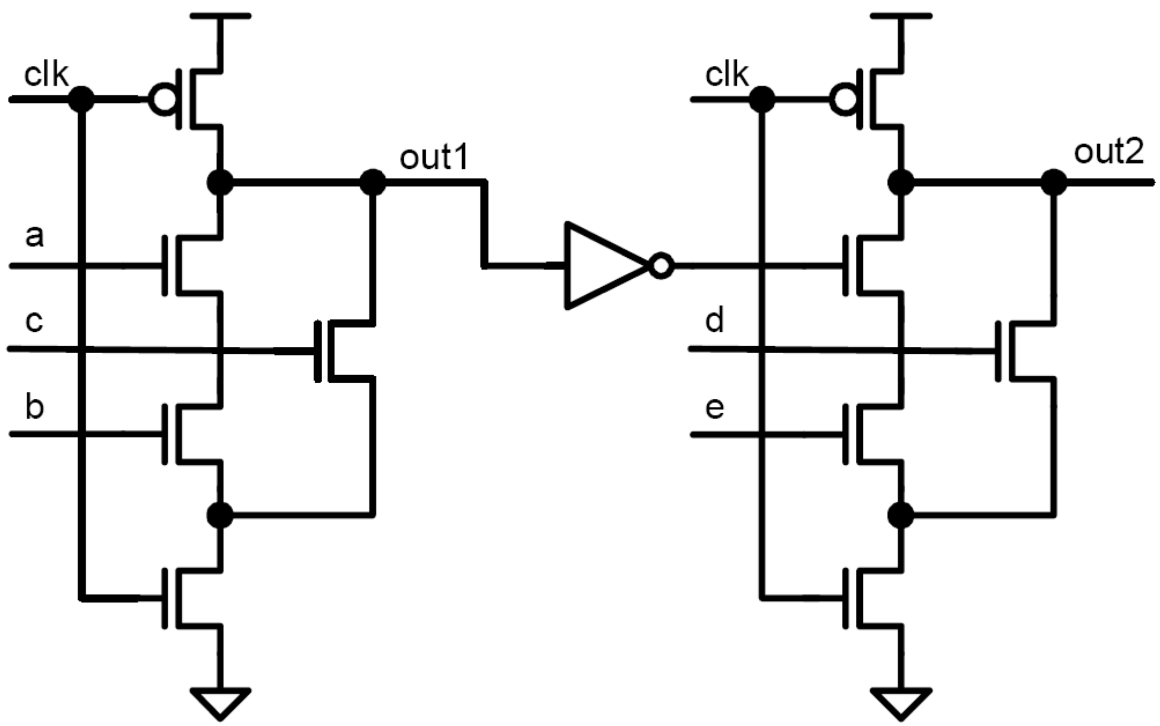
- Domino gates cannot be directly attached to one another
- High to low transition is not allowed at any input



Out1 discharges on the evaluate phase, however it is pre-charged when the evaluate phase begins. Out2 is suppose to stay pre-charged. However since the M1 input (out1) is high during the first part of the evaluate phase is can partially or fully discharge.

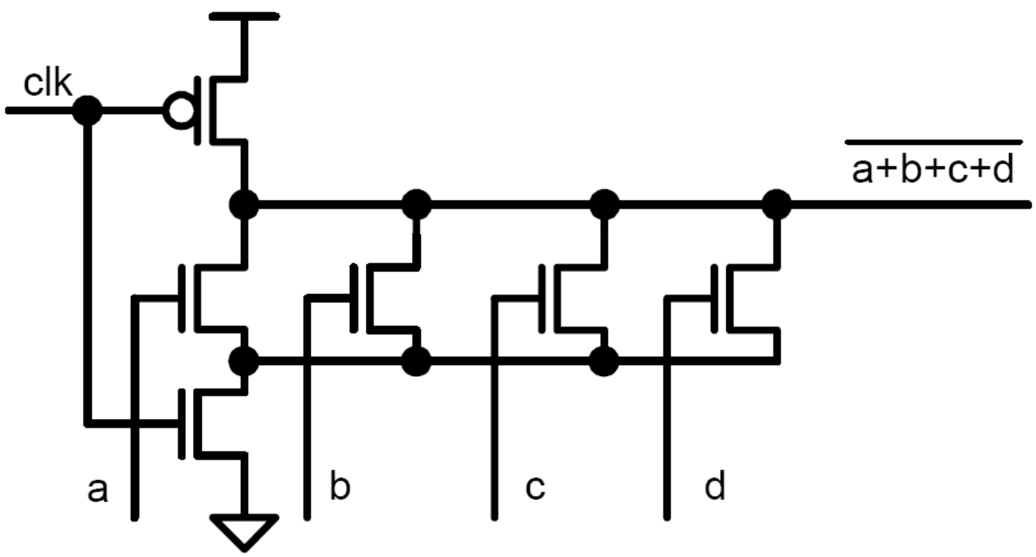
Domino Logic (Solution 4)

- **Cascaded gates must be buffered by static gates. This is called “domino” logic**
- **This eliminates the accidental discharge case by input high-to-low transition but also means that inverting domino gates can’t be built**



High Switching Activity (Problem 5)

- **The clock prechrages every dischrage every cycle (like the clock)**
- **Switching activity of a static NOR4 is 15/256 or about 6%, where switching activity of a dynamic NOR4 is 15/16 or about 94% (why?)**
- **This means that dynamic logic consume higher power than static logic**



Dynamic Logic Summary

- Domino logic provides a circuit style that allows very high fan-in gates to be built
- Advantages:
  - High fan-in
  - High speed
- Disadvantages:
  - Difficult timing constraints
  - Very high power consumption
  - Poor input noise immunity
  - Charge sharing noise can discharge the gate
  - Capacitive coupling can discharge the gate
  - Inverting functions cannot be built