ECE520 – VLSI Design

Lecture 16: Advanced Topics: Power Reduction Techniques

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Review of Last Lecture

- **Dynamic Logic**
  - **Advantages of dynamic logic**
  - **Problems of dynamic logic**
  - **Fixes to problems in dynamic logic**

Today's Lecture

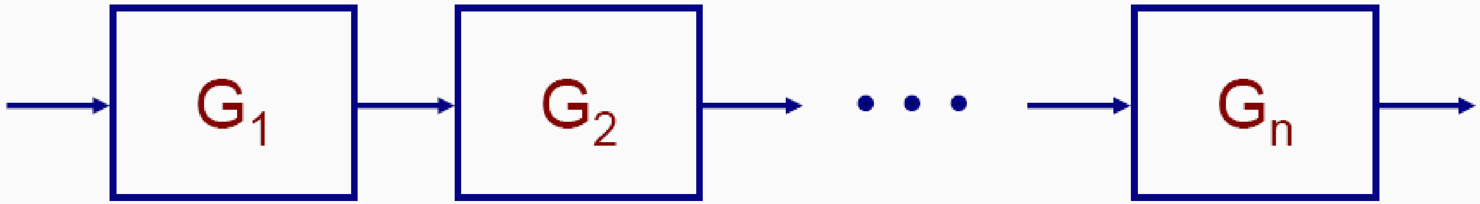
- **Active Power Reduction Methods**
  - **Reduce load capacitance**
  - **Reduce activity factor**
  - **Reduce frequency**
  - **Reduce supply voltage**

Active Power Dissipation Formula

$$P = \left(\frac{1}{2}\right) C V_{DD}^{2} f \alpha$$

- Reducing load capacitance
  - Technology scaling
  - Gate sizing, minimization, interconnect, CAD
- Reducing Switching Activity
  - Architectures
  - Glitch power reduction (15-20%)
- Reducing frequency
- Reducing supply voltage
  - Quadratic impact on power
  - Impact on delay – how to maintain throughput?

Load Capacitance Reduction via Gate Sizing



Increasing transistor sizes (width):

- reduces effective output resistance
  - → reduces time to drive a load
- increases transistor capacitance
  - → slows down previous stage
  - → increases dynamic power

Transistor-Sizing Optimization Problem (given a circuit):

Objective: size all transistors to minimize total power

Constraint: meet timing constraints

Load Capacitance Reduction via Wire Sizing

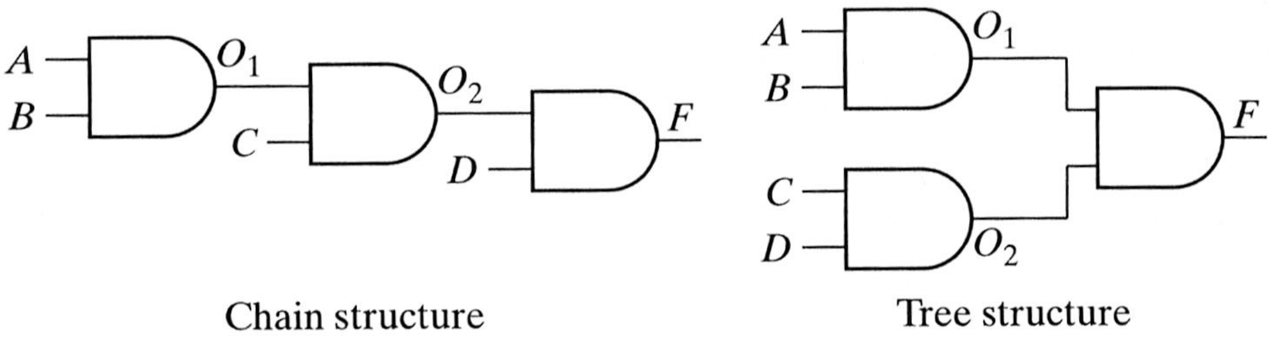
- Increasing wire width / thickness
  - increases capacitance → increases dynamic power
  - reduces resistance → reduces delay
- Increasing spacing between wires
  - reduces capacitance → reduces dynamic power
  - takes more area
    - → causes congestion and increase capacitance somewhere else

Wire-Sizing Optimization Problem (given placed circuit):
Objective: size all wires to minimize total power
Constraint: meet timing constraints

Switching Activity Management

- Logical Optimization
  - Logic restructuring
  - Input reordering
  - Bus coding
- Architectural Optimizations
  - Clock gating
  - Sleep mode

Logic Restructuring for Switching Activity



	O_1	O_2	F
p_1 (chain)	1/4	1/8	1/16
$p_0 = 1\text{-}p_1$ (chain)	3/4	7/8	15/16
$p_{0\text{->}1}$ (chain)	3/16	7/64 (0.1094)	15/256
p_1 (tree)	1/4	1/4	1/16
$p_0 = 1\text{-}p_1$ (tree)	3/4	3/4	15/16
$p_{0\text{->}1}$ (tree)	3/16	3/16 (0.1875)	15/256

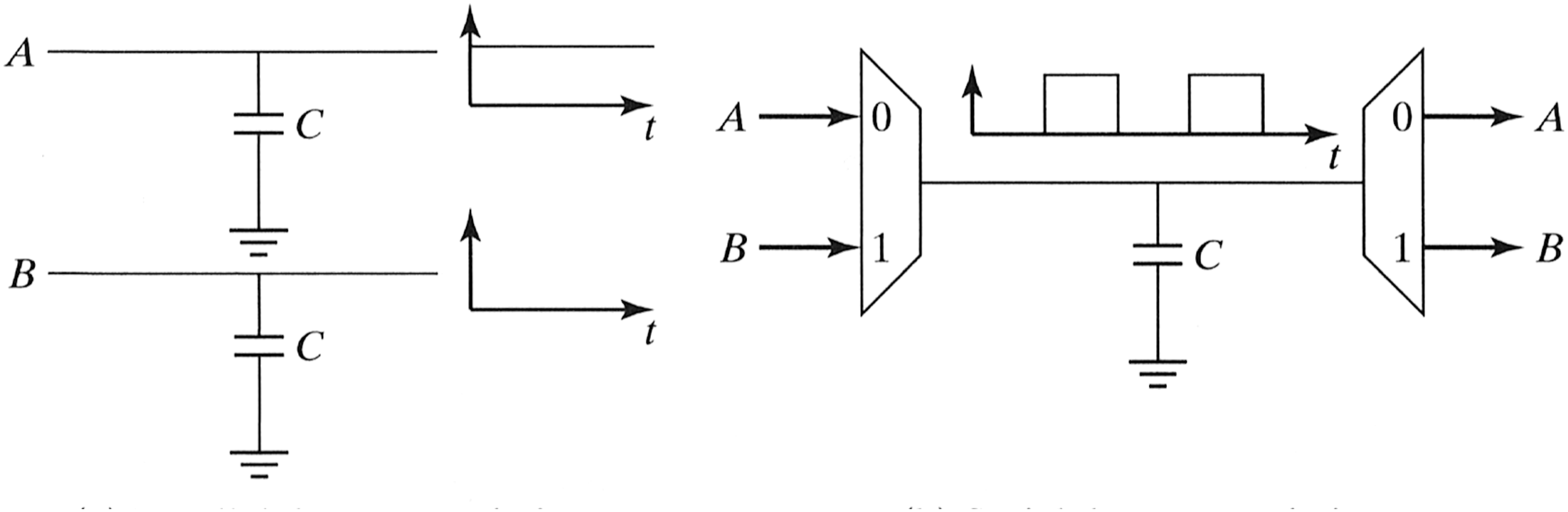
Logic Restructuring for Glitch

Logic restructuring to minimize spurious transitions

Buffer insertion for path balancing

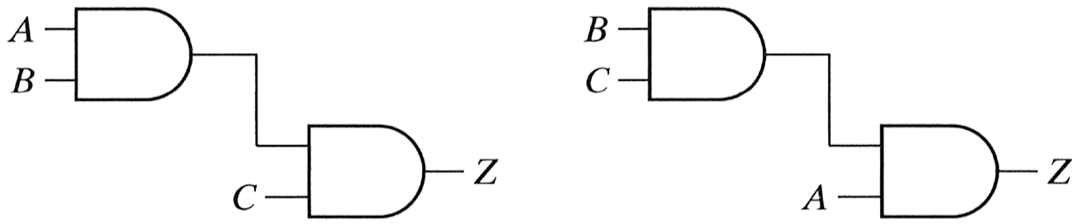
Resource Sharing can Increase Activity

- Parallel versus time-multiplexed data busses



Input Reordering for Switching Activity

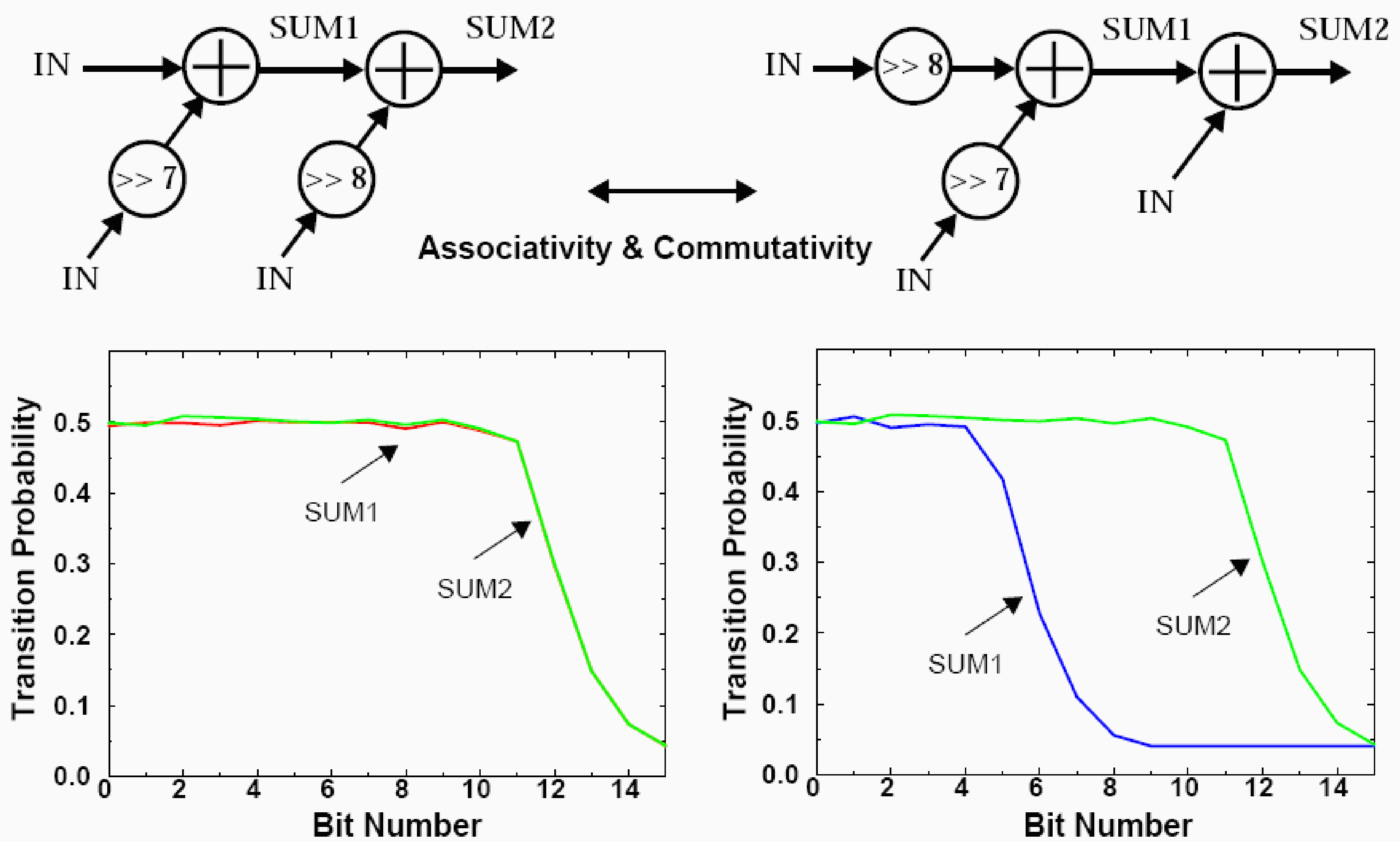
- Reordering of inputs affects the circuit switching activity



$p_{(A=1)} = 0.5$
$p_{(B=1)} = 0.2$
$p_{(C=1)} = 0.1$

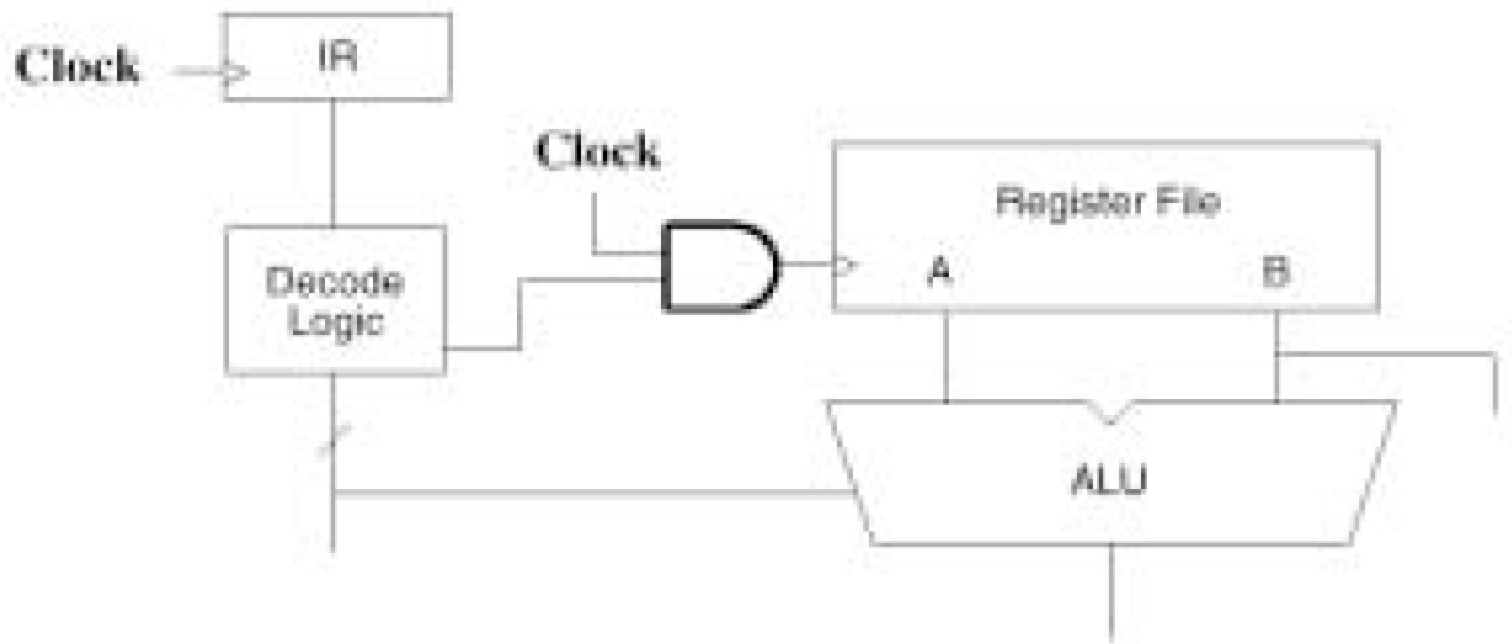
- Which circuit have lower switching activity?

Another Example of Input Reordering



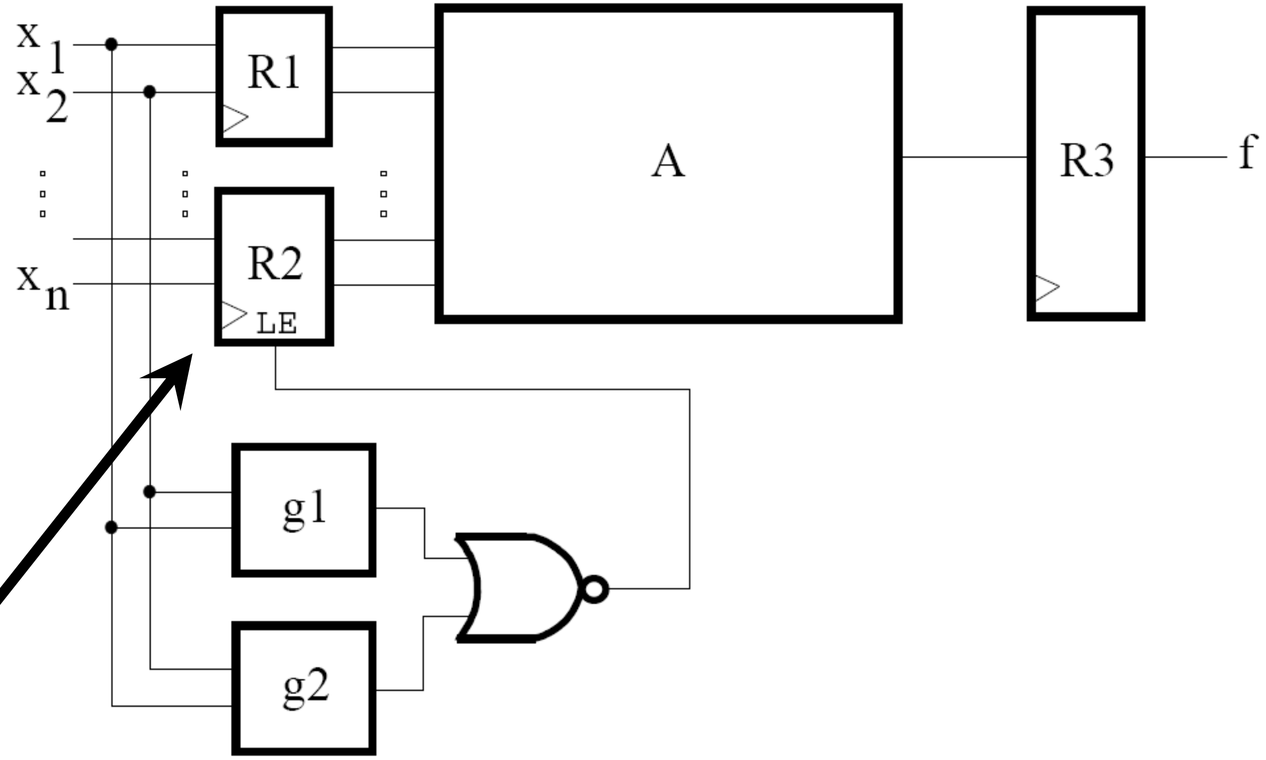
- 30% reduction in switching energy

Clock Gating



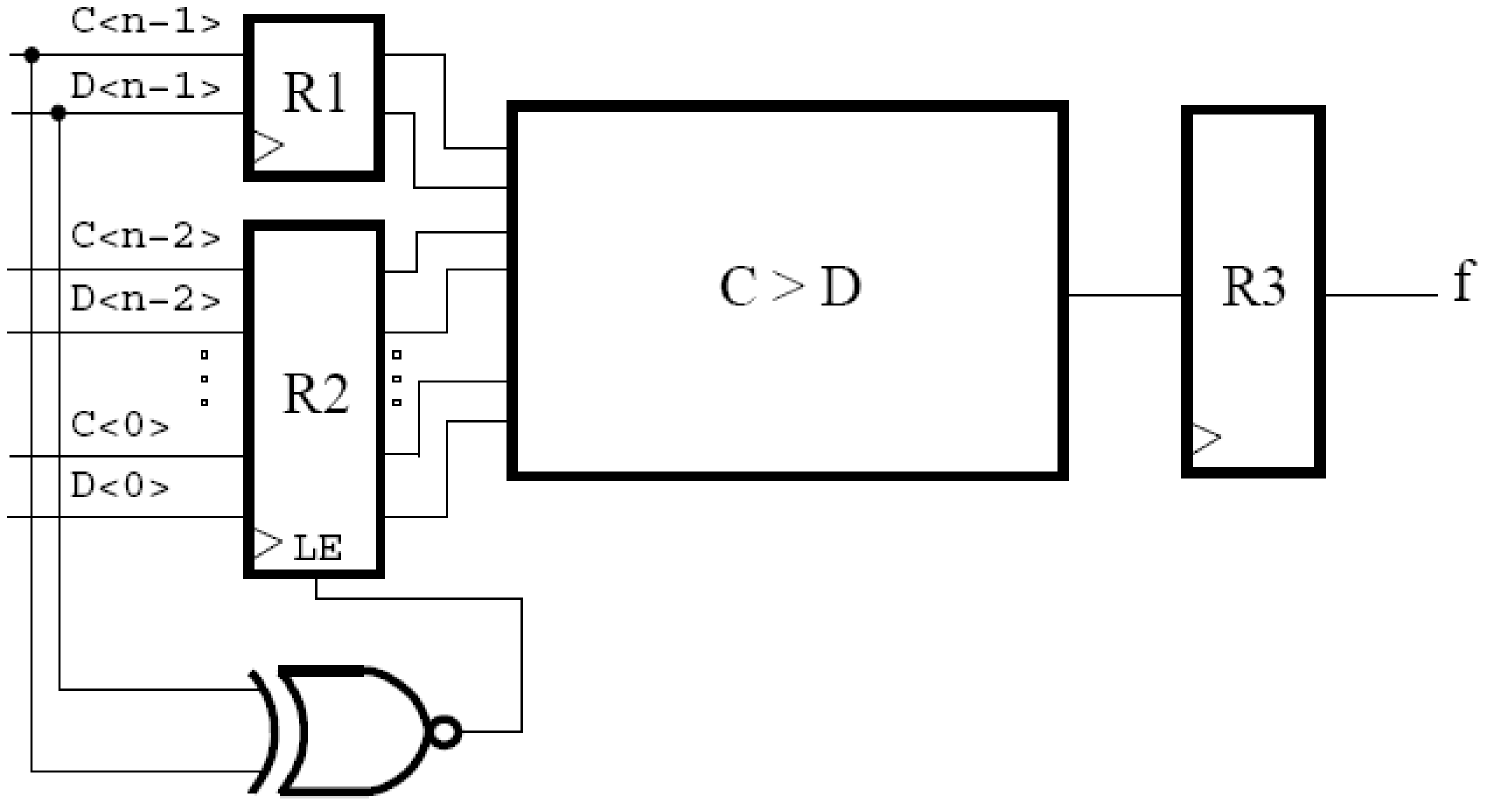
Requires careful skew control ...
Scary in current logic synthesis world!

Pre-Computation Technique



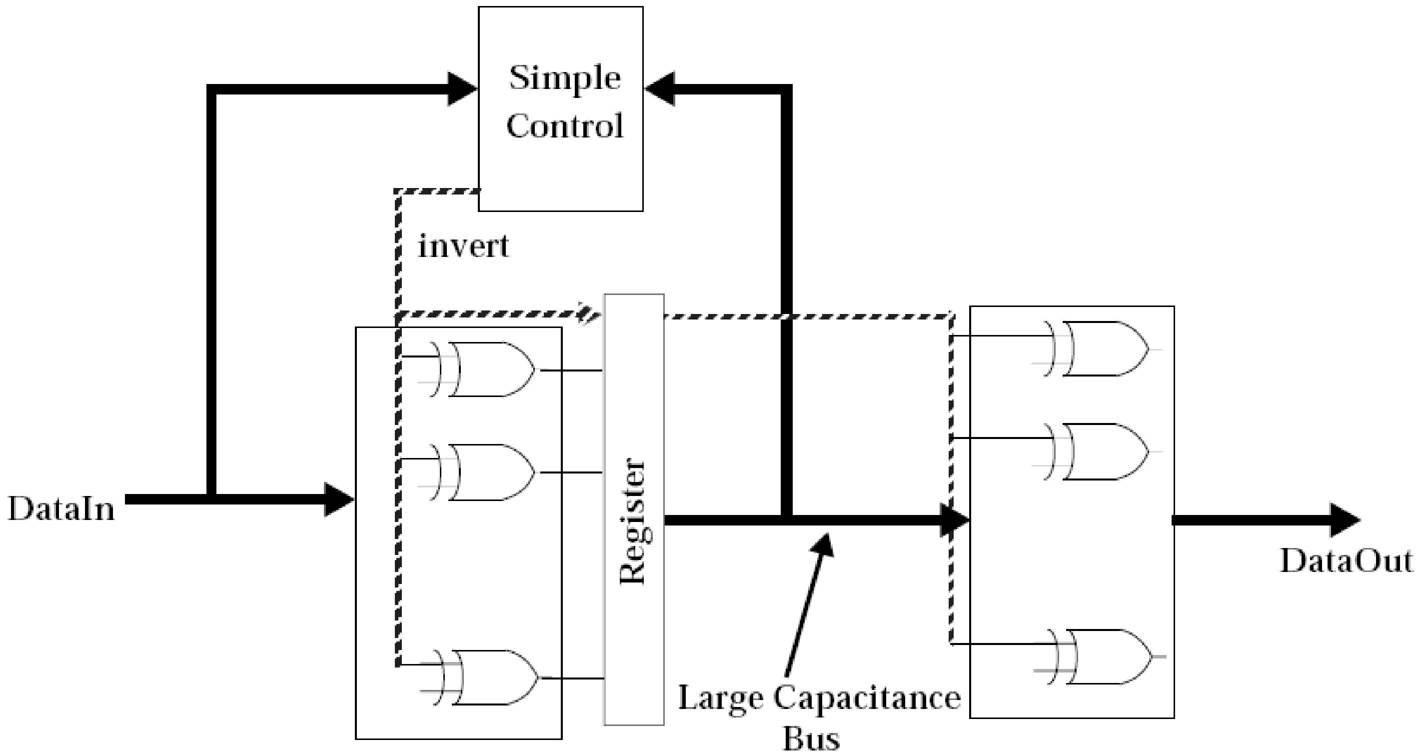
Inputs x_i … x_n are not applied
If pre-computing holds

Pre-Computation Example: Comparator



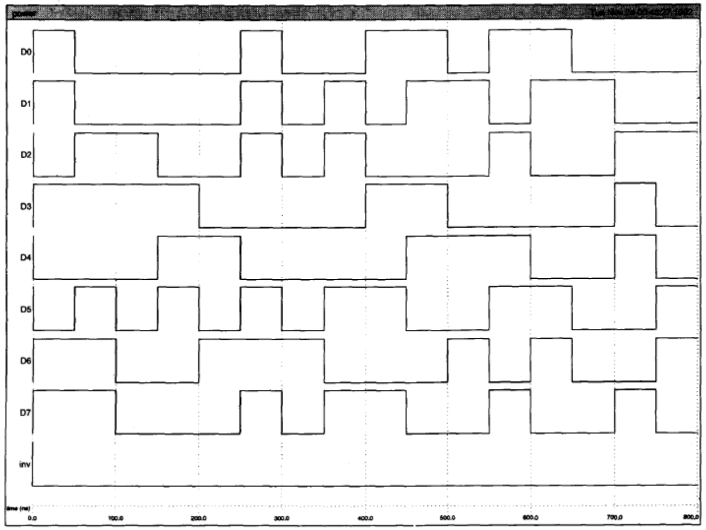
Circuit-Level Activity Encoding for I/O

- Conditional Inversion Coding for Interconnect – Reduces switching transition using coding

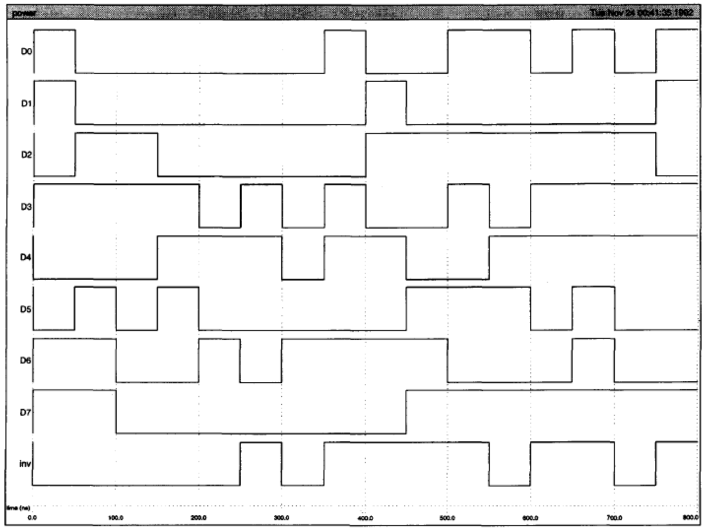


from [Stan94]
(*1994 International Workshop on Low-power Design*)

Activity Encoding Example

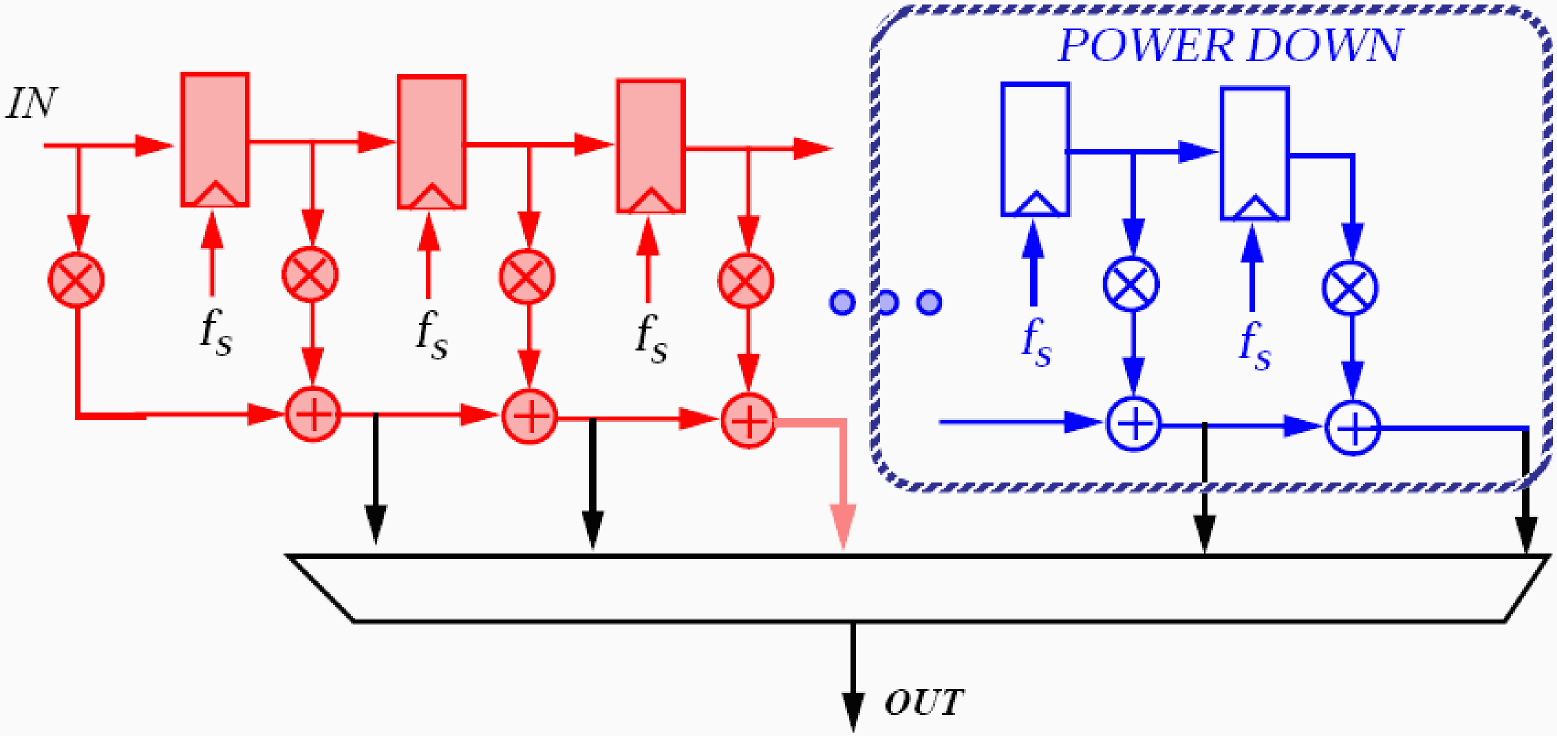


A typical 8-bit data bus
There are 64 transitions



Coded 8-bit data bus
There are 53 transitions

Eliminate Redundant Computations

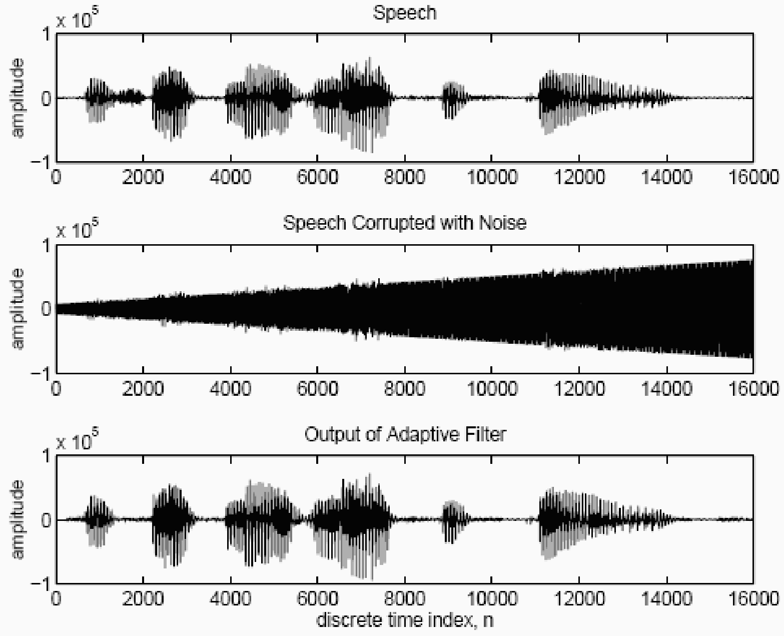


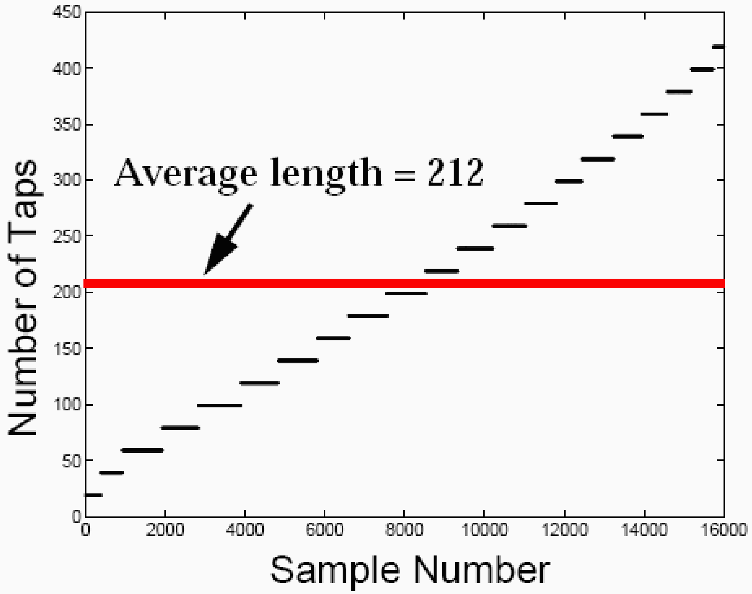
- Dynamically vary the number of operations per sample.

Trade power consumption and filter quality

from [Ludwig95]
(CICC95)

How much power reduction is possible?



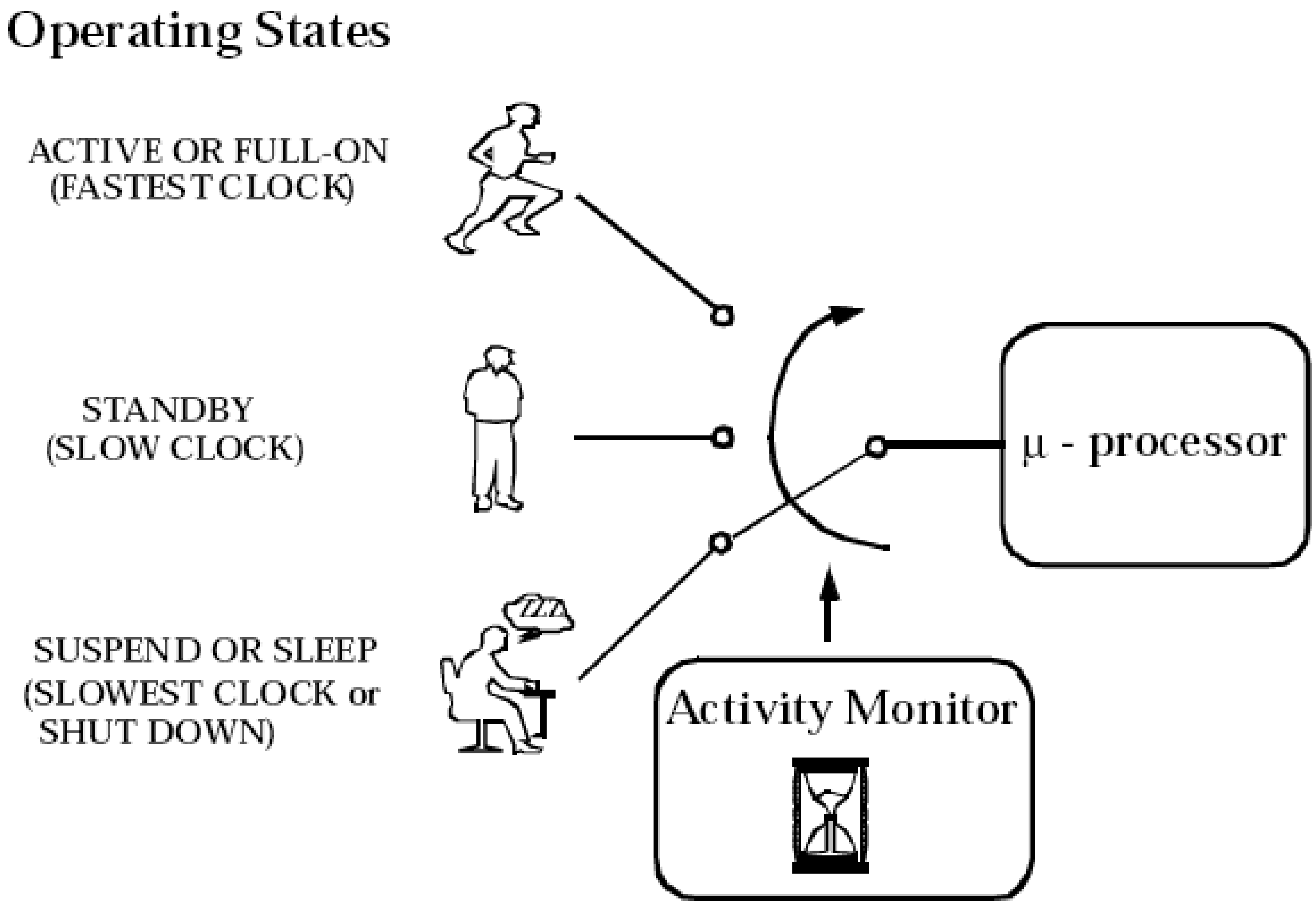


$$\text{Switched Capacitance Reduction} \approx \frac{\text{Peak Number of Operations}}{\text{Average Number of Operations}}$$

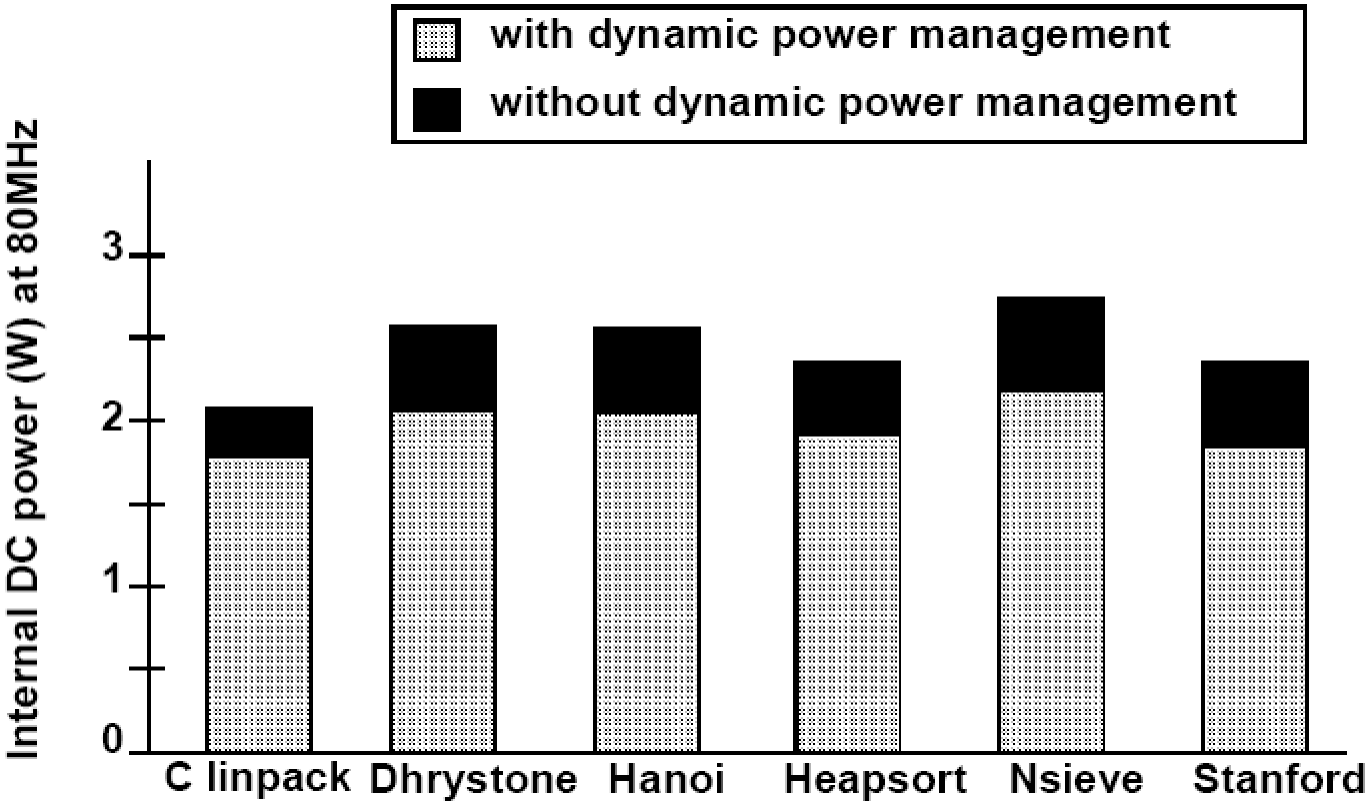
$$\approx 2$$

Strong Function of Signal Statistics

Frequency Reduction via Power-Down



Microprocessor Dynamic Power Management



PowerPC 603