ECE520 – VLSI Design

Lecture 18: Timing Issues

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Review of Last Lecture

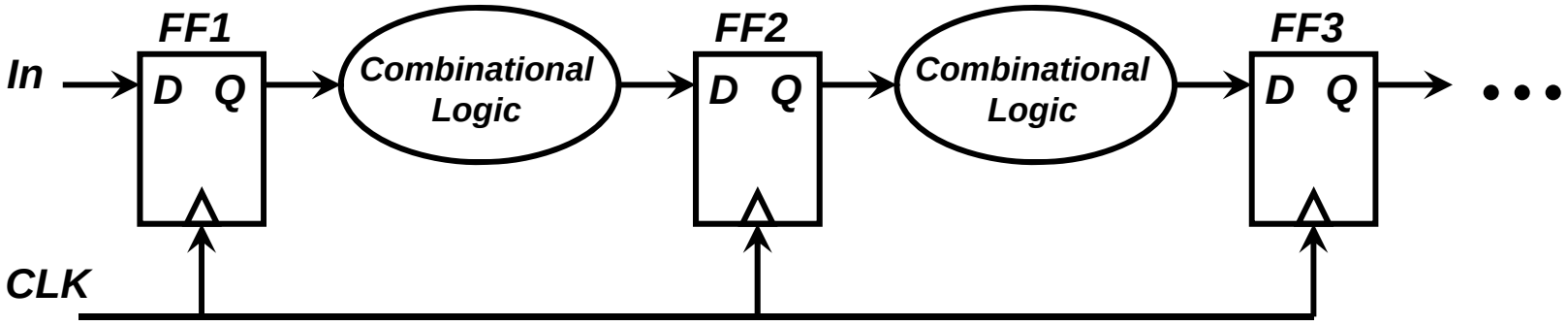
- **Sequential Logic**
  - **Latches and Flip-Flops**
  - **Timing Characteristics**
  - **Design of Latches and Flip-Flops**
  - **Setup and Hold Time Issues**

Today's Lecture

- **Timing Issues**
  - **Critical Path**
  - **False Path**
  - **Clock Skew**
  - **Clock Jitter**

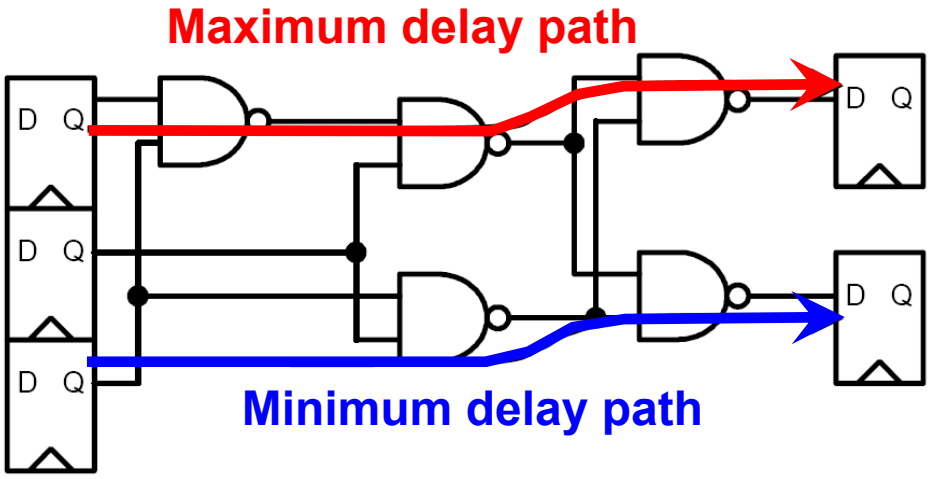
Pipelined Data path Circuit

- Flip flops synchronize data at each pipe stage start and finish
- Logic between them is combinational
- Since each stage begins and ends on a clock edge we can divide and conquer to determine the system timing
- This is called “timing analysis”



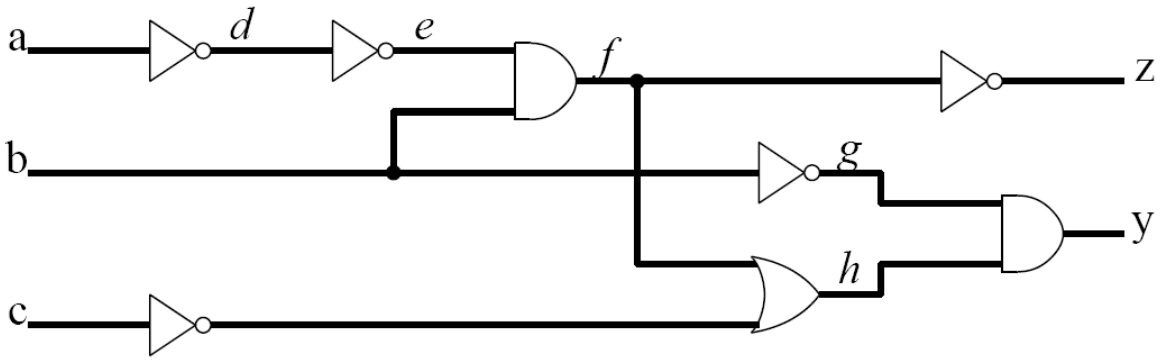
Timing Analysis

- Measure each path through the logic between FF's
- We really only care about the longest path, called maximum delay for setup
- Similarly, we only care about the shortest path, called minimum delay (or contamination delay) for hold
- The path that gives the maximum delay on the whole chip is called "critical path"



False Path

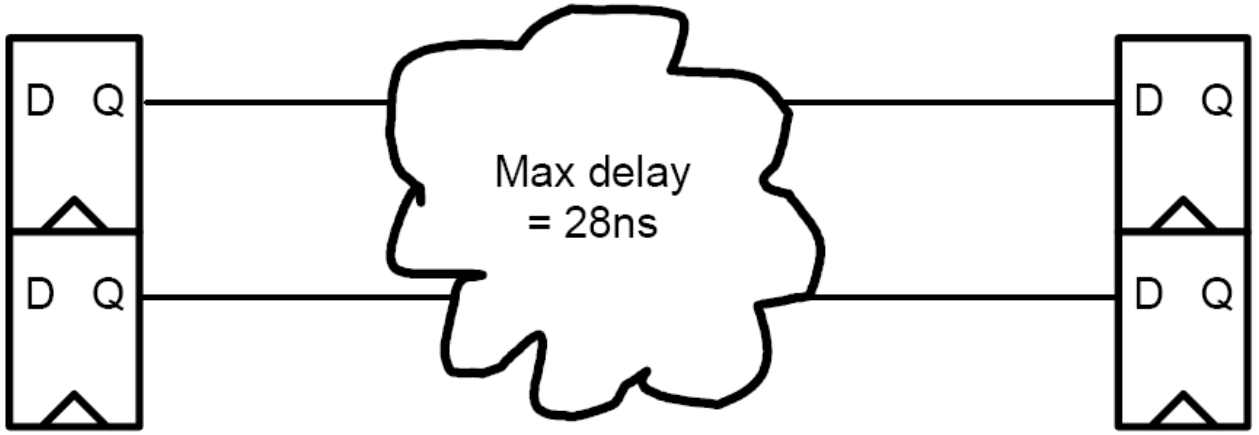
- Be careful! If a critical path cannot be exercisable, it is a "false path".
- In this case, you have to continue your search for maximum delay path that is exercisable.
- In general, finding "false path" is not easy and requires function evaluation
- Example: What is the minimum and maximum delays in this circuit?



gate	delay
NOT	2
AND	4
OR	4

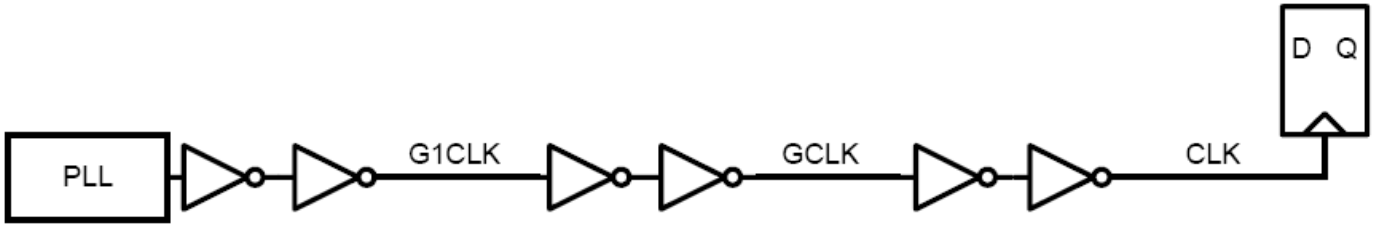
Minimum Clock Period

- Don't forget to consider delay of flip flops (setup, C2Q, and hold time) in maximum delay computation
- Example: Assuming that the setup time is 1ns, hold time is 1ns, and C2Q delay is 2ns, what is the minimum clock period? Why?



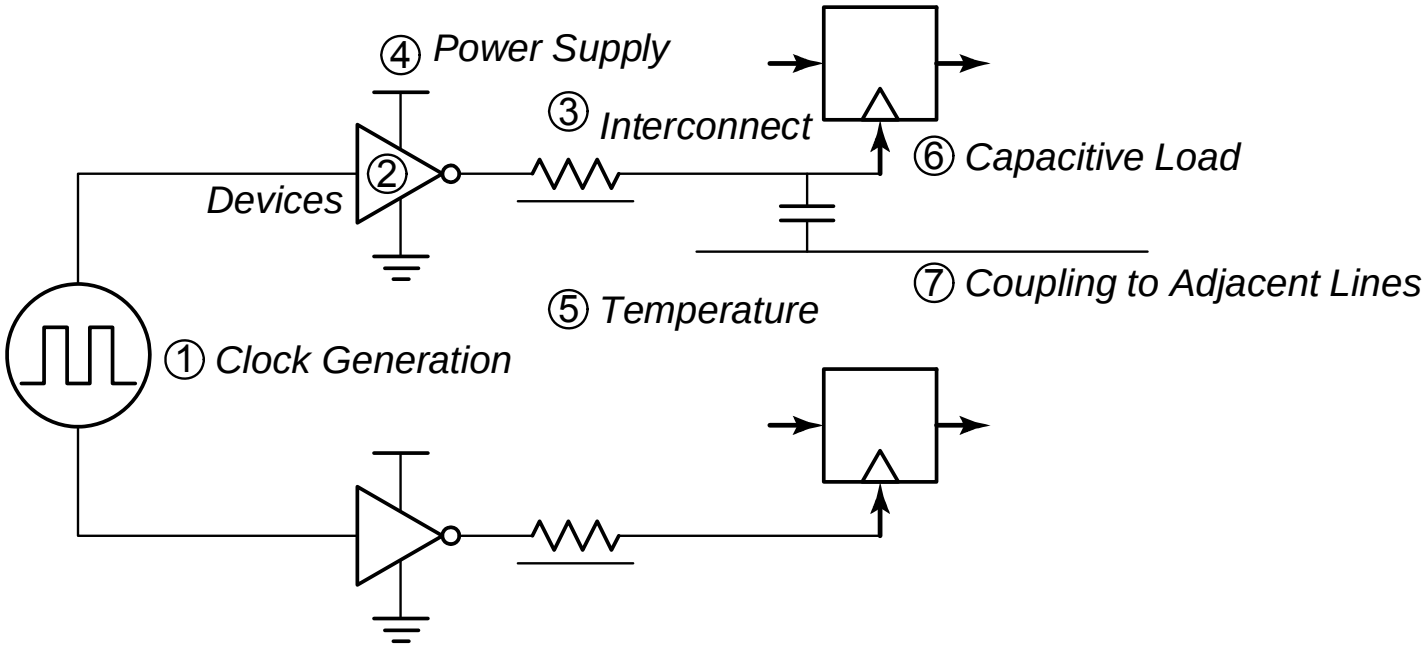
Generating Clocks

- Clocks are usually generated at a single origin
- A phase locked loop (PLL) is generally used to generate a high quality clock for the chip
  - Phase locked with the outside reference clock
  - PLL's can multiply the reference clock speed
  - E.g., T_{REF} = 10ns (100MHz), T_{CLK} = 1ns (1GHz)
- The clock must then be driven through many stages to generate enough drive strength to drive all the flip flops and latches on the chip
  - These can number in the 100's of thousands
  - Large equivalent load - add the gate widths of transistors in "clk" path
  - Usually the widest transistors are clock drivers



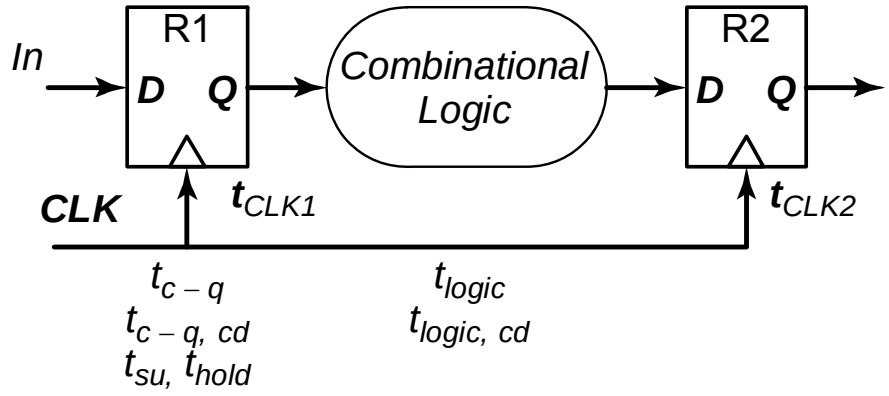
Clock Uncertainty

- **Clock skew**
  - **Spatial variation in temporally equivalent clock edges; includes: deterministic + random**
- **Clock jitter**
  - **Temporal variations in consecutive edges of the clock signal; includes: modulation + random noise**



Clock Skew and Setup Time Constraint

- Worst case is when receiving edge arrives early (positive δ)
- Maximum delay is impacted since a clock cycle can be shorter than ideal
  - Simply subtract the expected clock skew and jitter from the cycle time when designing
  - A failure here is not too bad: It means that you missed a setup time
  - The part is then "slow"—It will still work at a reduced clock rate

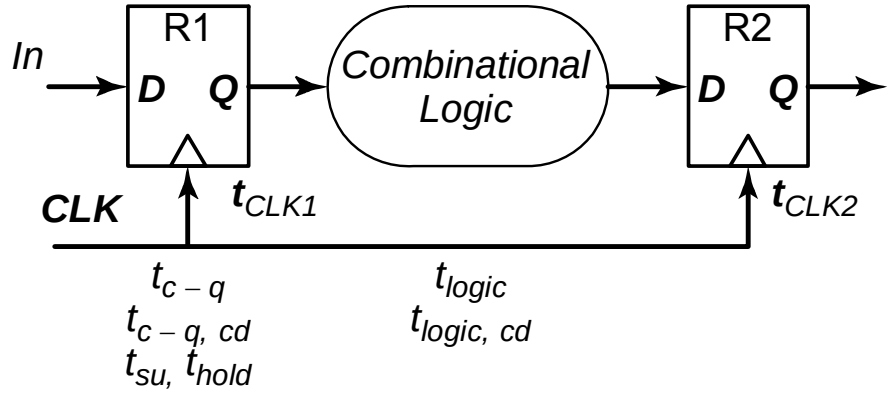


Minimum cycle time:

$T - \delta = t_{c\text{-}q} + t_{su} + t_{logic}$

Clock Skew and Hold Time Constraint

- Worst case is when receiving edge arrives late, (positive δ)
- Minimum delay is impacted since a receiving clock edge can be later than ideal
  - Means that the hold time at the receiving latch is more easily violated
  - A failure here is pretty much catastrophic
  - Since skew is built-in, there is nothing you can do post-silicon to fix it!
  - It is generally worth-while to add more design guard-band (margin) to your min-delay timing!

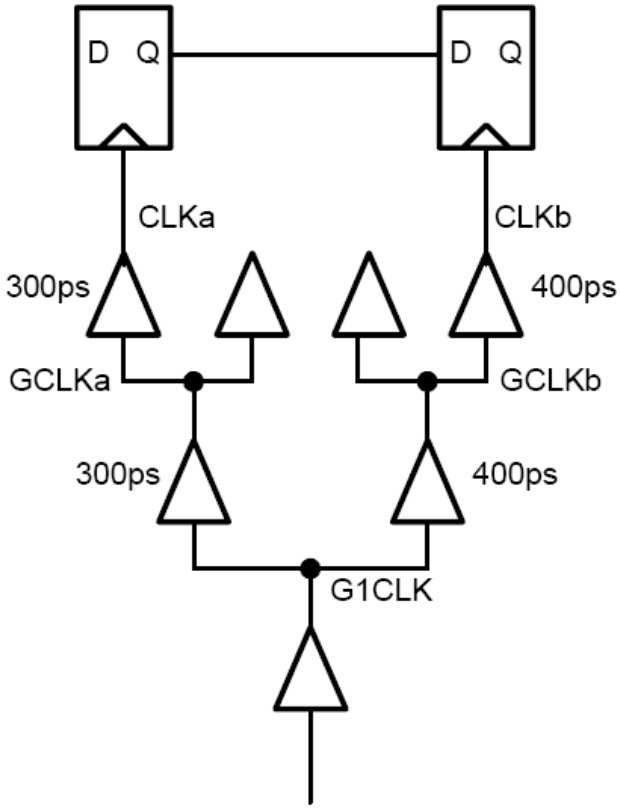


Hold time constraint:

$$t_{(c\text{-}q,\ cd)} + t_{(logic,\ cd)} > t_{hold} + \delta$$

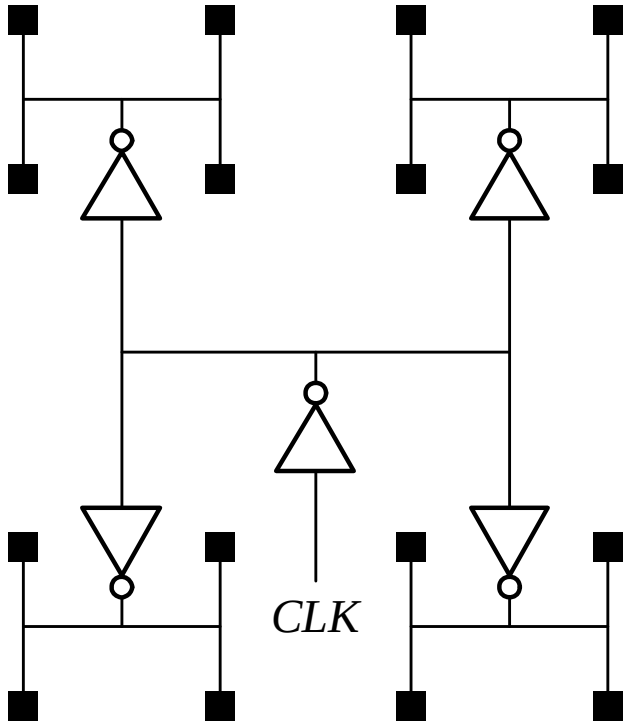
Example: Effect of Clock Skew

- Assume t_{C2Q} = 350ps and T_{hold} = 100ps. What happens?
- Assume t_{C2Q} = 150ps and T_{hold} = 100ps. What happens?



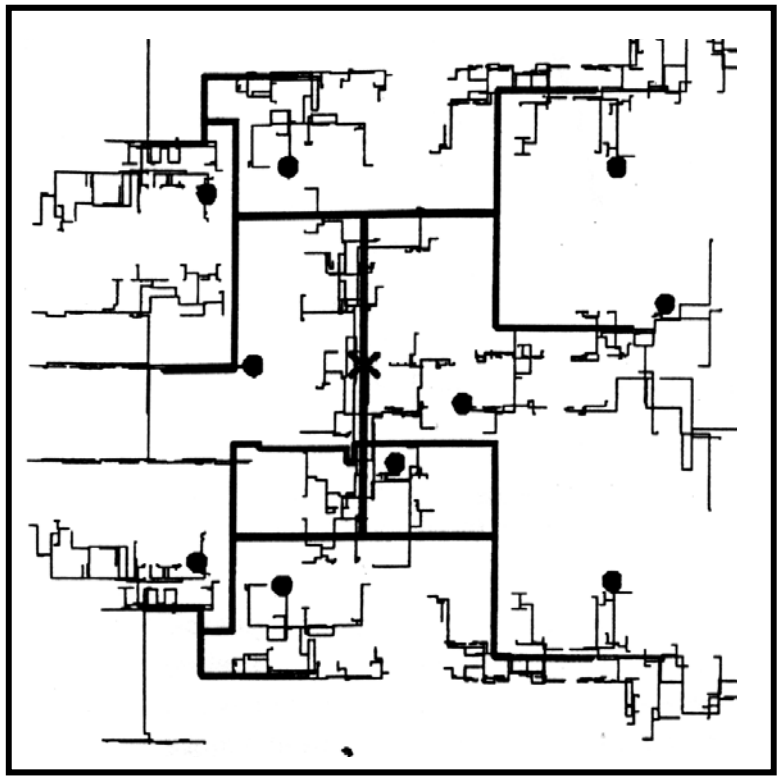
Clock Distribution Design: H-Tree

- Most common type of clock distribution is balanced H-Tree
- The balancing is to keep the CLK timing at the end point the same
- The clock must then be driven through many stages to generate enough drive
- Each driver is subject to variation due to systematic (process) or local environment (V_{DD}, Temp, or C_L) variations



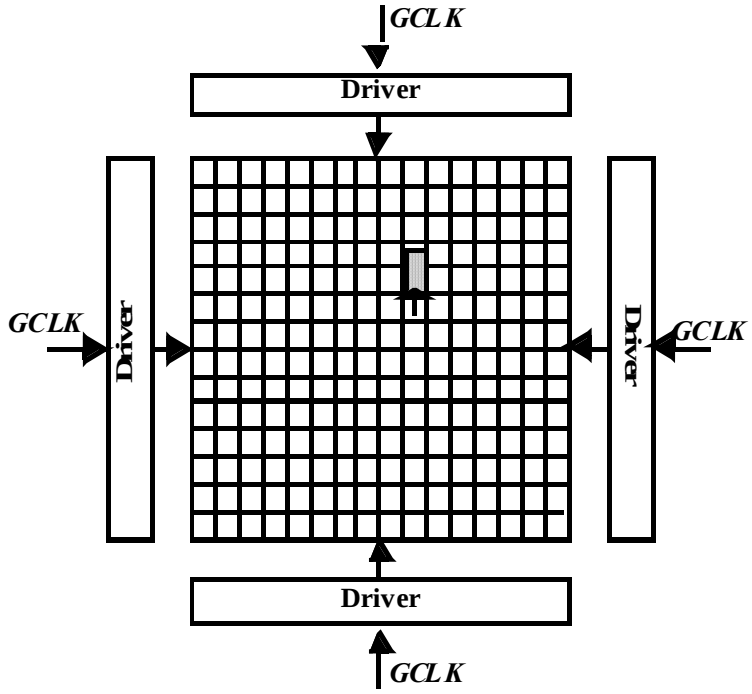
Clock Distribution Design: Balanced-Tree

- True H-tree clock routing is often not possible.
- In this case, the clock distribution designer balances the length of each clock branch to reduce skew as much as possible.

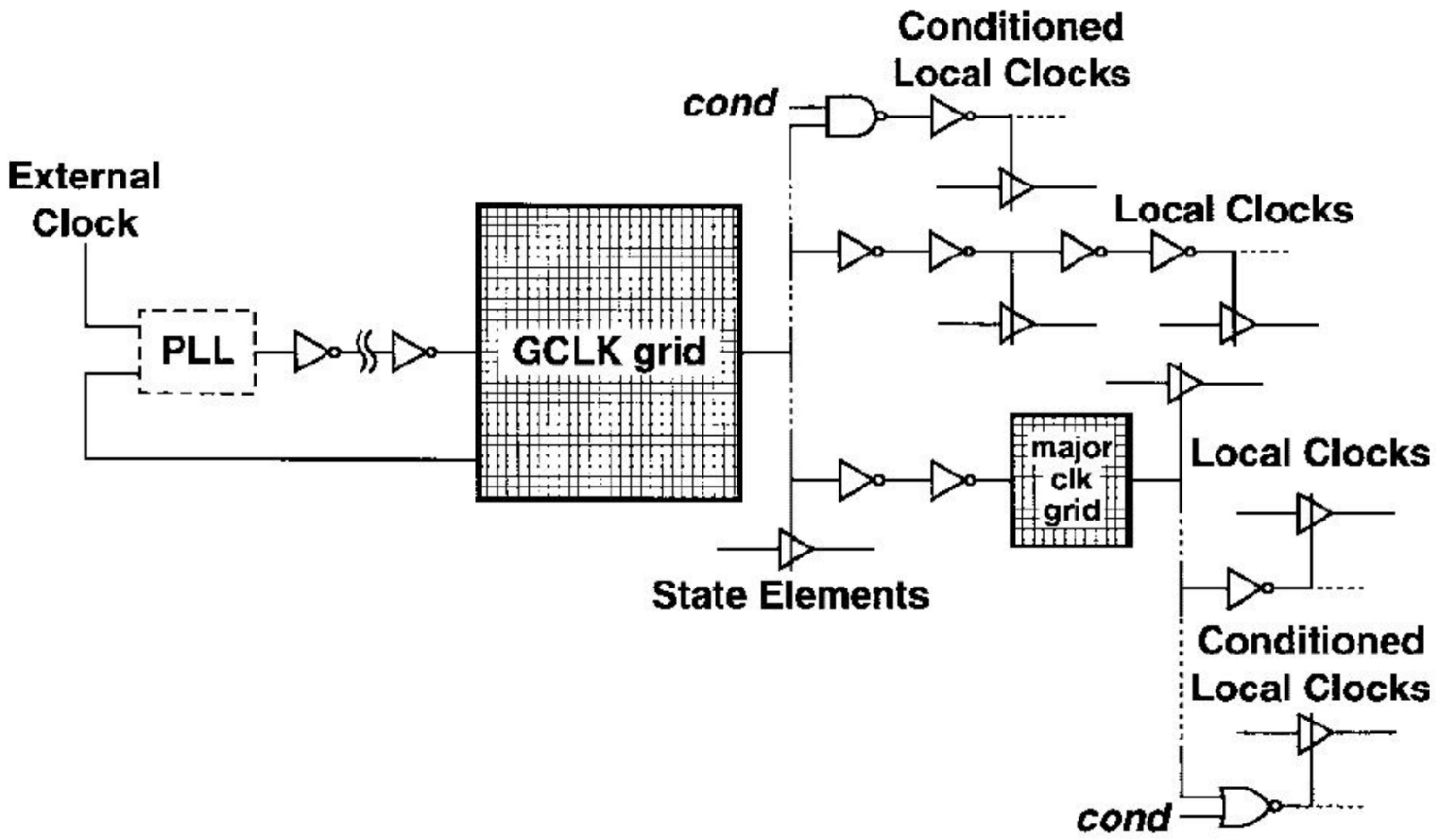


Clock Distribution Design: Mesh Clock

- Mesh clock distribution is used in some high end processor
- They often provide less clock skew
- They often consume some wiring resources
- They use a lot of power to drive all that metal load capacitance



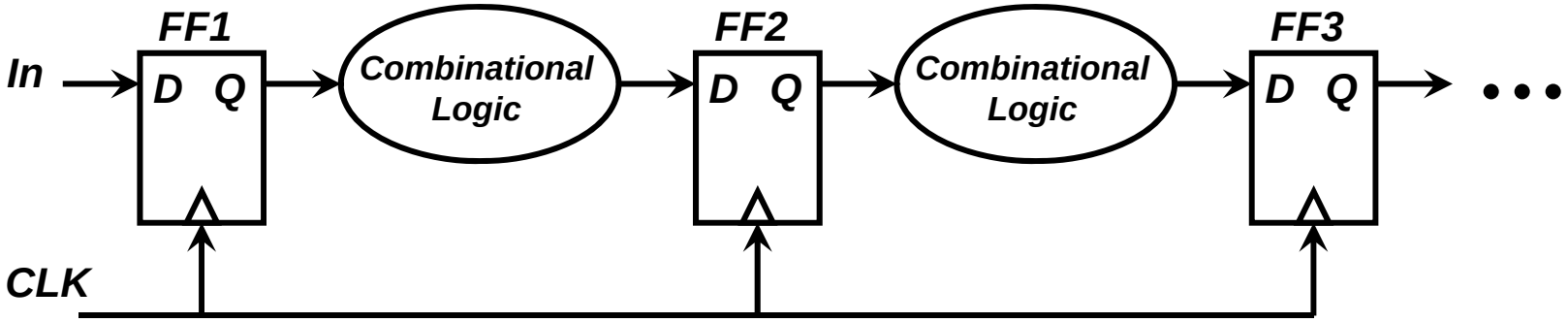
Clock Distribution Design: Hybrid Clock



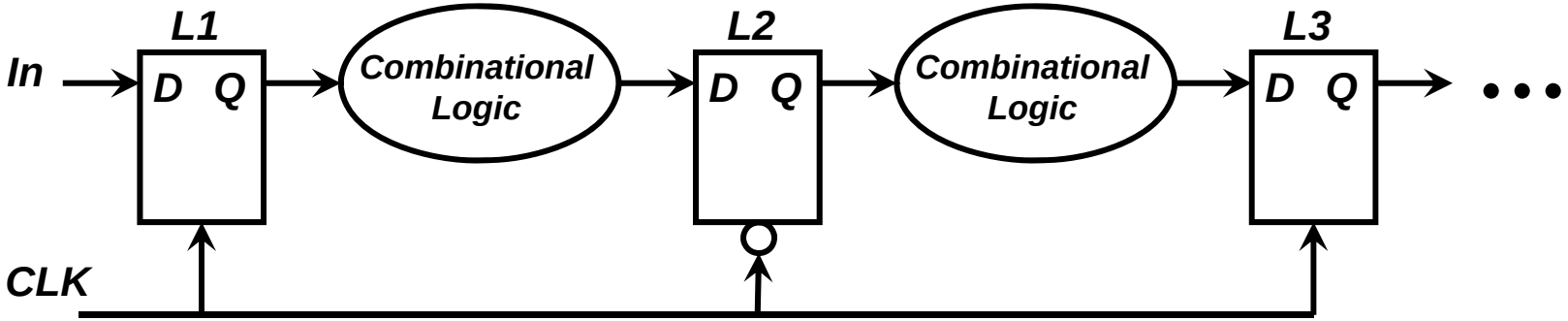
Clock Hierarchy for the Alpha 21264 Processor

Flip-Flop versus Latch-Based Clocking

Flip flop Clocking

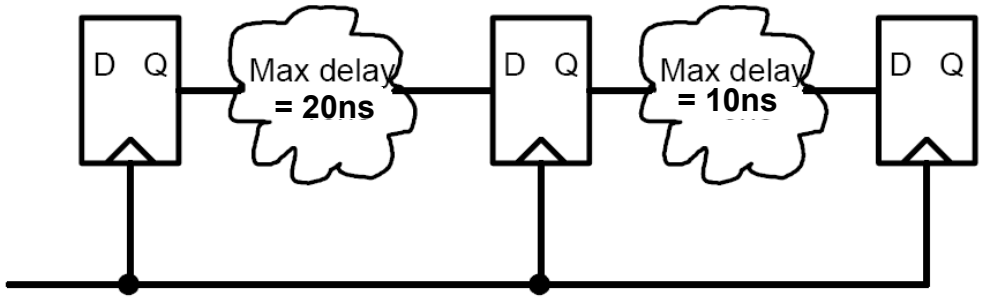


Latch-Based Clocking (Time Borrowing)



Example: Time (Slack) Borrowing

- Assume $t_{C2Q} = T_{su} = 0$. How fast is this path?



- Assume $t_{C2Q} = T_{su} = 0$. How fast is this path?