ECE520 – VLSI Design

Lecture 19: Clock Distributions - PLL

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

Review of Last Lecture

- **Timing Issues**
  - **Critical Path**
  - **False Path**
  - **Clock Skew**
  - **Clock Jitter**

Today's Lecture

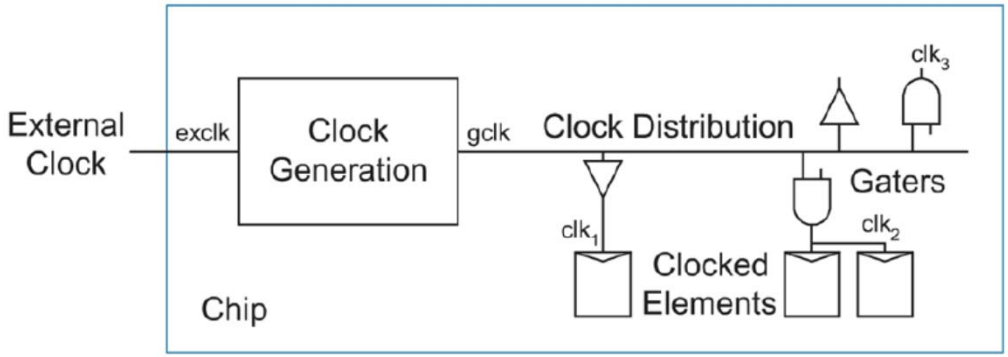
- **Clock Distribution Network**
  - **Clock generation (PLLs)**
  - **Clock distribution**
  - **Clock gaters**

Physical Clock

- **Distributing a single clock across a chip is challenging**
- **Distributing more than one clock signal is almost impossible**
- **Most systems distribute a single GLOBAL CLOCK even if the system needs multiple logical clocks**
- **Local clock gaters located close to the clocked elements produce the actual physical clocks and drive the clock to the elements along short wires**
- **Clock gaters are:**
  - **Buffers**
  - **AND gates for clock gating**
  - **Inverters to produce complementary clocks**
  - **Pulse generators for pulsed latches**

Clock System Architecture

- IC receives an external clock signal through the I/O pads
- The clock generation unit adjusts the phase and/or frequency of the global clock by either
  - Phase-locked loop (PLL)
  - or Delay-locked loop (DLL)
- The generated global clock is then distributed to points near all of the clocked elements via a clock distribution network
- Local gaters receive this global clock and drive the physical clock signals along short wires to small groups of clocked elements

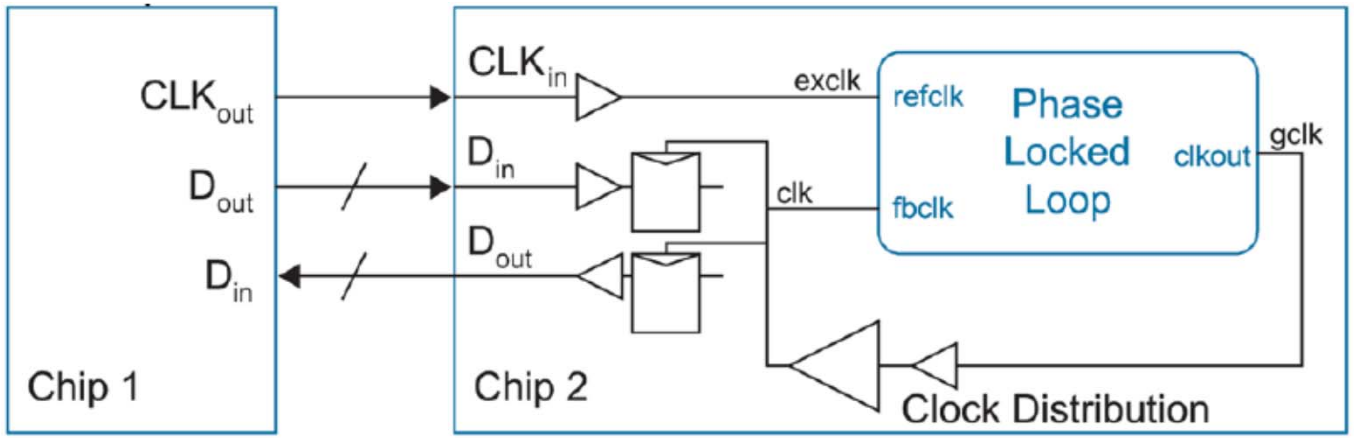


Global Clock Generation

- Global clock generator receives an external clock signal and produces the global clock that is distributed across the die
- Simplest clock generator: a buffer to drive the large capacitance of the clock distribution network
  - Delay of input pads, buffers, distribution network, and gaters cause a large skew between the external clock and the physical clocks received at the clocked elements
  - Clock skew varies with process and environment variations
- Because of clock skew, clocked elements on the chip are not synchronized with the external I/O signals
  - Guaranteeing signal arrival times (setup and hold time requirements) becomes difficult

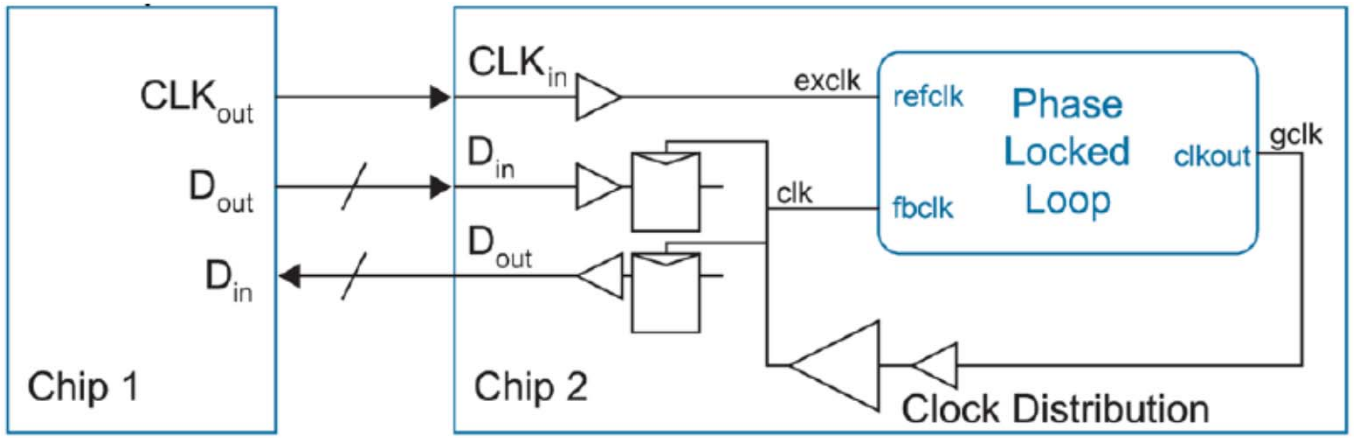
Global Clock Generation

- PLLs are used to compensate for this delay from the input pads of the IC to the individual clocked elements for achieving synchronization with the outside world
- PLLs are also used for frequency multiplication to provide an on-chip clock at a higher frequency than the external clock
  - Ex: Pentium 4 uses a 100MHz external system clock that is multiplied to obtain a 3GHz core clock



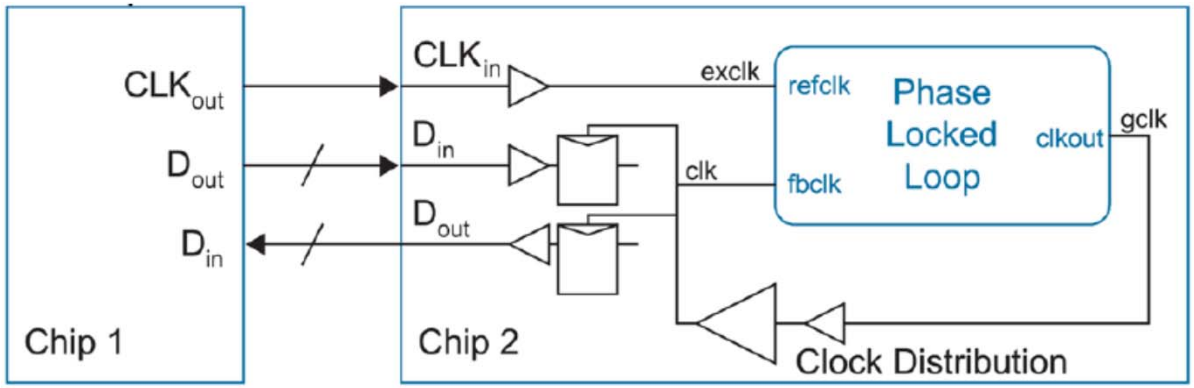
Global Clock Generation

- Chip1 sends a clock and data to chip2
- Chip2 sends data to chip1
- The data must be synchronized to the clock so that each chip can sample the data on the positive clock edge
- However, the internal clock in chip2 is delayed through the clock distribution network
- PLL adjusts the internal clock in chip2 to correct for this delay and keep the clock synchronized with the incoming data



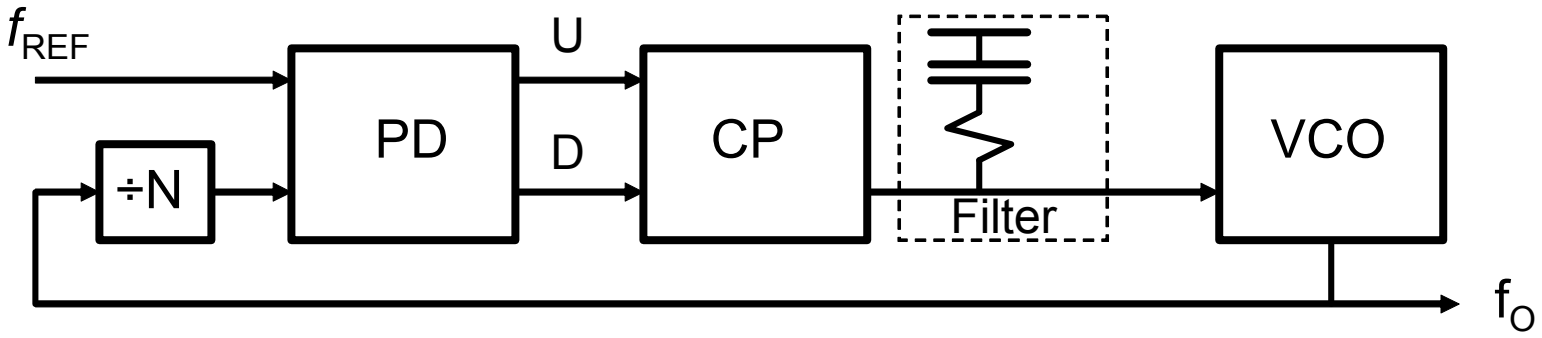
Phase Locked Loop (PLL)

- PLL receives a reference clock and a feedback clock and produces an output clock
- The phase and frequency of the output clock is adjusted until the feedback clock is exactly aligned with the external reference clock
  - Eliminates the systematic clock skew caused by the clock distribution delay
- The feedback clock is tapped off one of the physical clock wires that also drives the registers
- The output clock is the signal sent to the clock distribution network



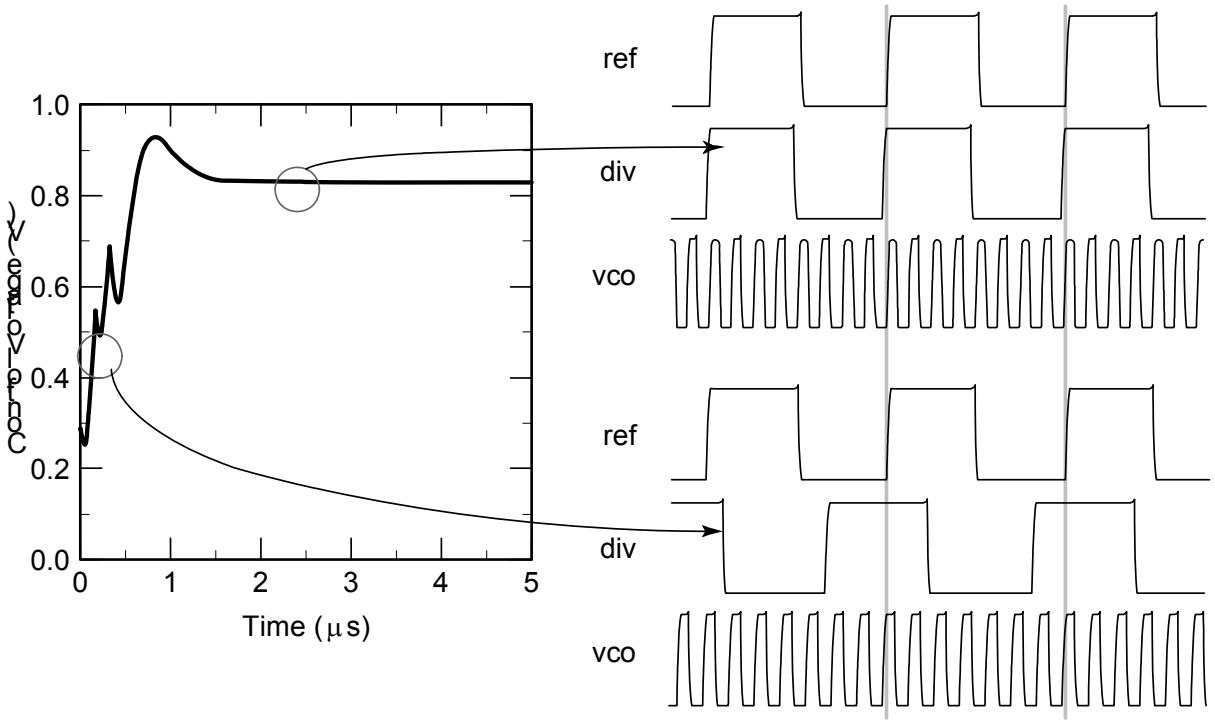
PLL Block Diagram

- PLL is an analog circuit with the following functional composition
- Phase detector (PD) determines whether the feedback clock leads or lags the reference clock
- Charge pump (CD) is an analog circuit that converts Up (U) and Down (D) pulses into an analog voltage
- VCO generates a periodic signal with a frequency that is a liner function of the input control voltage



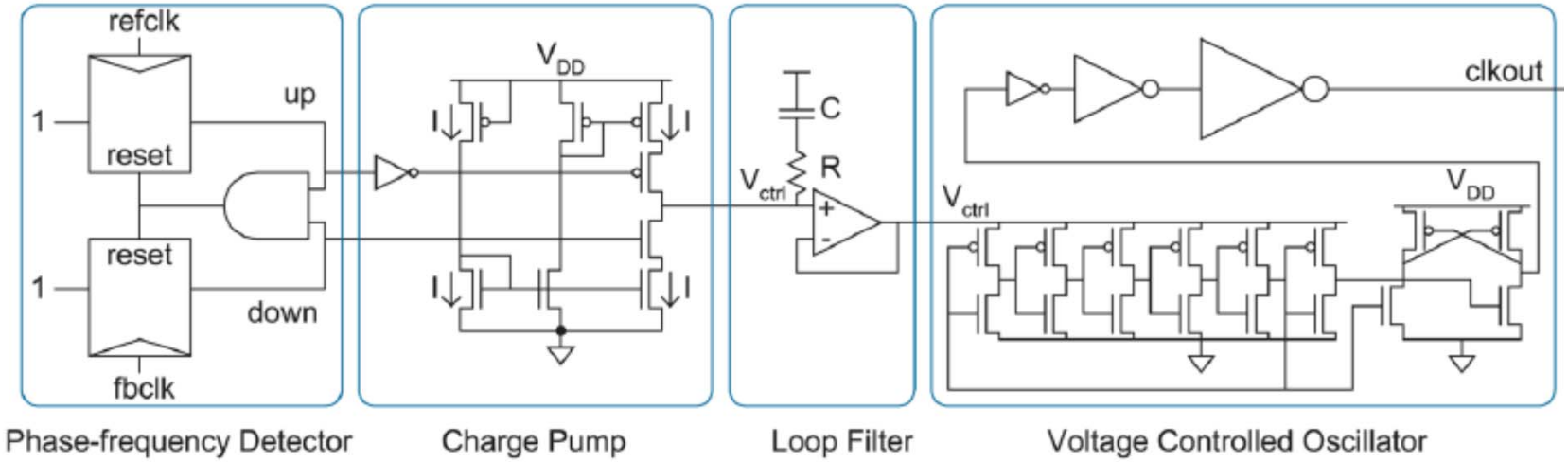
PLL Properties

- **Lock Range**
  - The range of input frequencies over which the loop can maintain functionality
- **Lock Time**
  - The time it takes for the PLL to lock onto a a given input signal



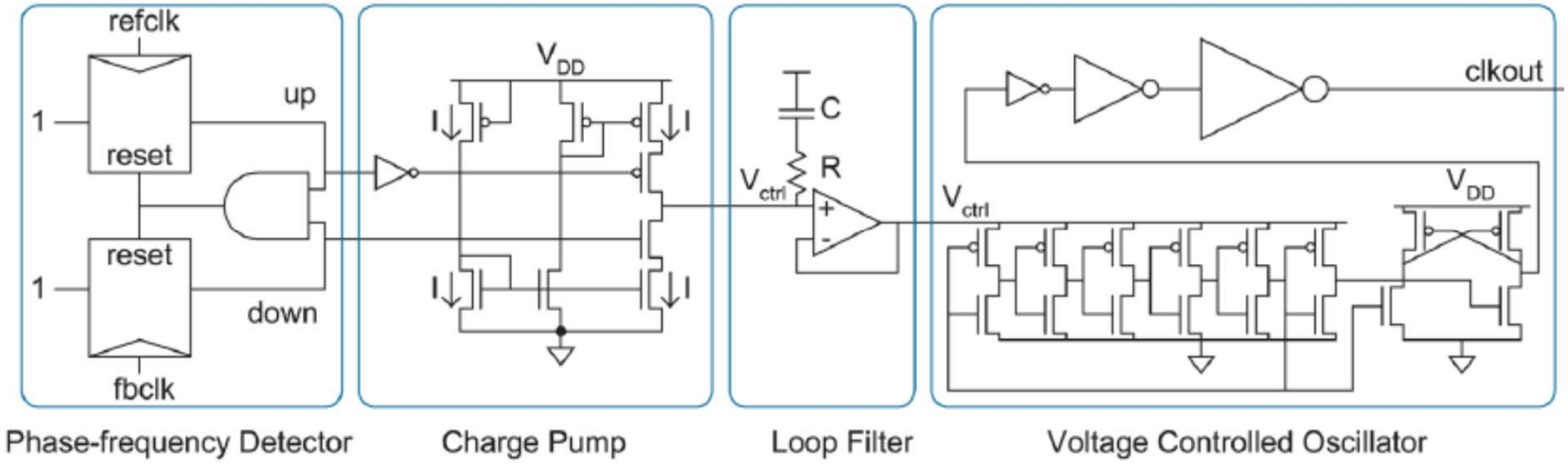
Detailed PLL Structure

- The phase detector consists of a pair of FFs with asynchronous reset that produces pulses to drive the frequency up or down depending upon which clock arrives first
- The charge pump is composed of a pair of current sources enabled by the up and down signals to adjust the voltage on V_{ctrl} until the feedback clock is aligned with the reference clock



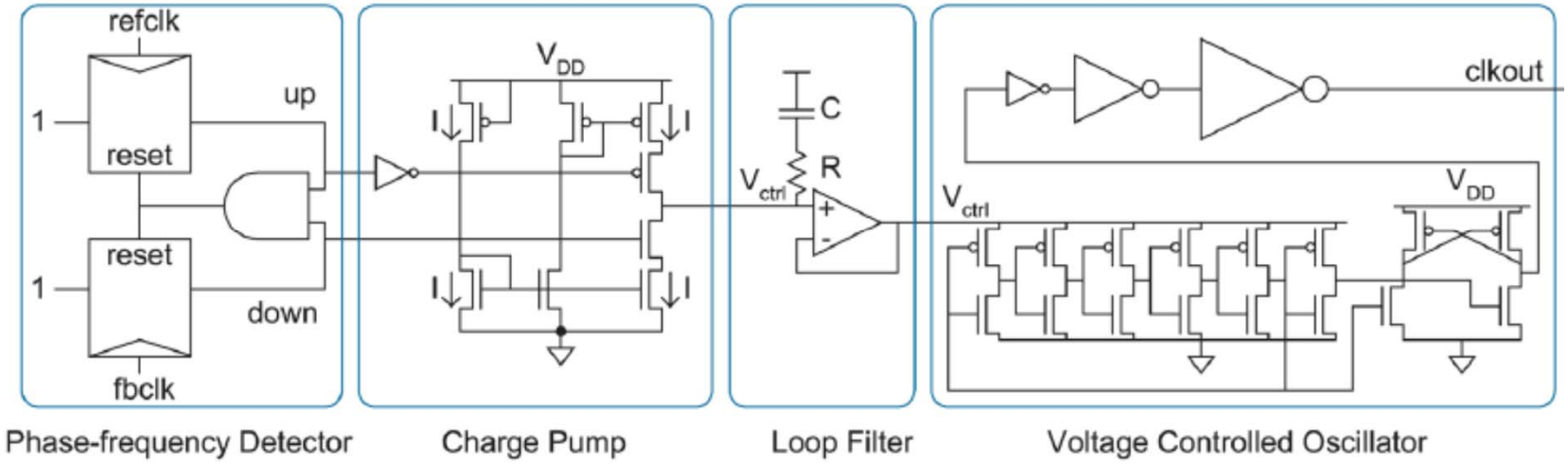
Detailed PLL Structure

- Voltage-controlled oscillator (VCO)
  - A ring oscillator
- The control voltage is adjusted until the oscillator produces an output clock of proper phase and desired frequency
- The control voltage is generated by a charge pump and RC filter



Detailed PLL Structure

- VCO is very sensitive to noise on Vctrl
- Primary sources of jitter in PLLs
  - Power supply noise
  - Substrate coupling noise
- Guard rings should surround all the devices for reducing jitter



Cycle Time and Skew Trend

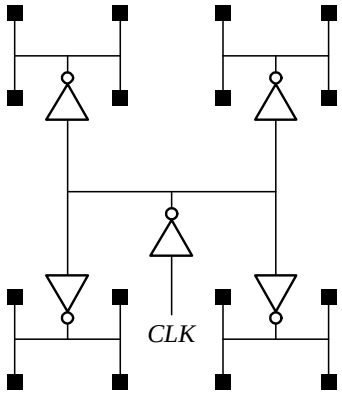
- Much of CPU performance comes from higher clock frequency
  - Clock frequency is enhanced faster than that can be attributed to technology scaling only
  - Skew budget shrinks together with the clock period
- Wires are longer and thinner
  - Higher resistance and capacitance
  - Longer RC delay
- Clock loads are increasing
  - More devices
  - More wire capacitance
- Clock distribution delay and skew tend to GO UP
- Systematic skew can be controlled by a good distribution network design
- Alternatively, random and drift skew and jitter budgets are becoming an increasing portion of the total cycle time

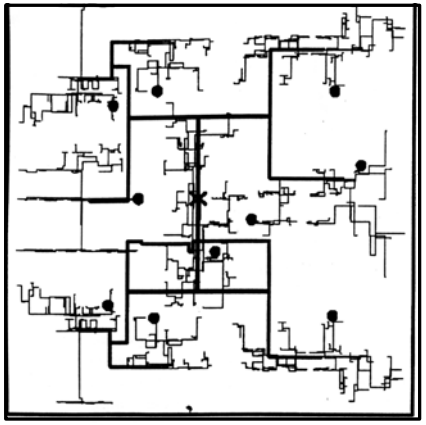
Challenges

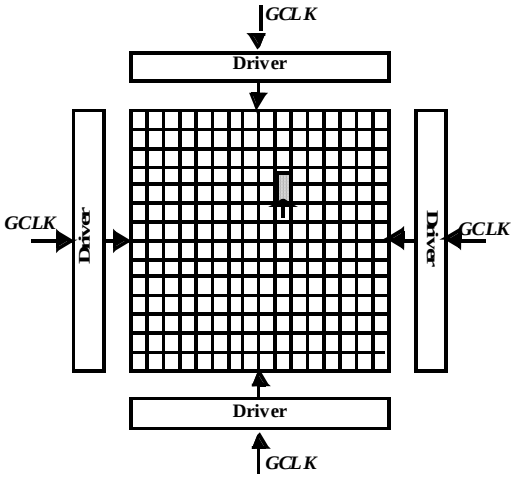
- **Reduce clock skew**
  - Careful clock distribution network design
  - Plenty of metal wiring resources
- **Characterize clock skew**
  - Only budget actual, not worst case skews
  - Difficult to guess
  - Local vs. global skew budgets
- **Tolerate clock skew**
  - Choose circuit structures less sensitive to skew

Global Clock Distribution Techniques

- H-Tree (most used technique, less power consumption)
- Balanced tree (easier to implement)
- Mesh distribution (less skew, high power consumption)
- Hybrid (combined tree and mesh)







Local Clock Gaters

- Generate the local physical clock from the global clock signal
- Outputs of clock gaters run short distances
- Can be used to
  - Adjust clock delay (skew management)
  - Gate the clock
  - Generate pulses
  - Stretch the clock
  - Generate non-overlapping clocks
  - Double the clock frequency
- Gaters can be an important source of clock skew due to random and drift parameter variations

Local Clock Gaters Examples