ECE520 – VLSI Design

Lecture 20: Power Distribution & I/O Circuits

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Review of Last Lecture

- **Clock Distribution Network**
  - **Clock generation (PLLs)**
  - **Clock distribution**
  - **Clock gaters**

Today's Lecture

- **Power Distribution Network**
  - **IR drop**
  - **Switching noise**
  - **Decoupling capacitor**
  - **Electromigrartion**
- **I/O Circuits**
  - **Output buffer**
  - **Level shifters**
  - **Schmitt trigger**
  - **Tri-state outputs**
  - **ESD protection**

Power Distribution Network

❑ Purpose of Power Distribution Network

- Providing power supply and ground to every gate
- Maintaining stable supply voltage across the chip (noise<10%)
- Providing robust supply to entire chip (electromigration)

❑ Challenges in Power Distribution Network Design

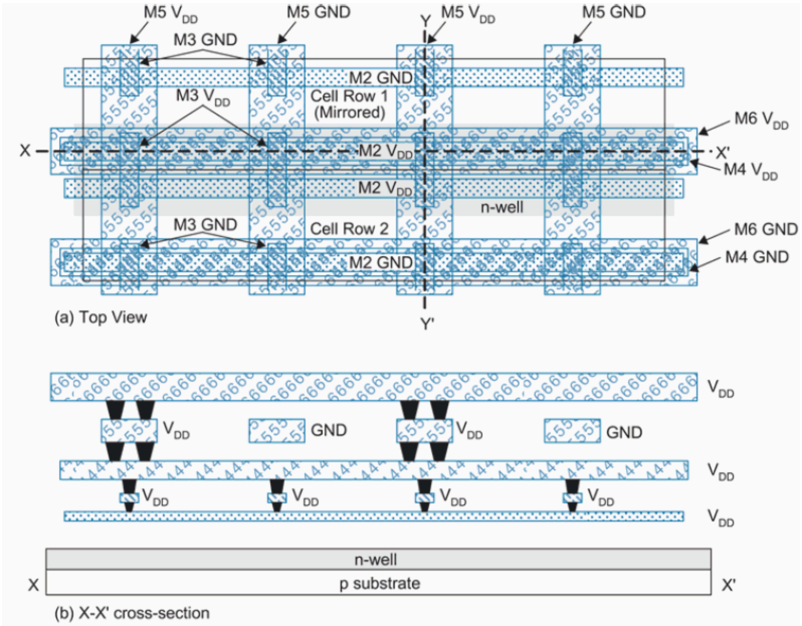
- Carrying 100’s of amps with only 1 V power supply
- Stabilizing the power while millions of gates are switching simultaneously
- Via resistance and electromigration limit becomes bottleneck

❑ Power Distribution Design Consideration

- IR-drop consideration
- Switching noise limitation
- Wiring area requirement
- Electromigration

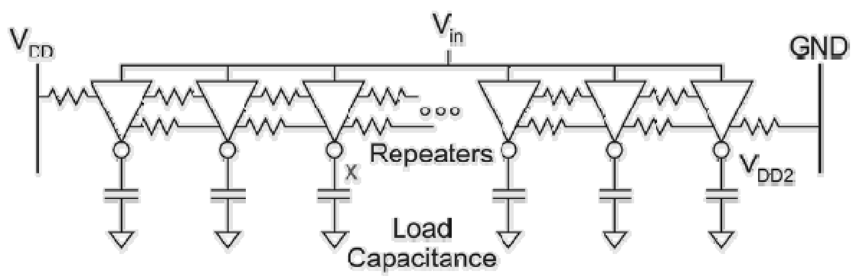
Power Distribution Network

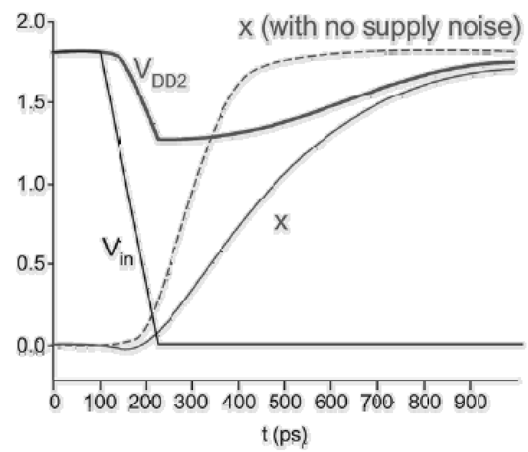
- Like clock distribution network, power distribution network consists of global and local networks
- Global power distribution network are routed at top metal levels across the chip with think and wide routes
- Local power distribution are within smaller blocks and connects all gates' power/ground pins together



IR Drop Consideration

- **On chip wiring resistance dominates IR drop**
- **IR drop affects the performance (increases delay). Why?**
- **Power distribution network must be designed carefully to meet IR drop noise limit. How?**
- **Modern chips devoted about 50% of wiring resource to power and ground distribution to limit the IR drop**

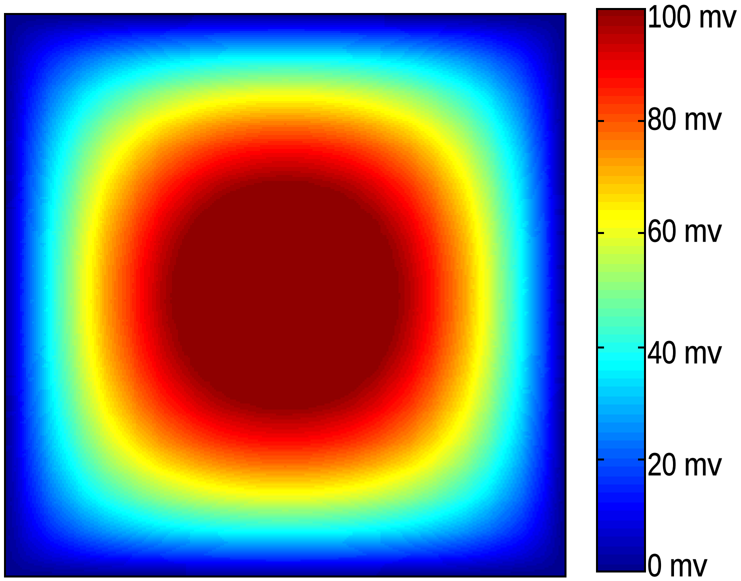




Impact of Packaging on IR Drop

- Packaging technology influences the IR drop

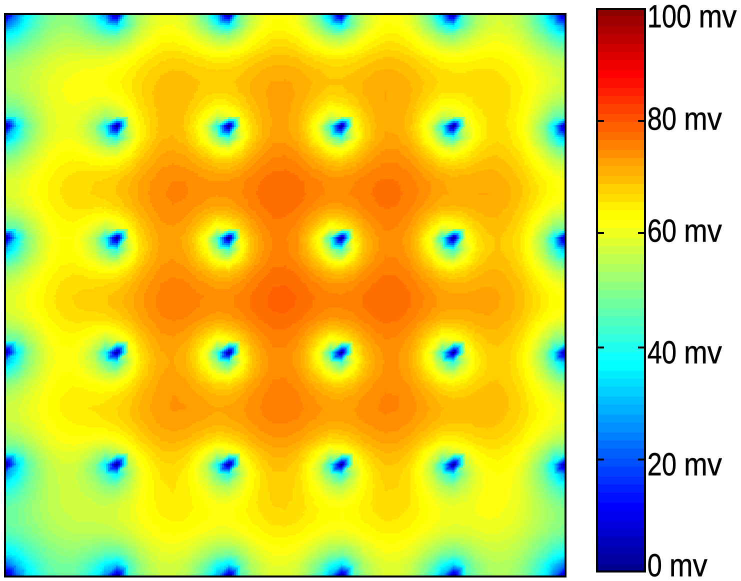
Peripheral Wire Bond System



H= 2 μm, V_{DD}= 1.0 V, P_{tot}= 20 W

Grids=50x50, A_{Chip}=100 mm^2

Area-array Bonding Pads



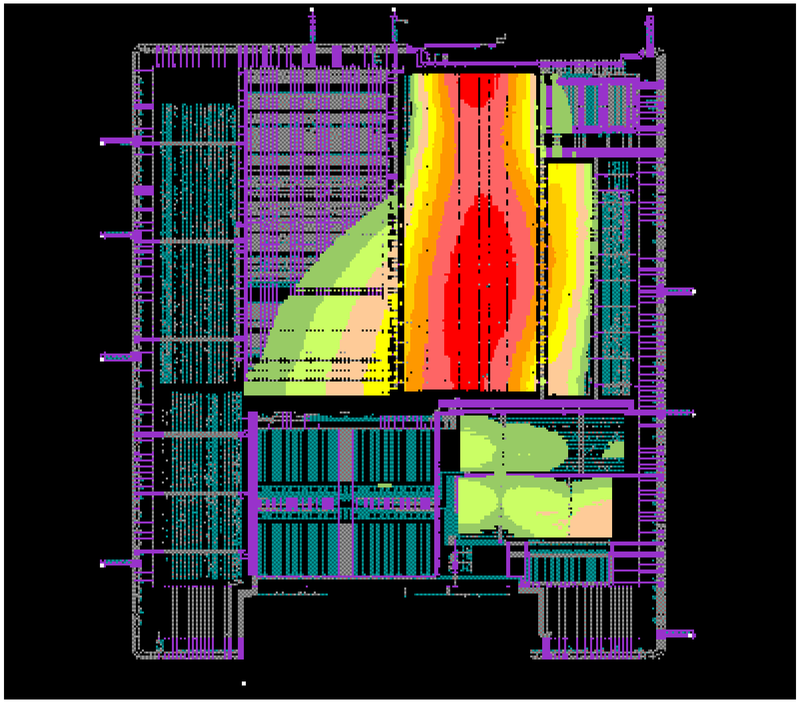
H= 2 μm, V_{DD}= 1.0 V, P_{tot}= 20 W

Grids=50x50, A_{Chip}=100 mm^2

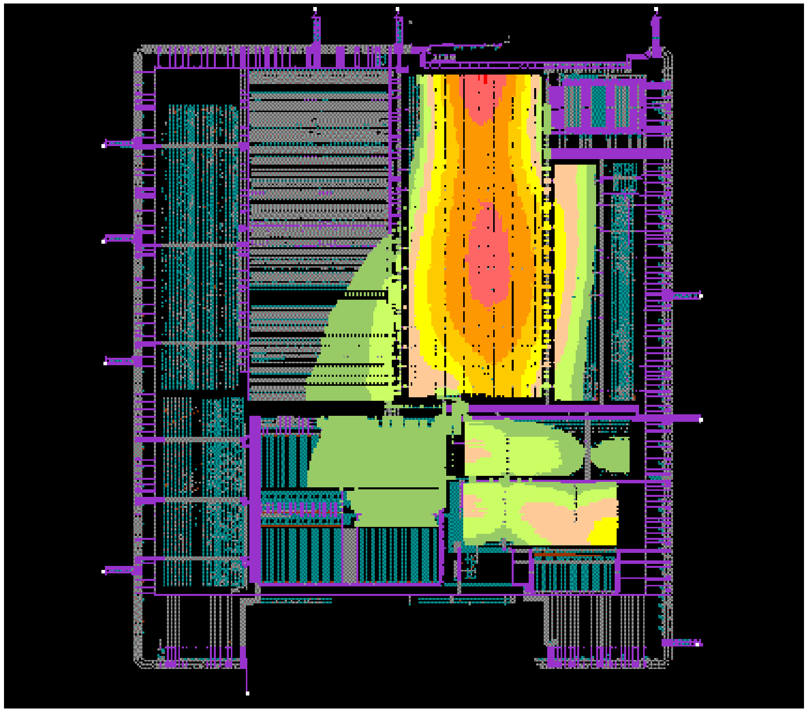
Example: IR Drop Analysis

- **IR drop is part of design sign off**
- **Most EDA tools can analyze power distribution network nd predict the IR drop**

Before



After



Switching Noise

- On chip wiring Inductance and the inductance of wire bonds are the source of on chip switching noise
- Packaging inductance and the inductance of circuit board planes and traces are the source of off chip switching noise
- Modern chips devoted about 50% of IO pins to power and ground distribution to minimize the power and ground impedance and to limit the switching noise
- Methods of switching noise reduction
  - Large decoupling capacitors
  - Large number of P/G pins
  - Architectural solutions
  - Using flip-chip instead of traditional wire bond packaging

Example of Switching Noise

- A 1GHz chip transitions from idle to full power active mode in a single cycle. I_{idle} = 20A. I_{active} = 60A. If the power distribution network has 20pH series inductance estimate the power supply noise caused by a transition from idle mode to active mode
- Answer:

$$\frac{\Delta I}{\Delta t} = \frac{60\,A - 20\,A}{1ns} = 40\ GA/s \quad \Rightarrow \quad \Delta V = L\frac{\Delta I}{\Delta t} = 0.8\ V$$

- Unacceptably high voltage drop
- Solutions
  - Prevent an IC transitioning from idle to active mode in one clock cycle
  - Use decoupling capacitors (Bypass capacitors)

Example of Bypass Capacitance

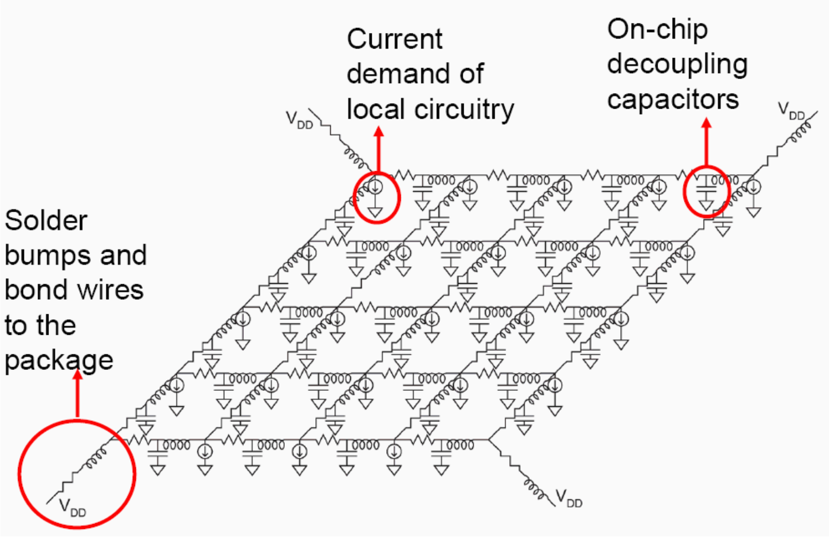
- **How much decoupling capacitor is needed to supply a sudden current spike of 40 A for 1ns with a voltage droop less than 200 mV**
- **Answer:**

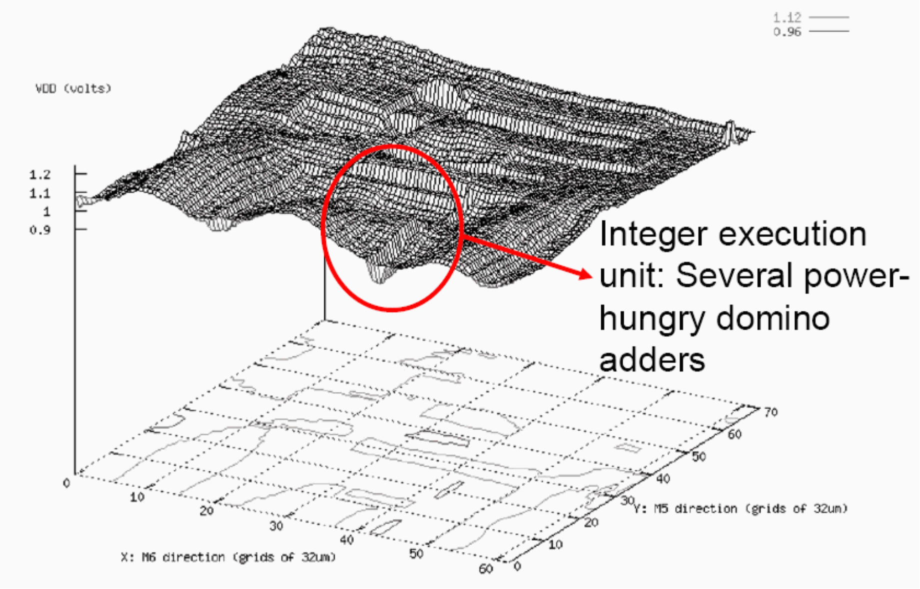
$$I = C\frac{\Delta V}{\Delta t} \quad \Rightarrow \quad C = \frac{I\Delta t}{\Delta V} = \frac{40\,A \times 1ns}{0.2V} = 200\ nF$$

- **Inherent parasitic and gate capacitance of quiescent transistors connected to the power distribution network are part of bypass capacitance**
- **Extra bypass capacitance is build from large MOSFETs**
- **This will increase the leakages power. Why?**

Full Chip Switching Noise Analsysis

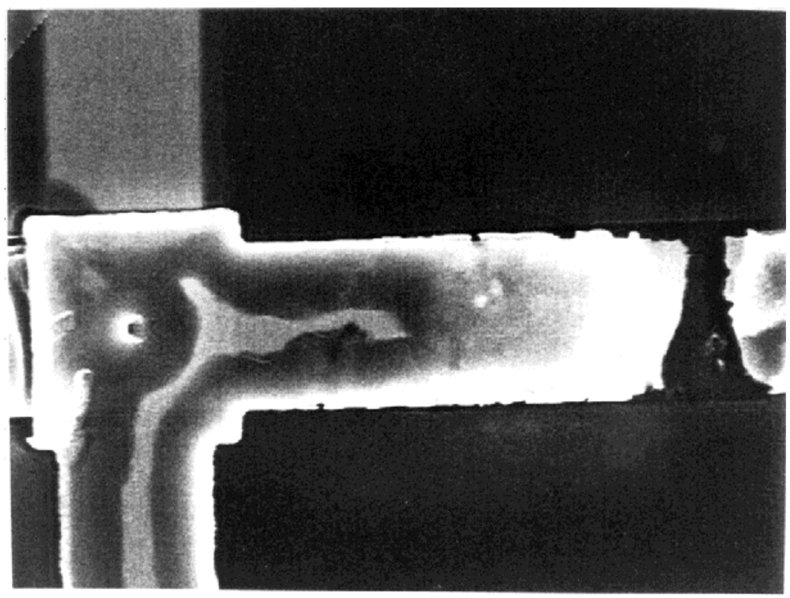
- ❑ **Itanium 2 power supply voltage simulation**





Electromigration Limit

- Power supply network carries unidirectional current which is a concern for electromigration
- Number of vias and the width of power/ground routing should be designed with electromigration in mind



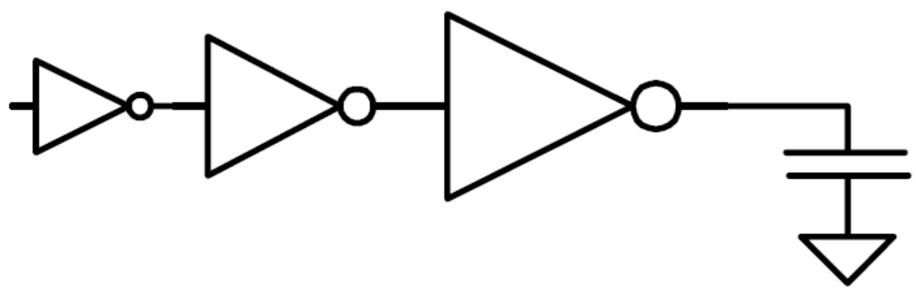
I/O Circuits

- **Input/output (I/O) circuits are the way of chip communication to outside world**

- **I/O has some characteristics to be dealt with**
  - **Much higher capacitances than those encountered on-chip**
  - **Different voltage levels than those on-chip**
  - **The need to protect core circuitry from electrostatic charges (ESD)**
  - **The need to "de-bounce" incoming signal to eliminate noise**

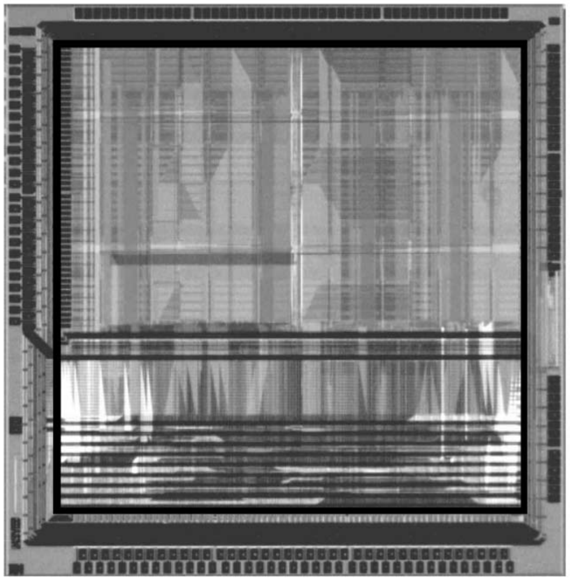
Buffering Output Loads

- Output pin loads are measured in 10's of pF
- We need to buffer up from small loads on chip to drive these large values
- This is simply the problem that we looked earlier
  - How many stages do we need?



I/O Ring

- Most chips have an "I/O Ring" that communicates with the outside world
- This runs at the clock rates of the I/O, rather than the core
- Voltage translations are also handled here
- The ring was necessary for wire-bonded chips, since bond wires connected a short distance to the package
- Even with C-4 (controlled collapse chip connections) and other flip-chip technologies, I/O is generally at the edge and the rest of the pads are used for power and ground



Level Shifting: Down

- If the transistors can handle the voltages applied, an inverter (or any logic circuit) can shift voltages down
  - Note that the PMOS gate will be driven beyond the lower power rail, but that is ok
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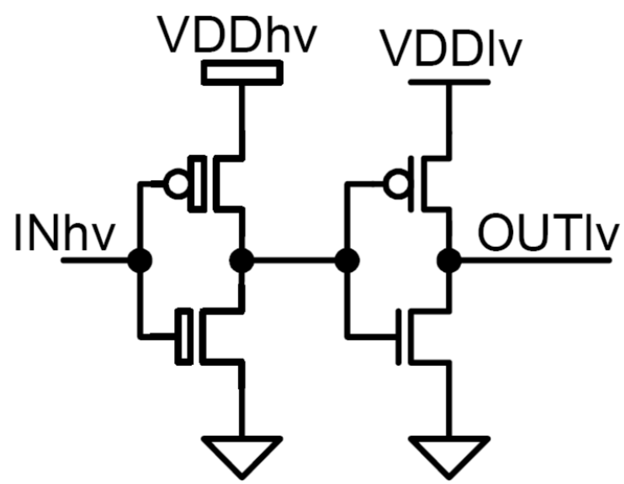
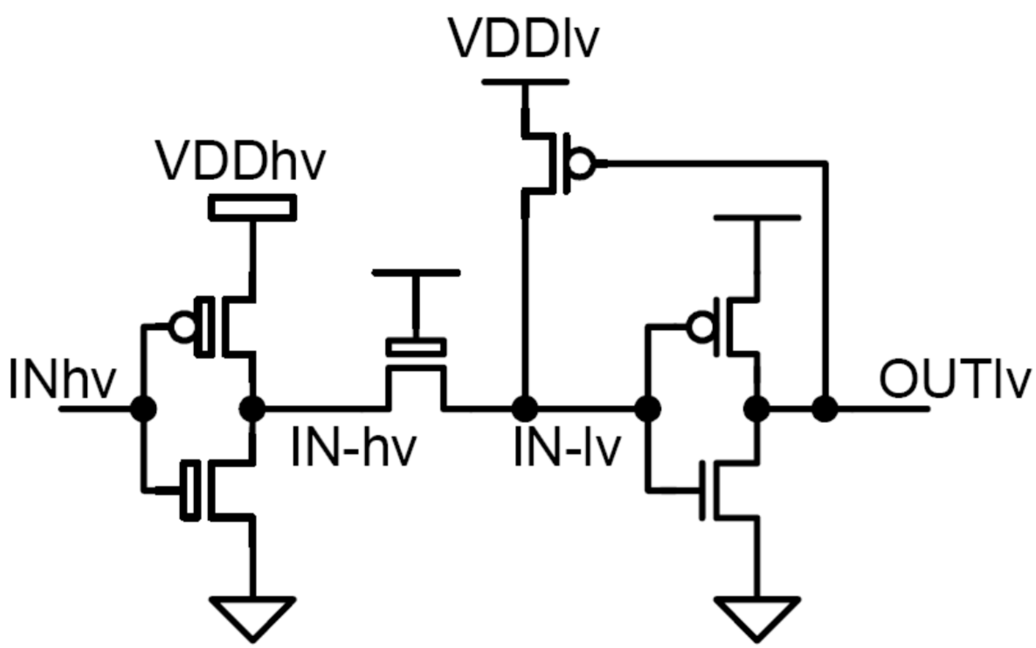
- However, if the high voltage exceeds the capability of the core transistors, they must be protected



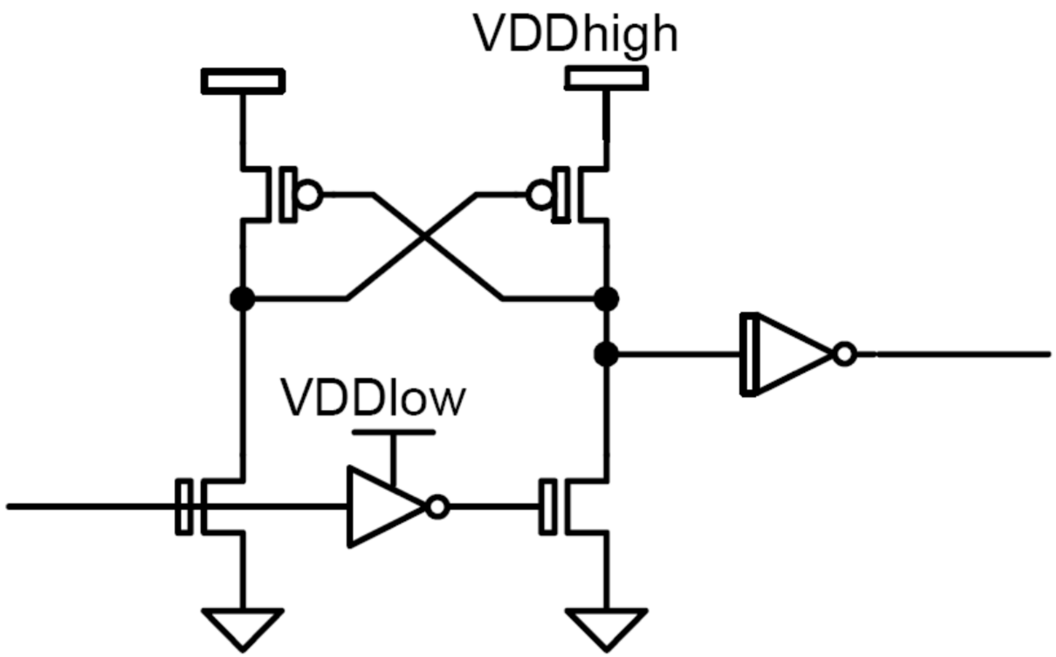
Level Shifting: Down

- A protecting level shifter looks like a latch
- The transparent input protects the circuitry inside by its cascode behavior
- Note the PMOS keeper since the input cannot pull up to the VDD rail



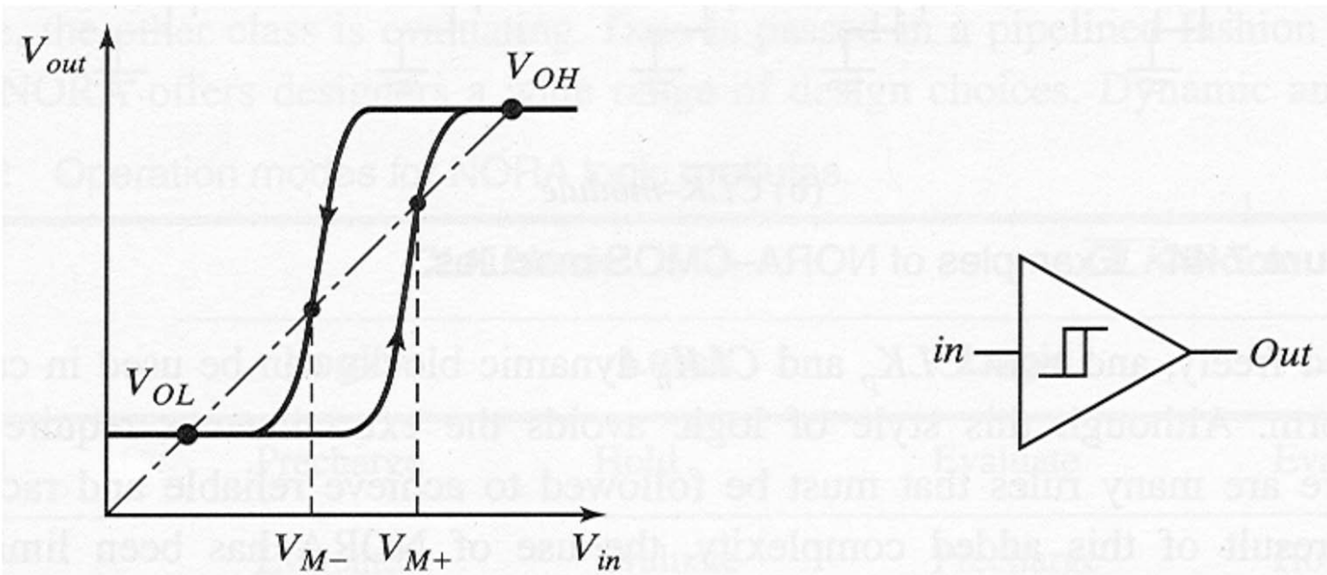
Level Shifting: Up

- Level shifting to a higher voltage is more difficult
  - If we used an inverter, the PMOS would never turn off
  - The DC currents would be unacceptable
- The circuit used is the now familiar differential (DCVSL) style



De-Bouncing Input Signals

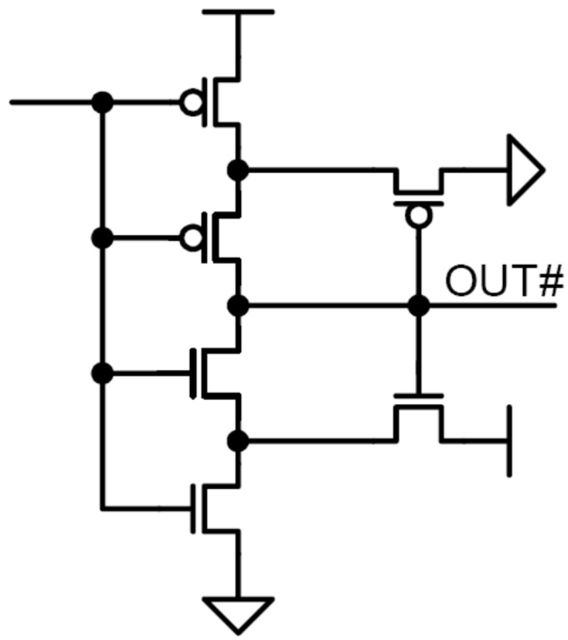
- Input signals can be noisy
- We don't want to respond to noise, so we'd like to use a circuit that will filter out small deviations around the switch point



(a) Voltage-transfer characteristic (b) Schematic symbol

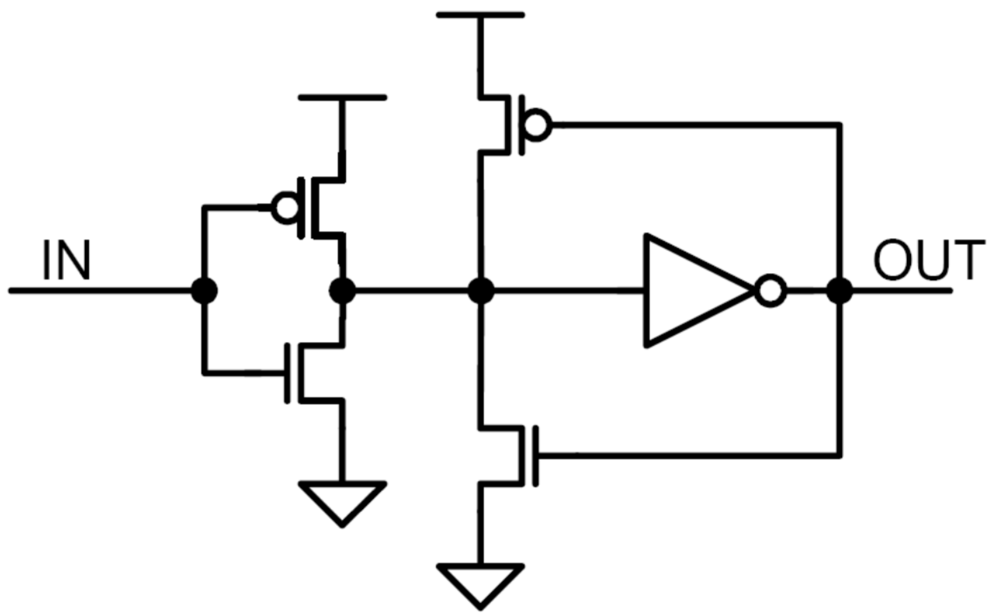
Schmitt Trigger

- **This is an inverter with a variable P to N ratio**
  - **Recall that the switch point of the inverter was movable by changing the size of the PMOS and NMOS transistors (their ratio)**
- **This circuit adjusts that ratio adding two more transistors that at first resist then help the transition**



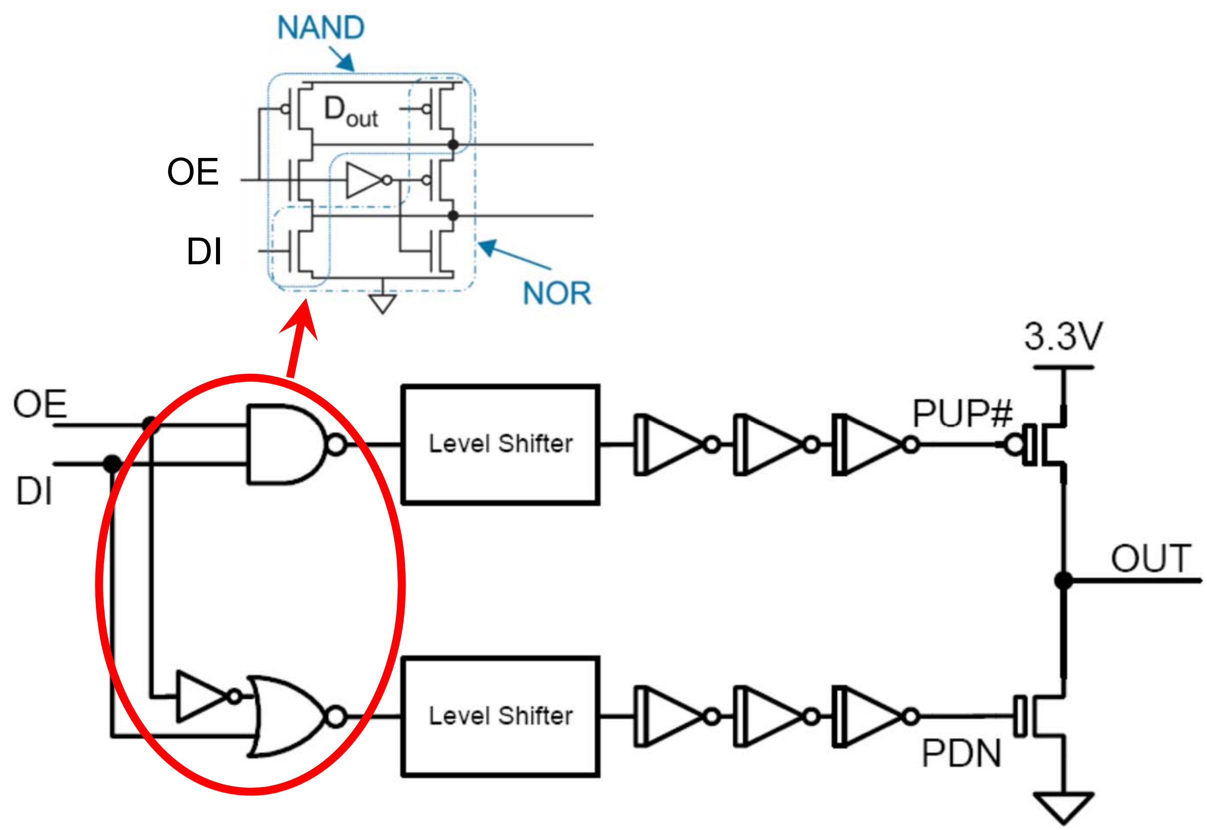
Another Circuit for Schmitt Trigger

- **This circuit also changes the P to N ratio based on the state of the output**
- **This circuit also needs 6 transistors**



Tri-State Outputs

- We'd like to avoid stacks since we'll be driving large loads
- The output enable control is before the level shifters
- The buffering up is in the thick gate domain



Electrostatic Discharge Circuit (ESD)

- **ESD is the transmission of built up static charge to the chip**
  - **It doesn't take much charge to create a large voltage on a small capacitance and most capacitances on ICs are small**
- **Circuits must be added to the IC to shunt the voltages away before they grow too large**
- **The currents can be pretty large, so these circuits can be large, e.g., 10 mm wide devices!**
- **ESD design for Human Body Model (HBM) requires to protect the circuit against 1.33A peak current with the rise time of 10-30ns**

ESD Protection

- The incident charge is generally dumped to the power Rails
- For outputs, the parasitic diodes of the large output transistors can often do the trick
- For inputs, there is usually a current limiting transistor and diodes dump the charge to the rails