ECE520 – VLSI Design

Lecture 22: Nonvolatile Memories

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

Review of Last Lecture

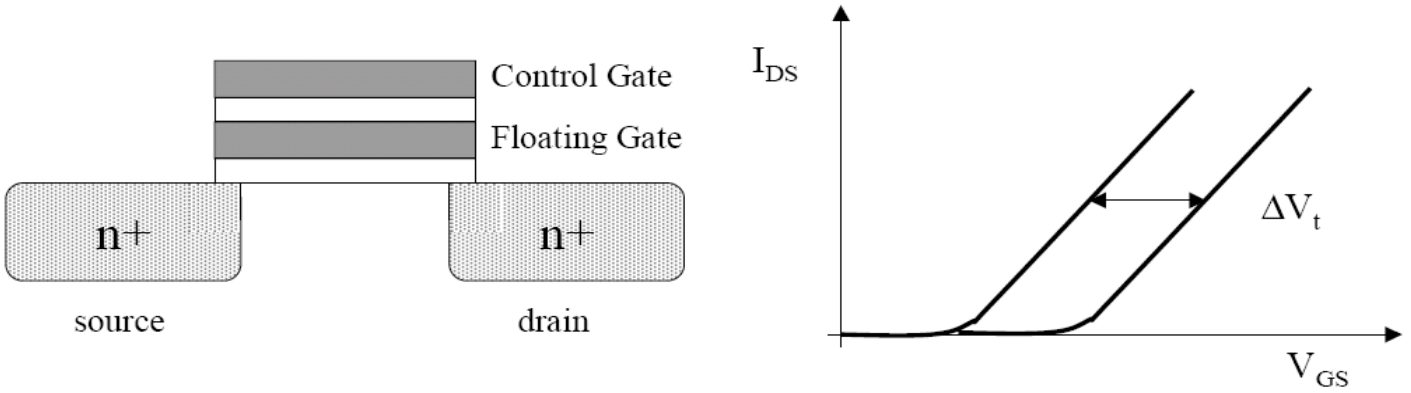
- **Memory architectures**
- **ROM**
  - **NOR ROMs**
  - **NAND ROMs**

Today's Lecture

- **Nonvolatile Memories**
  - **EPROM**
  - **EEPROM**
  - **Flash**

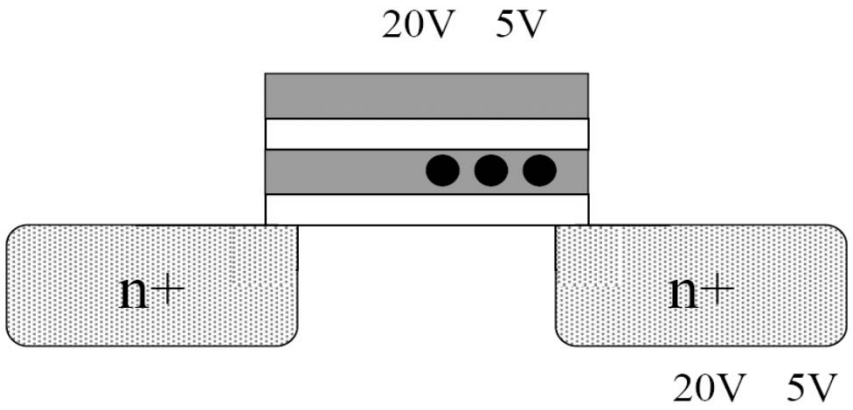
Nonvolatile Memories

- All present non-volatile memories are based on ROM memory configurations
  - All retain the single BL, although the sensing may be differential, using comparison to some reference voltage or replica BL
- The key to present memories is the ability to change the V_T of the transistor by adding or removing charge from a floating gate



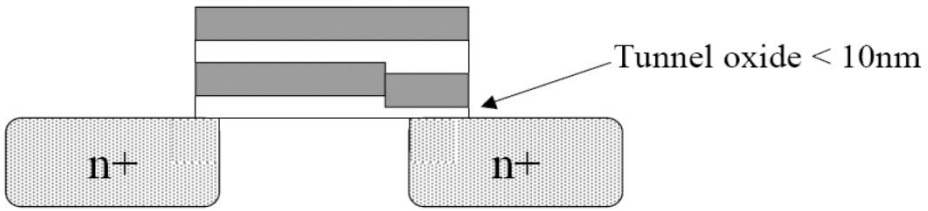
Erasable Programmable ROM (EPROM)

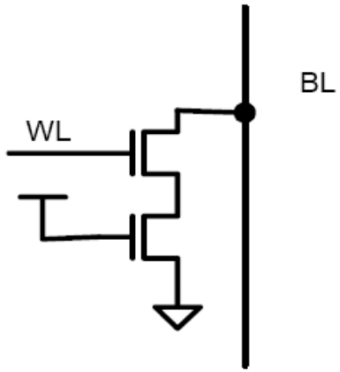
- Uses the same ROM NOR topology but can electrically increase the V_T of a cell via hot electron injection to a floating gate
- Erase is by UV light: Energetic photons knock the charge off the floating gate
  - This is an off-line operation and requires expensive packages with windows
  - Windowless packages are used for one time program (OTP)



Electrically Erasable PROM (EEPROM)

- **EEPROM allows electrical erase of the cells**
  - **By providing a thin oxide at the drain end, the proper voltage can remove the charge via Fowler-Nordheim tunneling**
  - **The cells require two transistors per cell however**
- **A drawback of this cell is V_T drift when exposed to read voltages A separate access transistor helps to alleviate this problem, but at a significant density penalty**





Flash Memories

- Flash memories also allow electrical erase but at better granularity and speed
- A single thin oxide is used and a one transistor cell is possible
- Flash is available in NOR and NAND varieties
  - Flash is faster so can be main memory - still very slow compared to SRAM
  - It is impractical to directly run code from NAND so it is primarily popular as data storage, e.g., photos, USB drives, etc.
- Multiple level cells are possible with choices of 4 V_Ts
  - This requires multiple sense amplifiers or multiple passes
  - Programming precise values is difficult and "over-erase" must be avoided
- Scaling flash transistors is very difficult since the oxide cannot scale
  - About 1 electron per month is the allowable loss