ECE520 – VLSI Design

Lecture 23: SRAM & DRAM Memories

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Review of Last Lecture

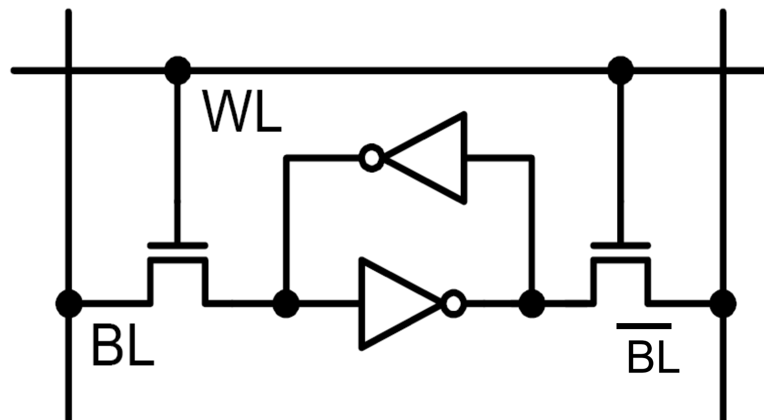
- **Nonvolatile Memories**
  - **EPROM**
  - **EEPROM**
  - **Flash**

Today's Lecture

- Static Random-Access Memory (SRAM)
  - SRAM cell
  - SRAM architecture
  - Sense amplifier
- Dynamic Random-Access Memory (DRAM)
  - DRAM cells
  - DRAM Capacitor implementation
  - DRAM Sense amplifier
- ECE 638 (Spring '16) – ST: VLSI Design & Testing

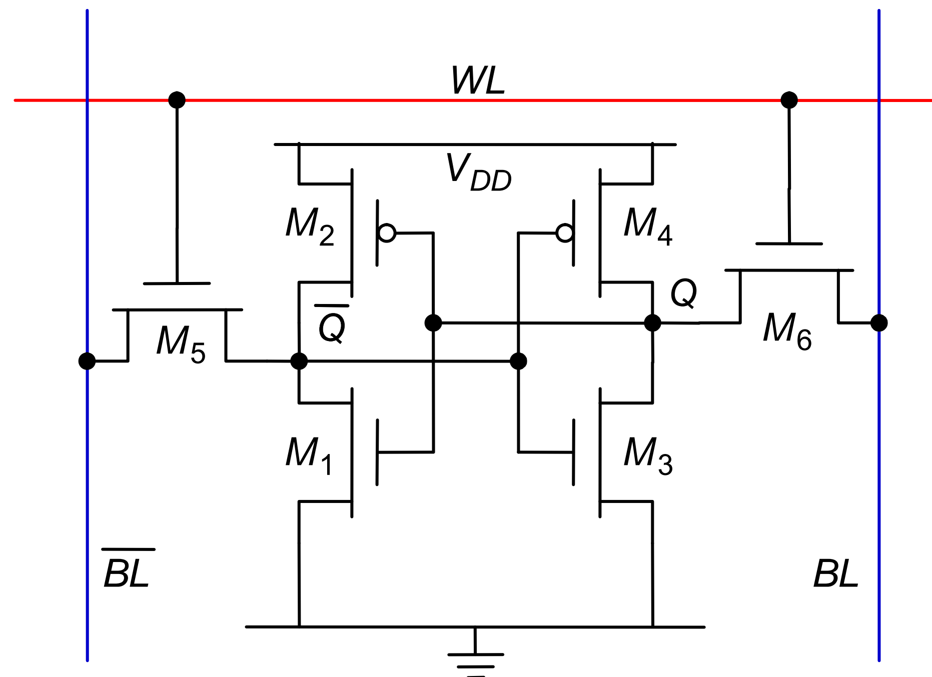
SRAM Cell

- SRAM cell is quite similar to flip-flop without any protective circuitry
- Therefore, reliable operation imposes transistor sizing constraints.
- Cell is selected by word line (WL=1) and read and write are often differential



6-T SRAM Cell

- SRAM cell consists of 6 transistors (6T cell) with differential BL
- When reading, BLs are at VDD and have high capacitance
  - This is essentially a short to VDD for both side of the cell
  - The side at logic one is unaffected. e.g. Q at VDD and BL at VDD
  - Node $\overline{Q}$ is pulled up by the voltage divider of two NMOS transistors

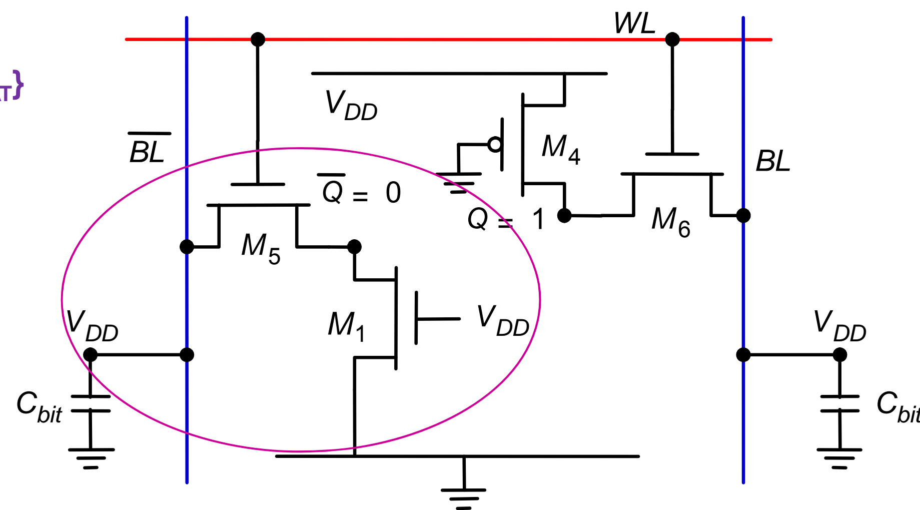


6-T SRAM Cell – Read operation

- **The pull down must be stronger than the access transistor**
  - **The access transistor is then generally narrower and longer channel**
  - **Read margin is greatly affected by process variation**
- **The amount of voltage rise at $\overline{Q}$ node, ΔV is computed as follow:**

V_{min}=min{V_{GS}-V_T, V_{DS}, V_{DSAT}}

V_{Q_bar}=small then:
M1 in Linear region
M5 in Velocity Saturation



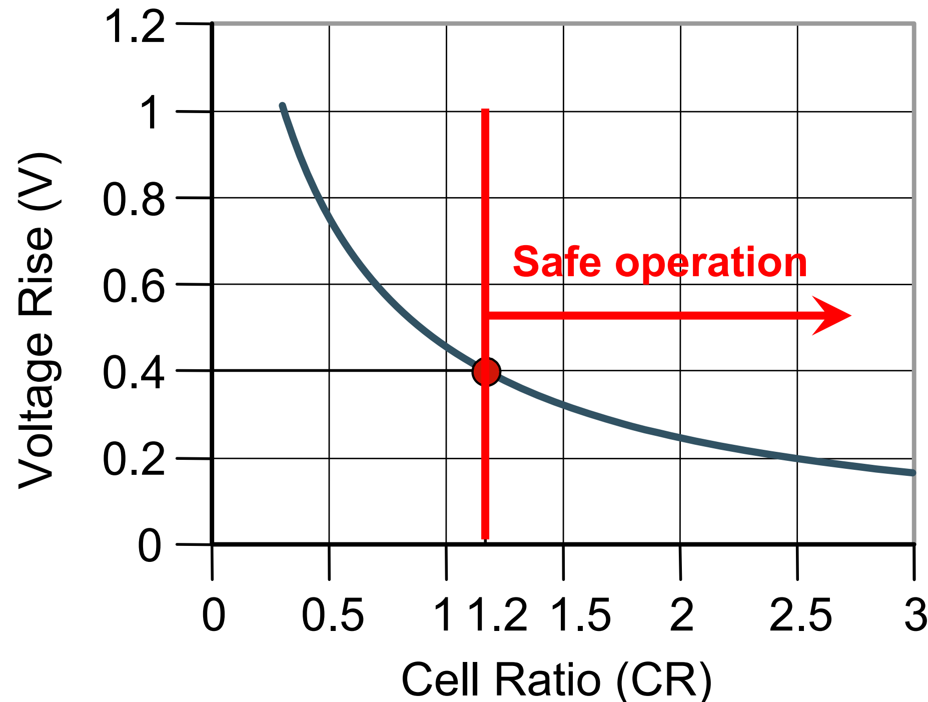
$$CR = \frac{W_1/L_1}{W_5/L_5}$$

$$k_{n,M5}\left((V_{DD} - \Delta V - V_{Tn})V_{DSATn} - \frac{V_{DSATn}^2}{2}\right) = k_{n,M1}\left((V_{DD} - V_{Tn})\Delta V - \frac{\Delta V^2}{2}\right)$$

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{Tn}) - \sqrt{V_{DSATn}^2(1 + CR) + CR^2(V_{DD} - V_{Tn})^2}}{CR}$$

6-T SRAM Cell – Read operation

- Pull down NMOS must be stronger than access transistor to prevent ***read upset***
- For 0.25um technology cell ratio, CR, must be larger than 1.2



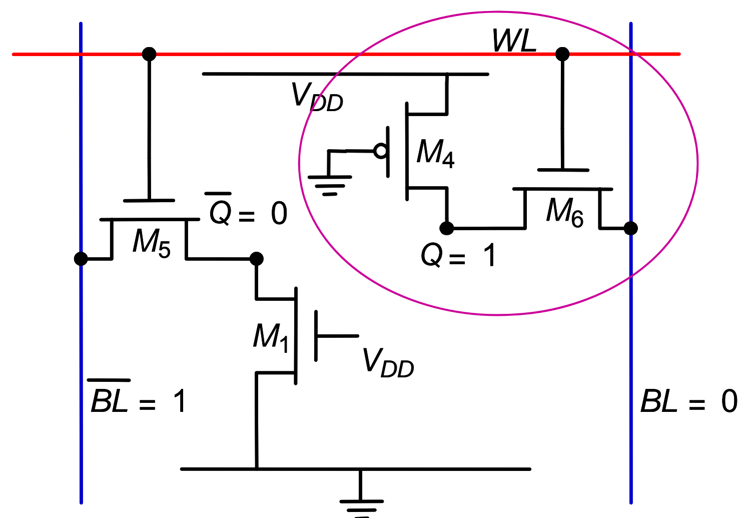
$$CR = \frac{W_1/L_1}{W_5/L_5}$$

6-T SRAM Cell – Write operation

- **The pull up PMOS must be weaker than the access transistor**
  - **Write margin is also affected by process variation**
- **The amount of voltage at Q node, V_Q is computed as follow:**

$V_{min}=min\{V_{GS}-V_T, V_{DS}, V_{DSAT}\}$

V_Q=small then:
M6 in Linear region
M4 in Velocity Saturation



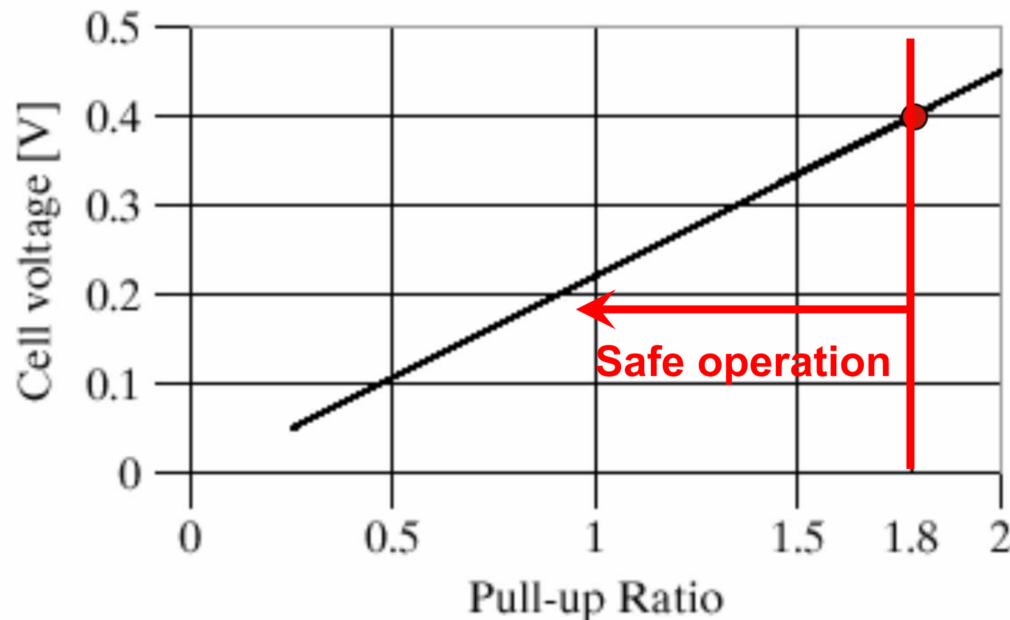
$$PR = \frac{W_4/L_4}{W_6/L_6}$$

$$k_{n,M6}\left((V_{DD}-V_{Tn})V_Q-\frac{V_Q^2}{2}\right) = k_{p,M4}\left((V_{DD}-|V_{Tp}|)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)$$

$$V_Q = V_{DD}-V_{Tn}-\sqrt{(V_{DD}-V_{Tn})^2-2\frac{\mu_p}{\mu_n}PR\left((V_{DD}-|V_{Tp}|)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)},$$

6-T SRAM Cell – Write operation

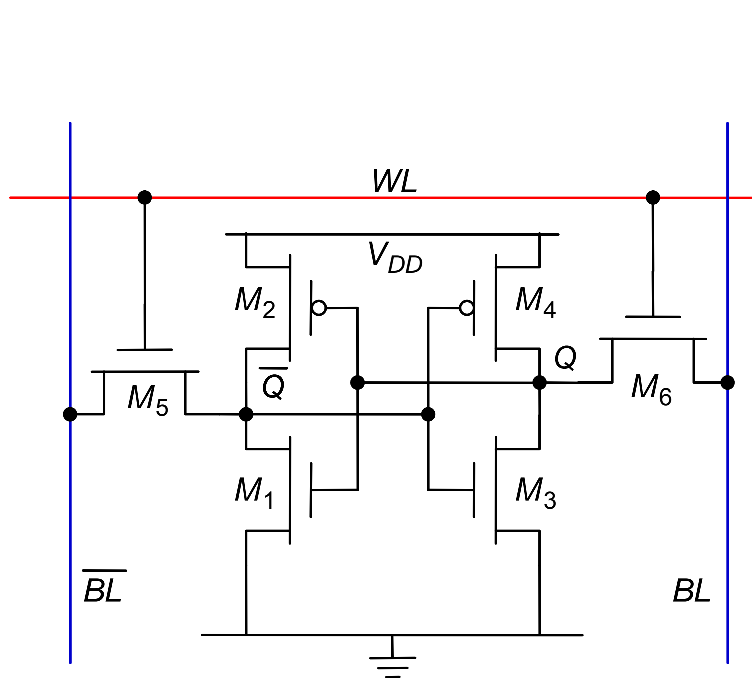
- **Pull up PMOS must be weaker than access transistor to make the SRAM cell "writable"**
- **For 0.25um technology pull up ratio, PR, must be smaller than 1.8**

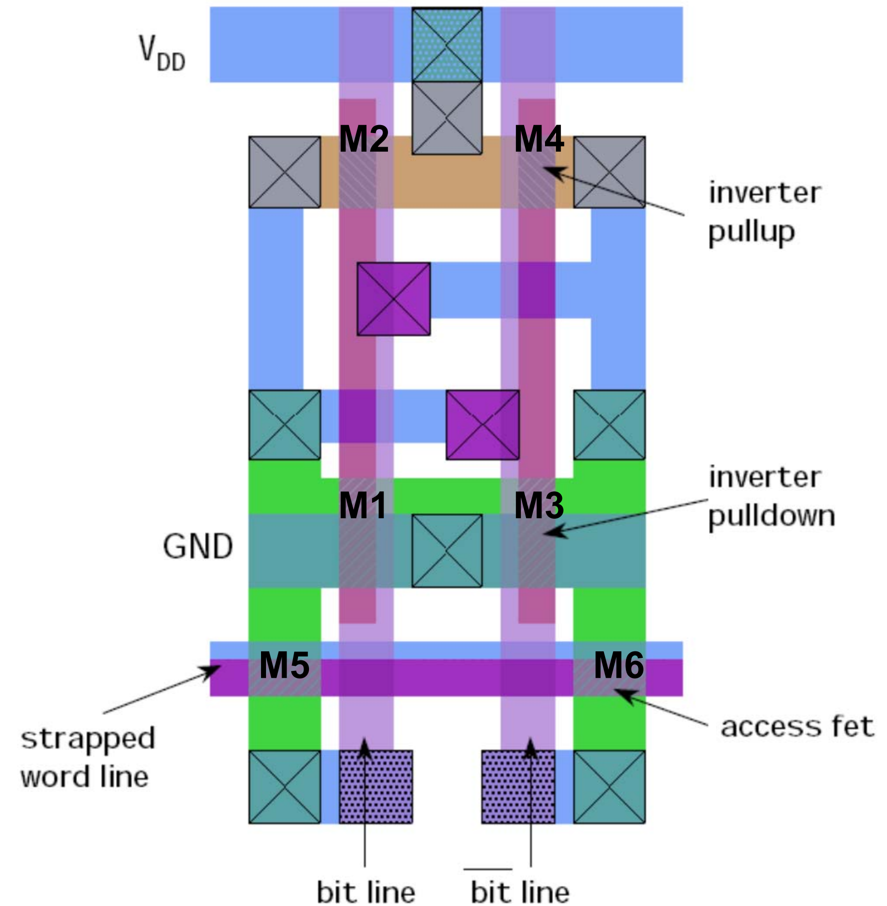


$$PR = \frac{W_4/L_4}{W_6/L_6}$$

SRAM Layout

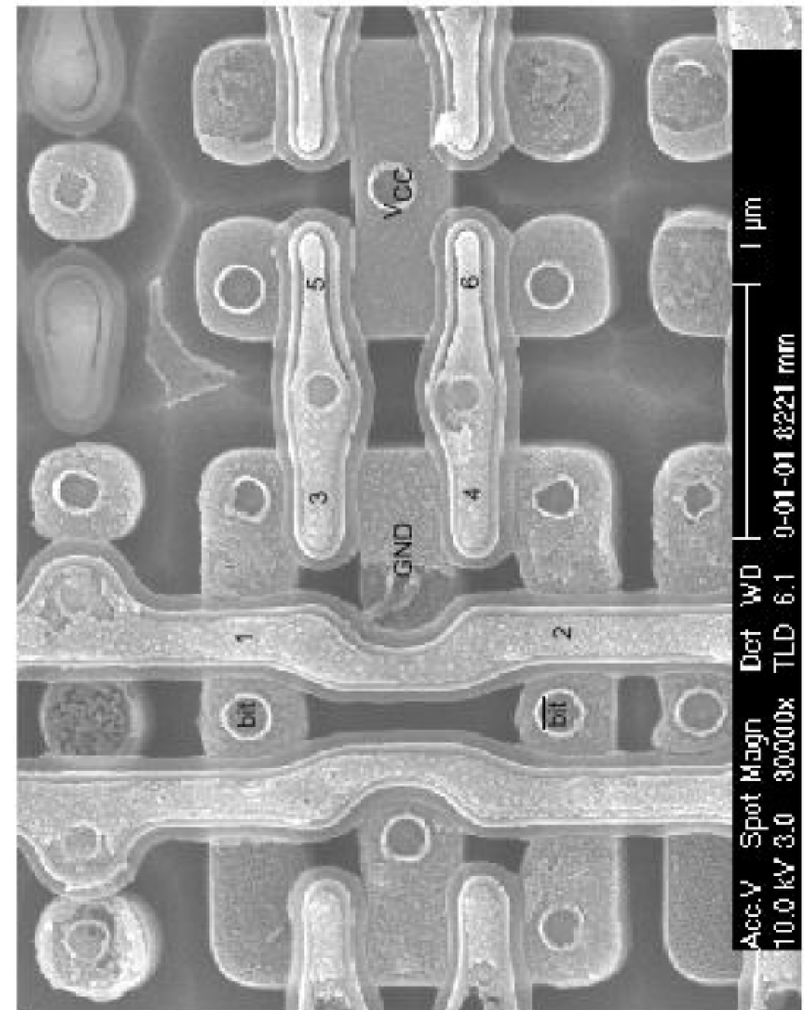
- Layout must be symmetric to reduce process variation





Real SRAM Cell

- Real cells will have extensive corner rounding and layer misalignment
  - Hence the cell will not be symmetric in reality
  - Note rounding and misalignment!
- Since there are a lot of statistics in a large SRAM, e.g., 1MB L2 has nearly 10M cells (including ECC) so random variation will work against full yield
  - This can be partly made up by redundancy
  - But solid cell design is essential
  - Worst case process corners must be used

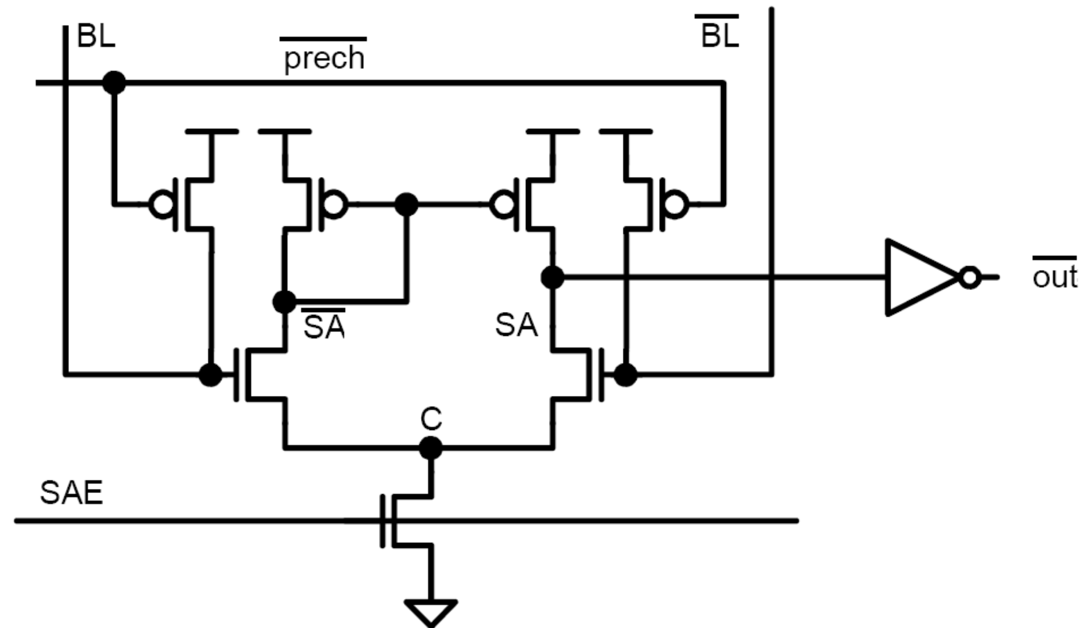


SRAM Read - Sensing

- The simplest reading is an inverter sense
  - This is slow unless the BL is very short
- Generally, we want to use a sense amplifier
  - Smaller swing on BLs (only about 50mv is necessary)
  - The SRAM cell transistors are small and weak and BL has high capacitance. Therefore, BL swing is very slow. Faster operation requires smaller swing.
  - Smaller swing saves power (as long as we don’t drive the BLs with the sense amplifier) by limiting swing on the BLs

Sense Amplifier : Static

- A simple OPAMP can be used as sense amplifier
  - Unfortunately in practice, it is very slow to respond
  - This is static, since the output is only as a function of input
- This circuit has serious CMRR problems, particularly when both inputs are near the VDD rail

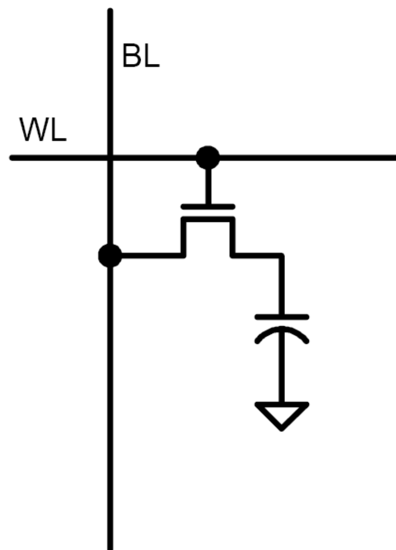


Sense Amplifier : Regenerative

- Consists of two inverters in a positive feedback configuration
  - The input voltage imbalance V(BL) and V($\overline{BL}$) is put on SA and $\overline{SA}$ and then positive feedback is enabled to amplify to the voltage rails

1T DRAM Cell

- Stored bit is held dynamically on a capacitor
- Very small storage cell – only 1 transistor
  - Originally the capacitance was just the drain capacitance
- Unfortunately, charge doesn't scale – key to technology is packing more capacitance into a smaller area over time
  - Tow main approaches: (1) Trench capacitor, (2) stacked capacitor

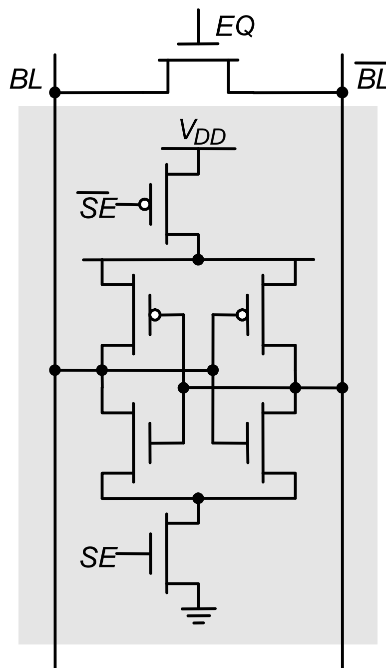


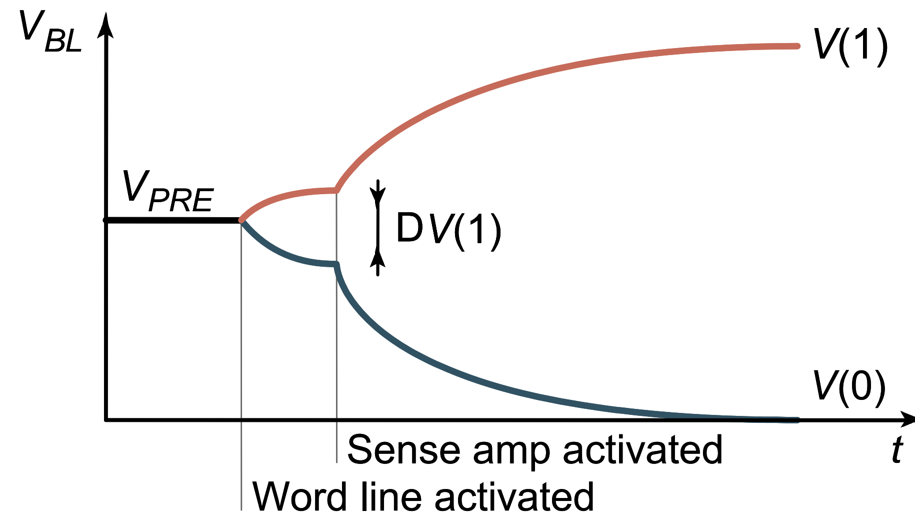
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out
- DRAM memory cells are single ended in contrast to SRAM cells
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation
- When writing a "1" into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than VDD

Sense Amplifier in DRAM

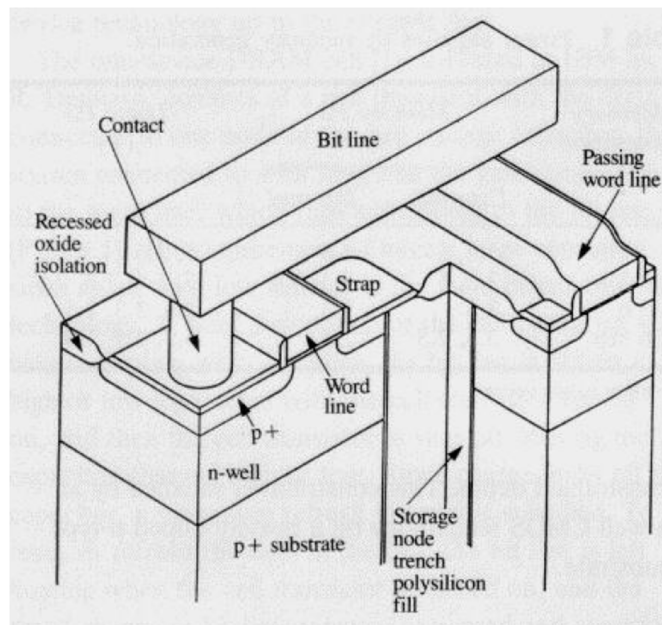
- sense amp enabled with SE
- Initialized in its meta-stable point with EQ
- Once adequate voltage gap created, positive feedback quickly forces output to a stable operating point

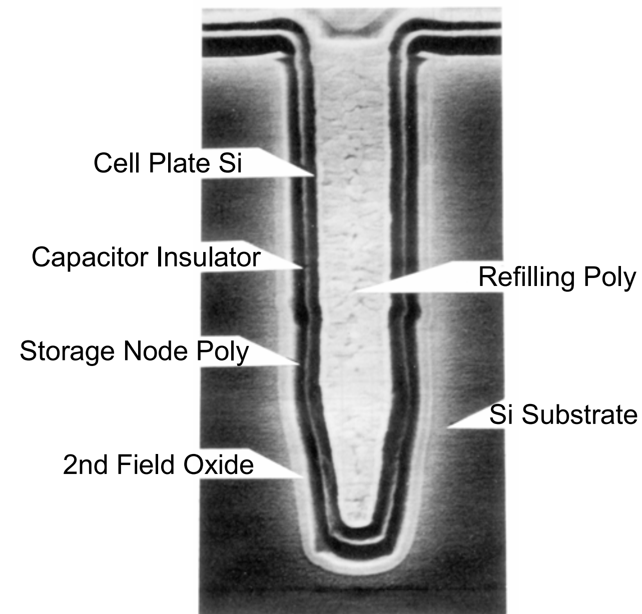




DRAM Technology – Trench Capacitor

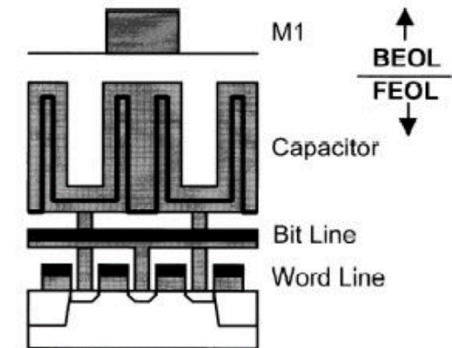
- Capacitor is the trench under select line
- The sidewalls and bottom of the trench are used for capacitor
- Trench is up to 5um deep

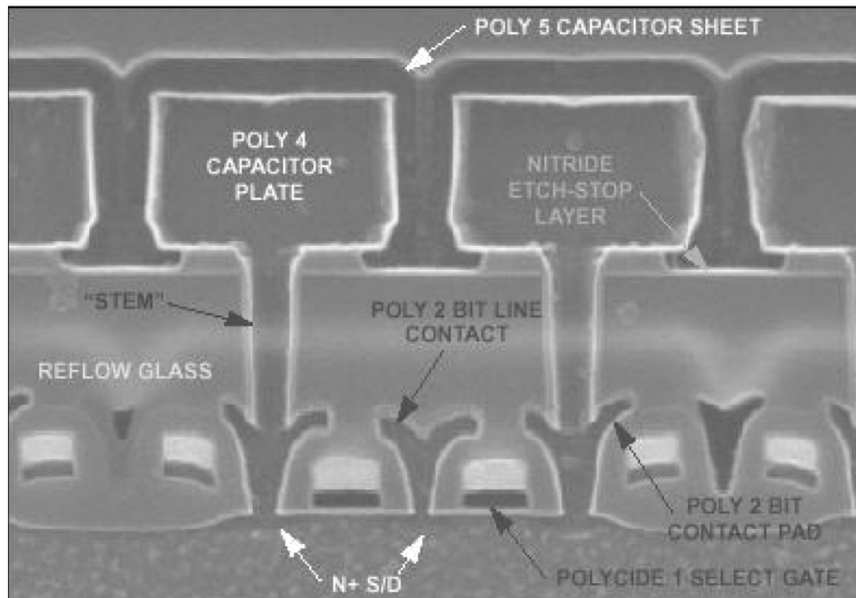


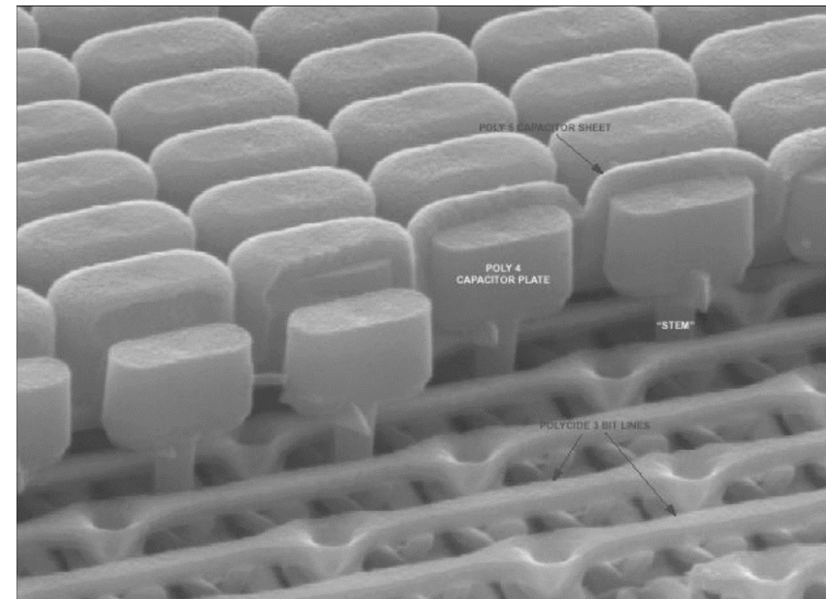


DRAM Technology – Stacked Capacitor

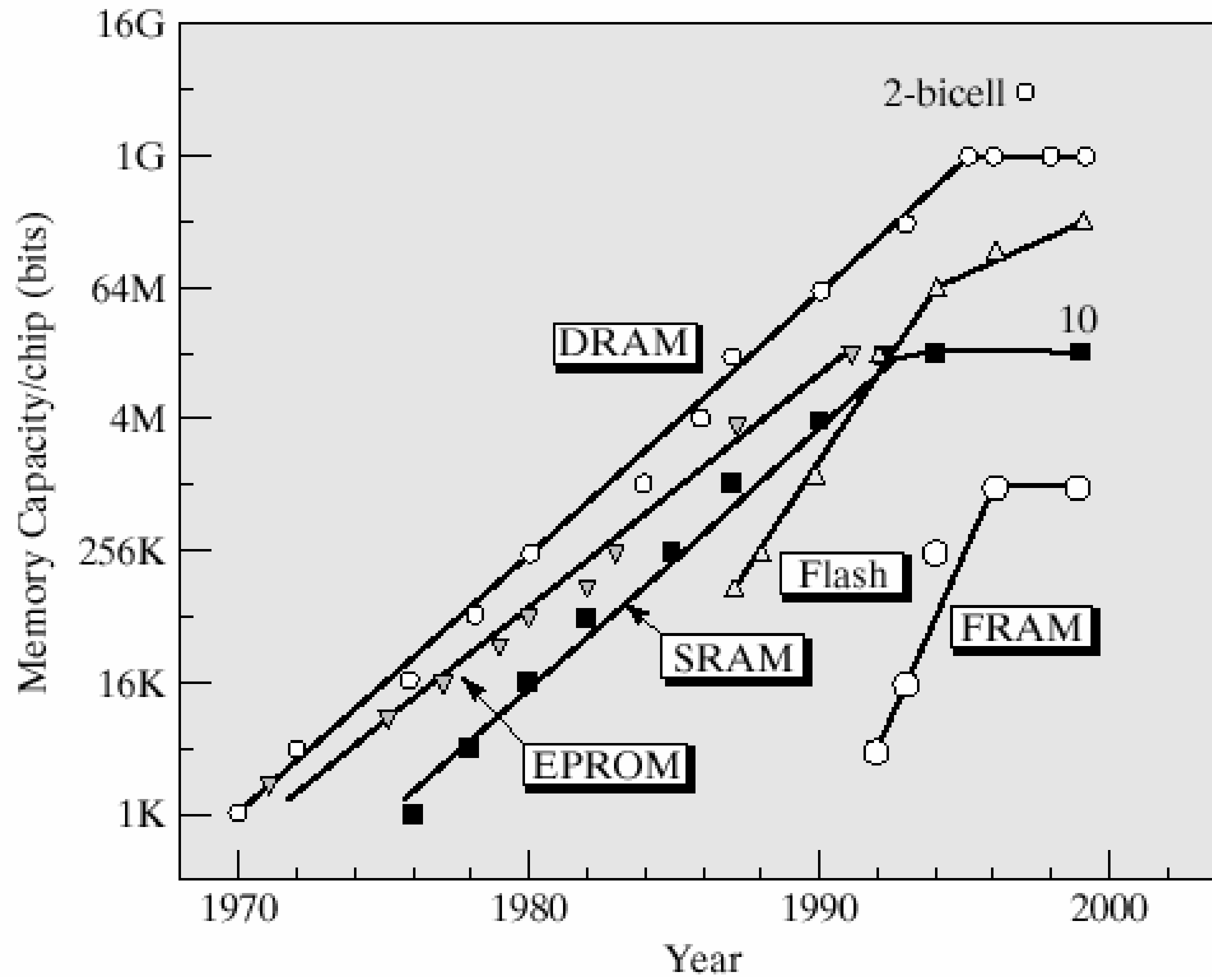
- Capacitor is above select transistor
- Polysilicon vias to polysilicon Plates







Semiconductor Memory Trends



ECE520 – Final Review

- To prepare for the exam, you can find some problem sets on the textbook's website at http://bwrc.eecs.berkeley.edu/IcBook/index.htm
- The final exam will be held next Wednesday, May 6th 2015 in the same room (ECE 310) at ***10:00AM***
- Good luck on your final exam!