ECE520 – VLSI Design

Lecture 3: More MOS Physics

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Review of Last Lecture

- "Static Parameters of Long Channel MOSFET"
- MOSFET Operational Regions
  - Cutoff region
  - Depletion region
  - Inversion region
  - Linear region (inversion)
  - Saturation region (inversion)
- Basic MOSFET Parameters
  - Threshold voltage
  - Body effect
  - Channel length modulation

Today's Lecture

- "Dynamic Parameters of Long Channel MOSFET"
- **MOSFET Parasitic Capacitances**
  - **Overlap capacitances**
  - **Channel capacitances**
  - **Junction capacitances**

Threshold Voltage Equation (Correction!)

Zero body bias threshold voltage:

$$V_{T0} = \varphi_{ms} + 2\varphi_F + \frac{\sqrt{2qN_A\varepsilon_{si}\left|2\varphi_F\right|}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Where: $\varphi_F = \frac{KT}{q} Ln\left(\frac{N_A}{n_i}\right)$ **and** $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Threshold voltage with body bias:

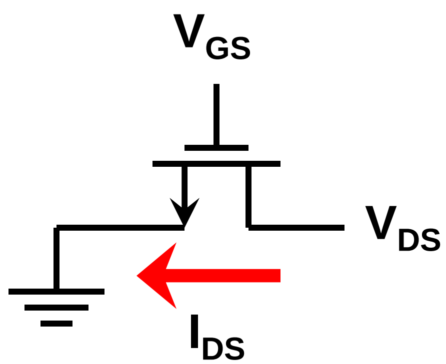
$$V_T = V_{T0} + \gamma\left(\sqrt{\left|2\varphi_F - V_{BS}\right|} - \sqrt{\left|2\varphi_F\right|}\right)$$

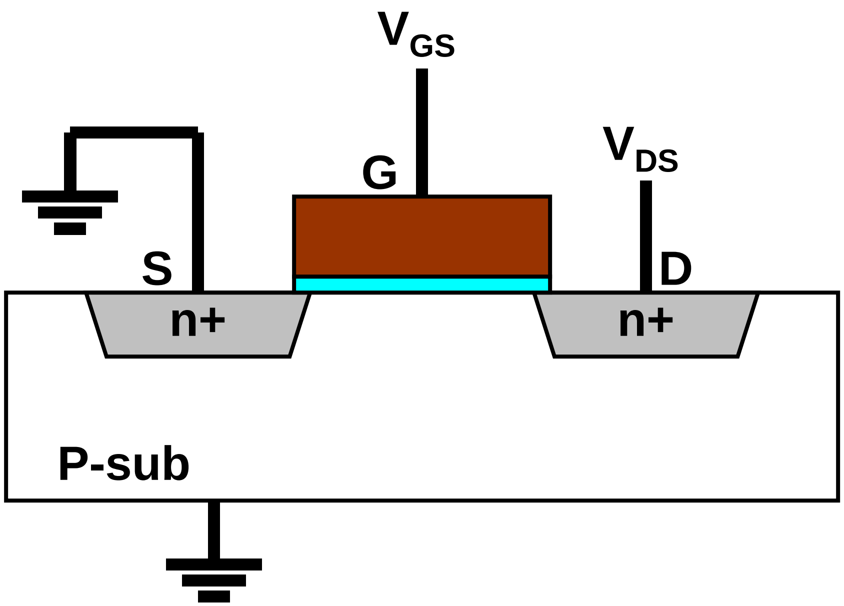
Where: $\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$

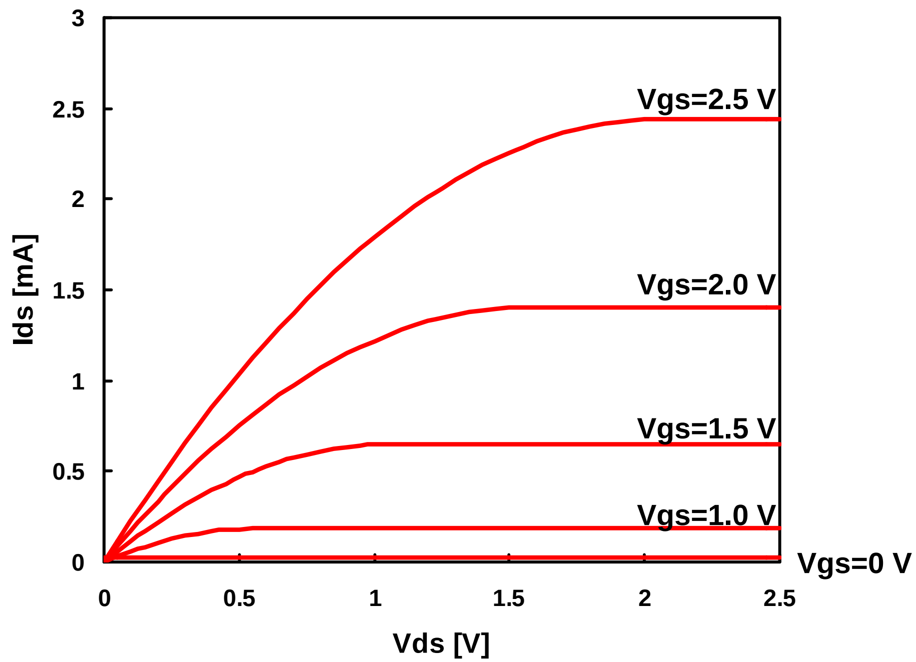
Important Facts:

- **Body bias increases threshold voltage**
- **Threshold voltage is positive for normal NMOS**
- **Threshold voltage is negative for normal PMOS**

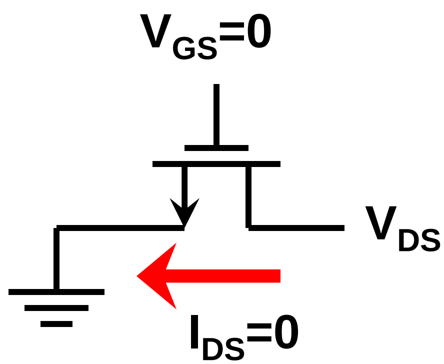
I-V Characteristic of MOSFET

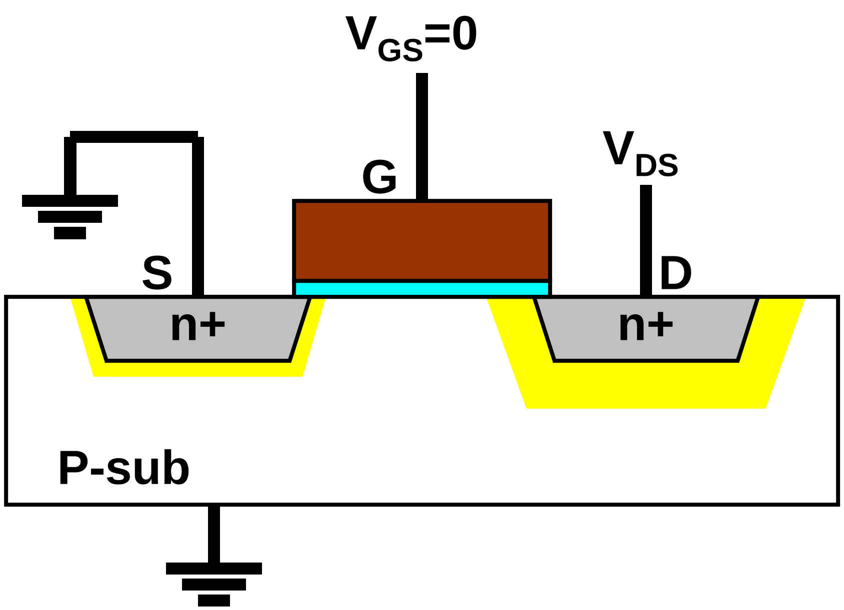


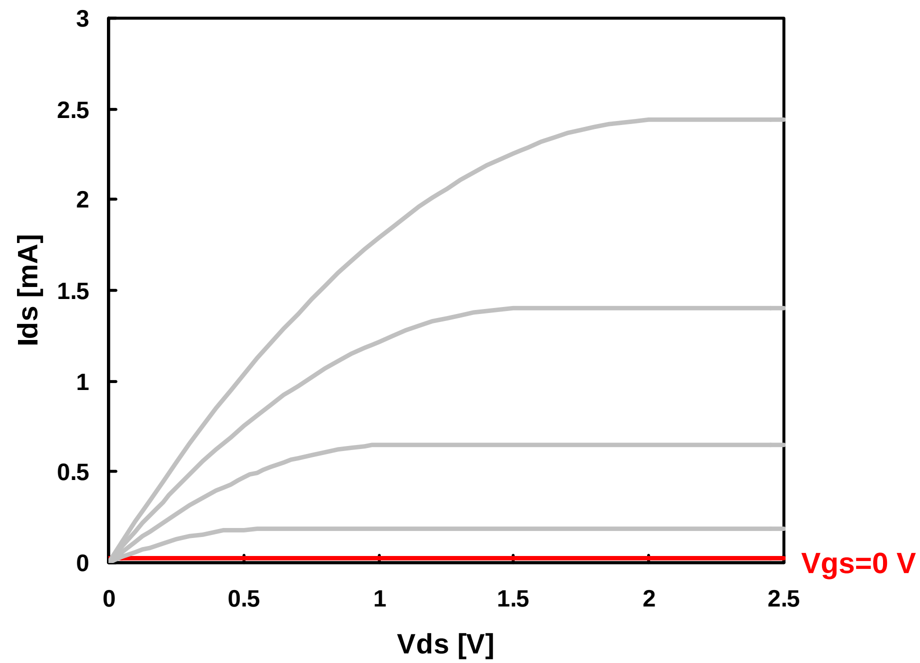




Cutoff Region



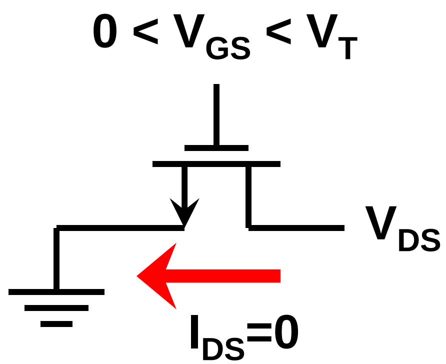


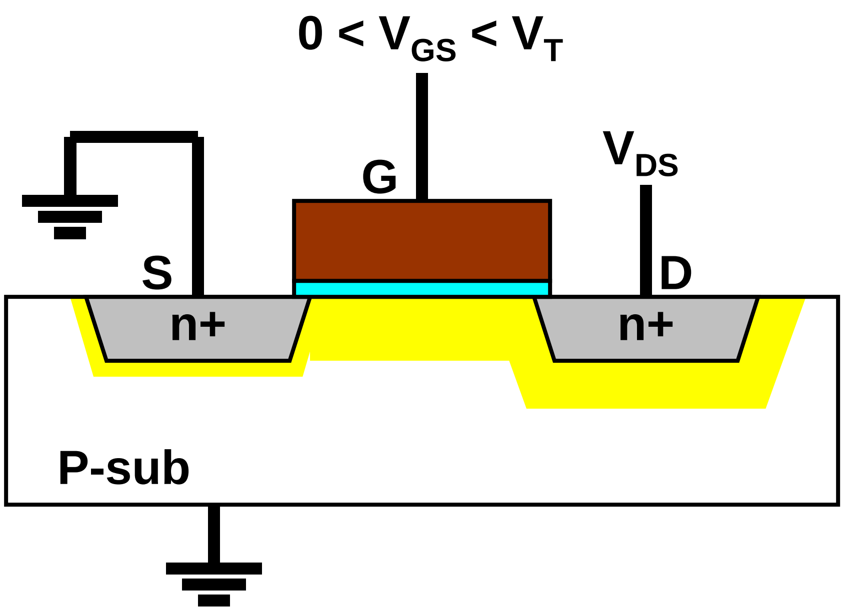


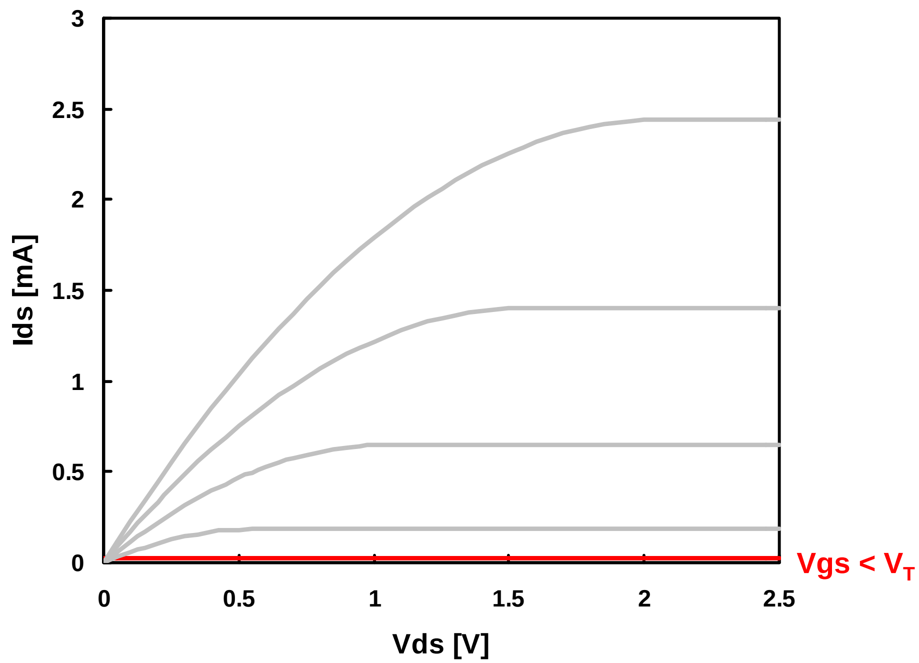
When: $V_{GS} = 0$

$I_{DS} = 0$

Depletion Region



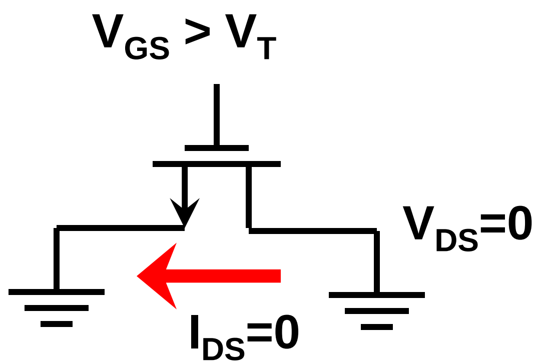


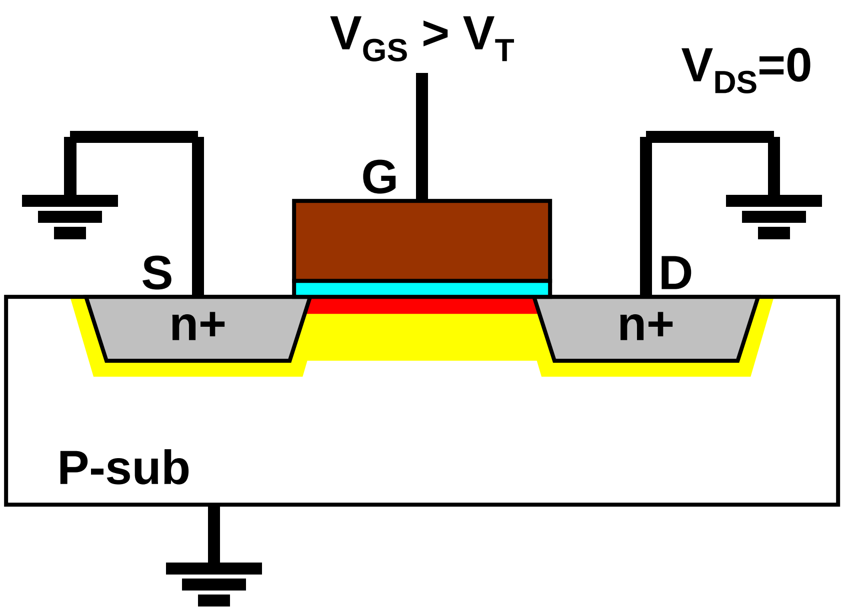


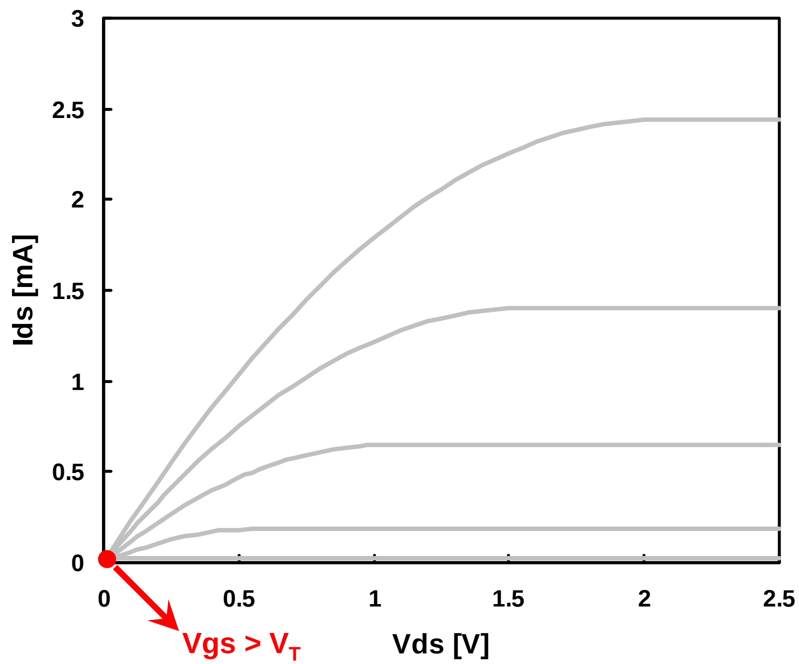
When: $V_{GS} < V_T$

$I_{DS} = 0$

Inversion Region



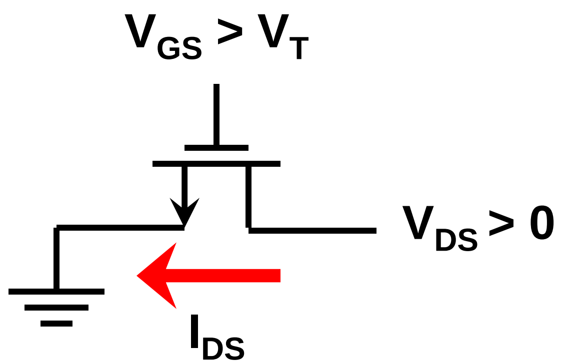


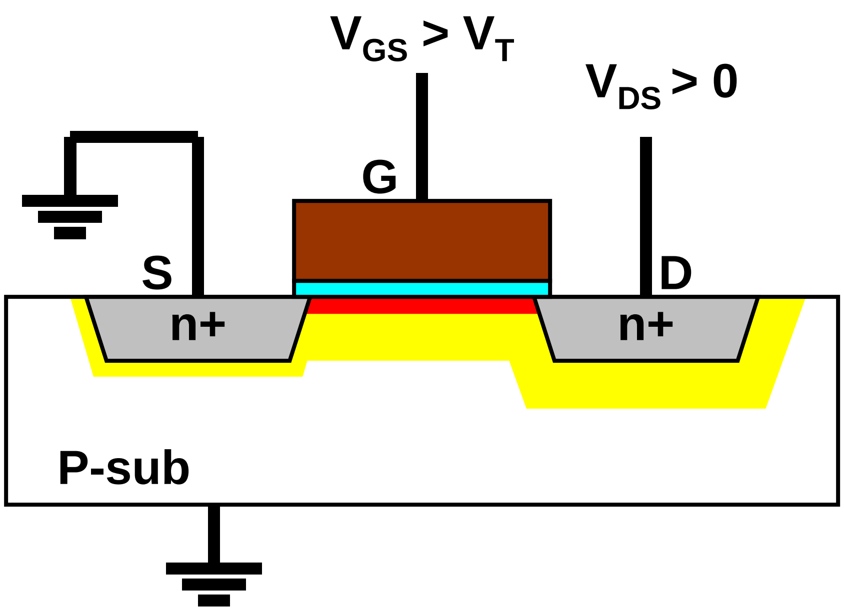


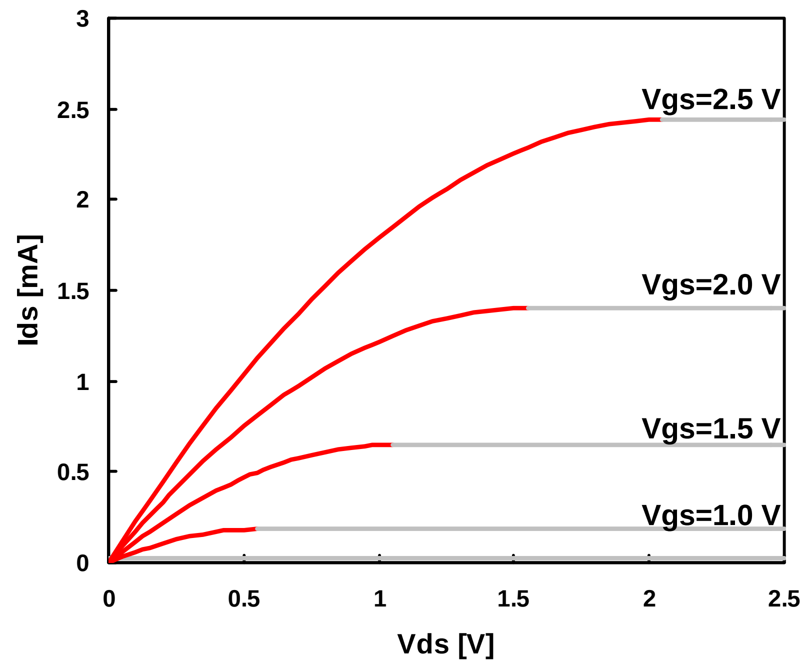
When: $V_{DS} = 0$

$I_{DS} = 0$

Linear Region (inversion)



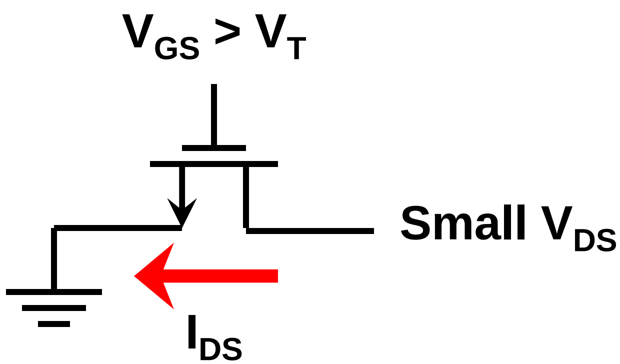


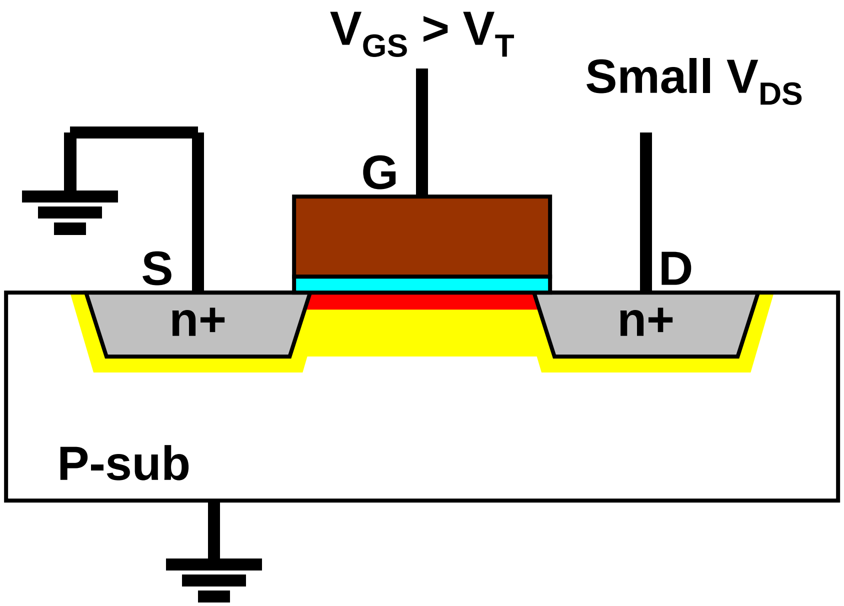


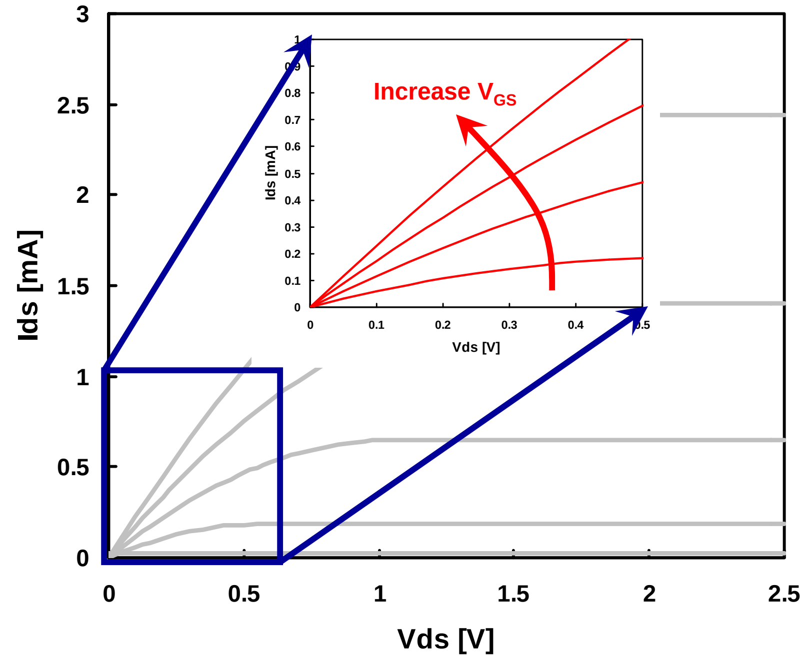
When: $V_{DS} < V_{GS} - V_T$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Ohmic Region (inversion)



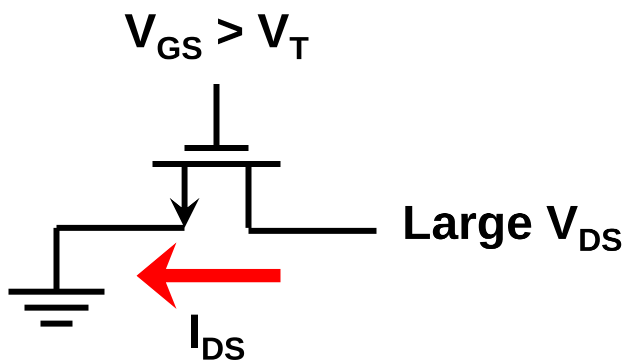


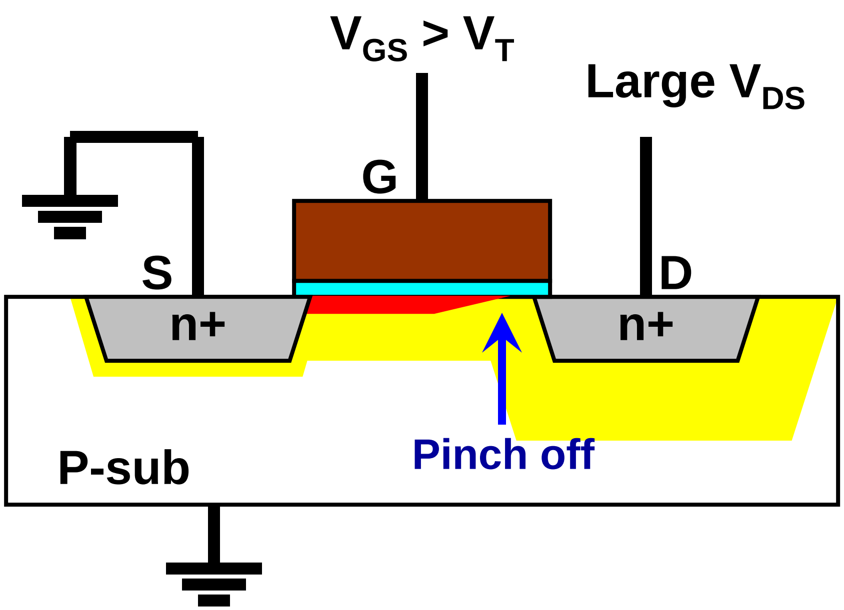


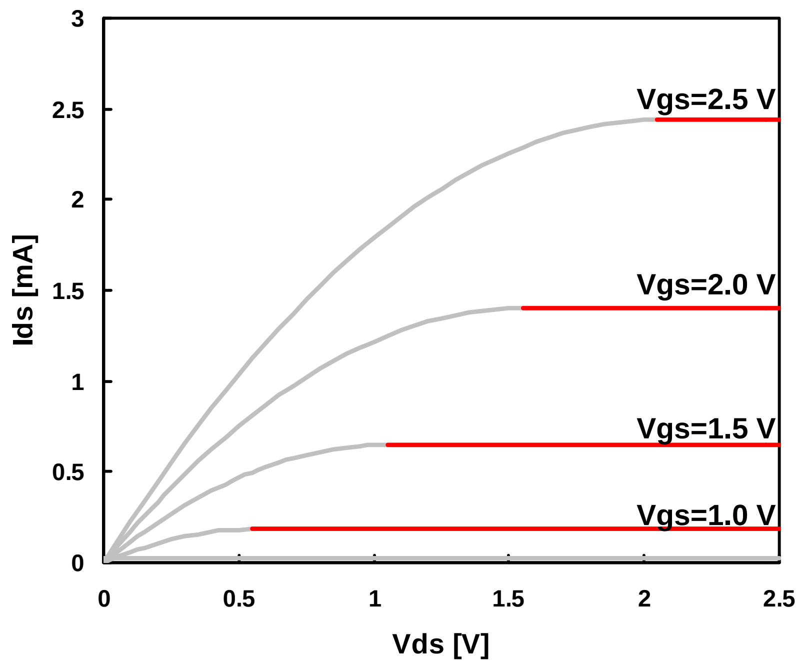
For small V_{DS} :

$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_T\right)}$$

Saturation Region (inversion)







When: $V_{DS} > V_{GS} - V_T$

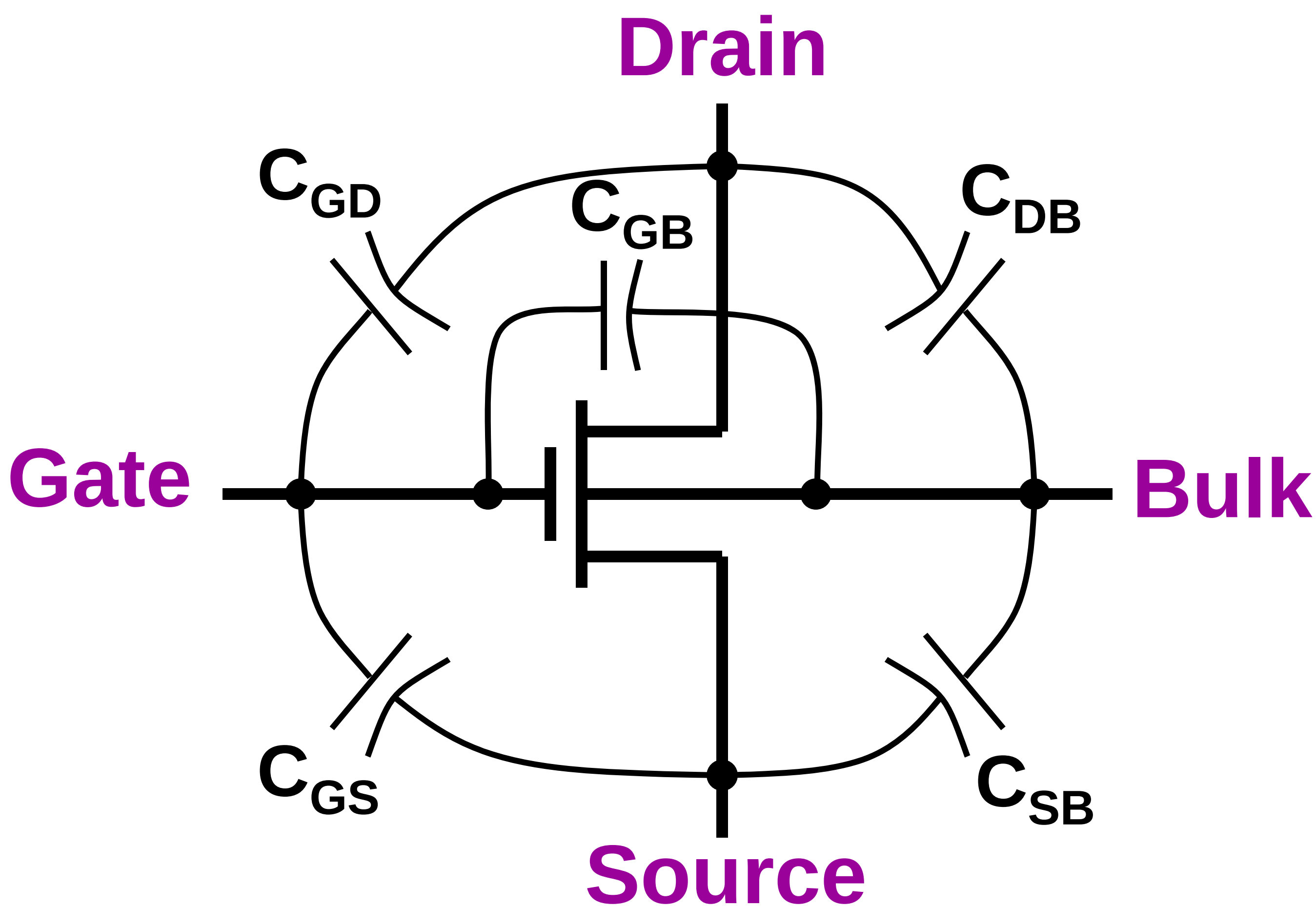
$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2$$

$$I'_{DS} = I_{DS}\left(1 + \lambda V_{DS}\right)$$

MOS Capacitance

- Delay of digital CMOS circuits depends of capacitance of MOS device
- There is a trade off between parasitic capacitance and drive strength of MOS device
  - Larger C_{ox} increases the drive strength (I_{DS} equation)
  - However, larger C_{ox} increases the device parasitic capacitance
- MOS parasitic capacitance includes
  - Overlap capacitances
  - Channel capacitances
  - Junction capacitances
- Between almost every two terminals of MOS device, there is a source of parasitic capacitance

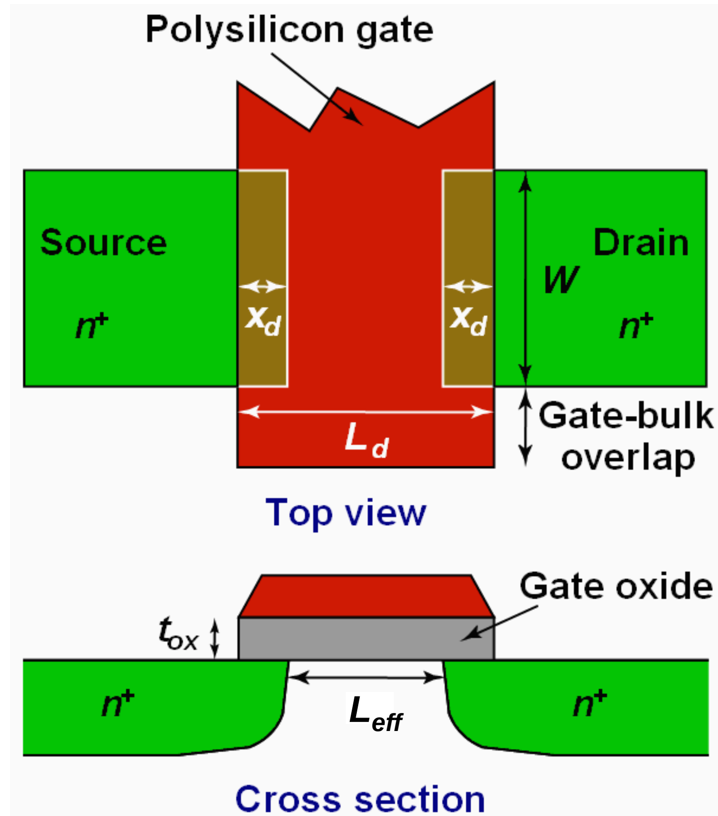
MOS Parasitic Capacitances



Overlap Capacitances

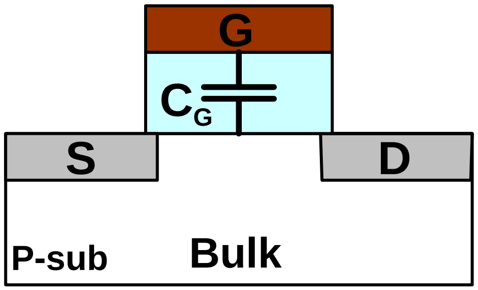
- Because of the lateral S/D diffusion, there is an overlap between gate and S/D junctions
- This overlap capacitance is a constant linear capacitance

$$C_{GSOV} = C_{GDOV} = WC_{ox}X_d$$

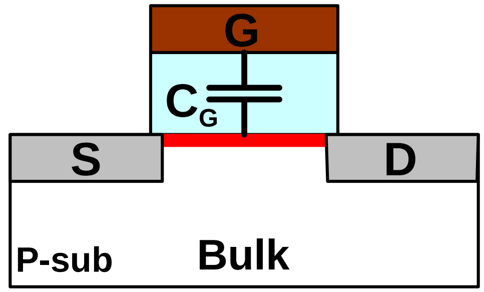


Channel Capacitances

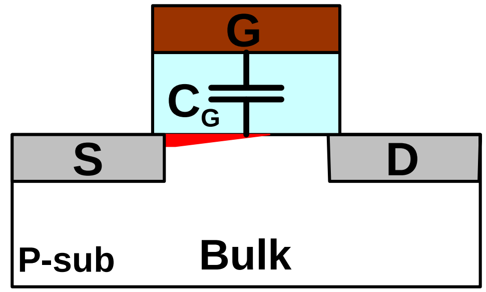
- Channel capacitance is a voltage dependent and non-linear capacitance



Cutoff Region



Linear Region

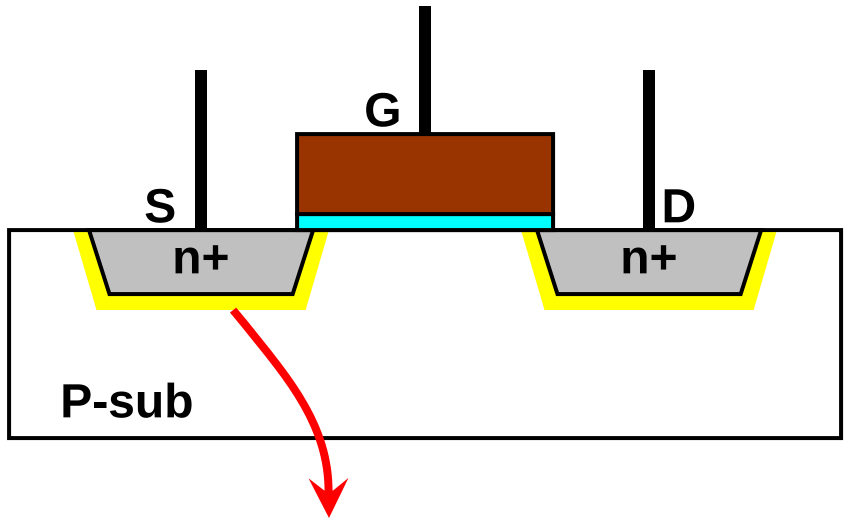


Saturation Region

Operation Region	C_{GBCH}	C_{GSCH}	C_{GDCH}
Cutoff	$C_{OX}WL_{eff}$	0	0
Linear	0	$\frac{1}{2}C_{OX}WL_{eff}$	$\frac{1}{2}C_{OX}WL_{eff}$
Saturation	0	$\frac{2}{3}C_{OX}WL_{eff}$	0

Junction Capacitances

- Junction capacitance is the *depletion region* capacitance of S/D
- It is a voltage dependent capacitance (remember reverse biased diode)

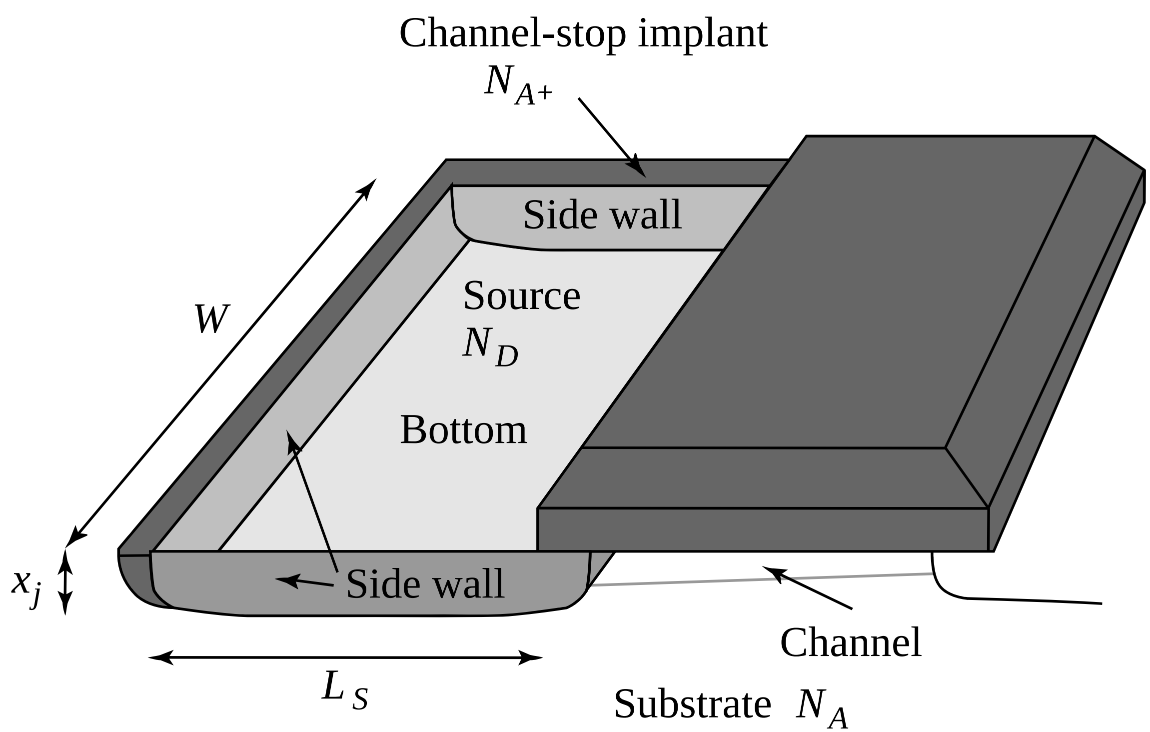


$$C_j = \frac{C_{j0}}{\left(1 - V_{SB}/\varphi_0\right)^m}$$

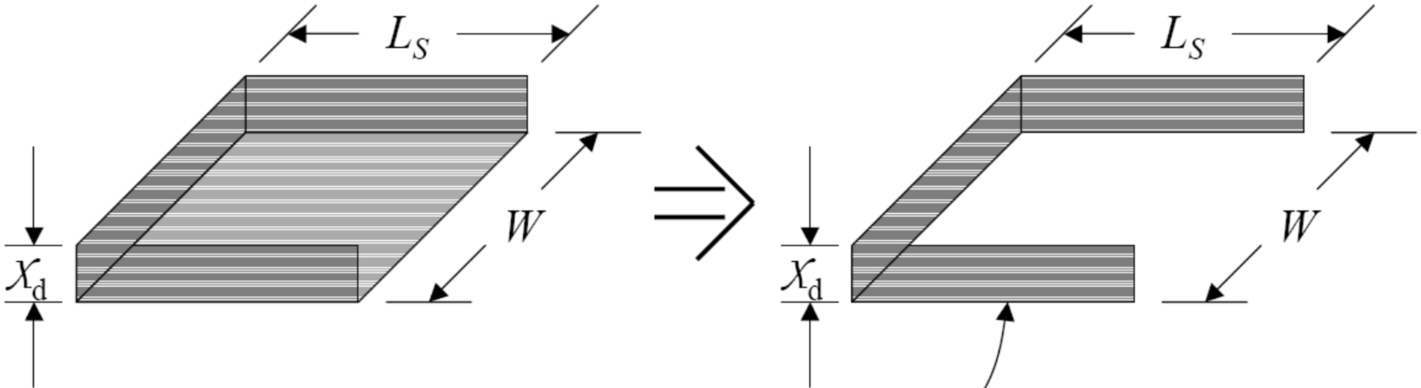
$$C_{j0} = A_D \sqrt{\left(\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}\right) \varphi_0^{-1}} \qquad \varphi_0 = \frac{KT}{q} Ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Junction Capacitance Components

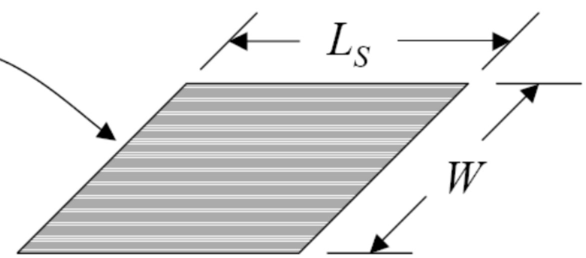
- The Junction capacitance of bottom plate is treated separately from the three non-gate edges
- The gate edge is often ignored since it is part of the conducting channel
- The bottom plate is usually step graded with m=0.5
- The sidewall are step graded with m=0.33 and face the ***channel-stop implant*** which has much higher doping than substrate



Junction Capacitance Components



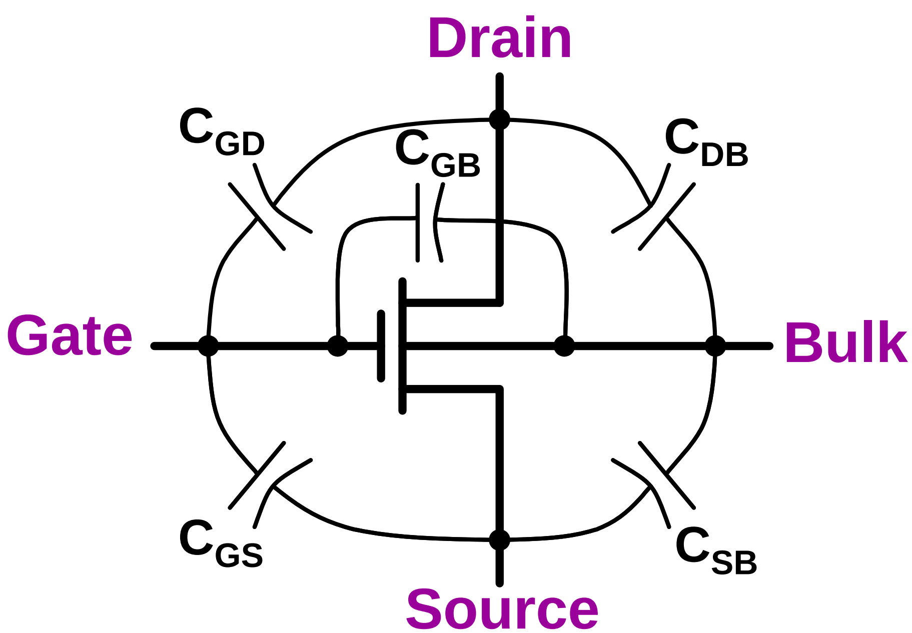
$$C_{Diff} = C_{Bottom} + C_{SW}$$



$$C_{Bottom} = C_J W L_s$$

$$C_{SW} = C_{JSW}\left(2L_s + W\right)$$

MOS Parasitic Capacitances



$$C_{GS} = C_{GSCH} + C_{GSOV}$$

$$C_{GD} = C_{GDCH} + C_{GDOV}$$

$$C_{GB} = C_{GBCH}$$

$$C_{SB} = C_{Sdiff}$$

$$C_{DB} = C_{Ddiff}$$