ECE520 – VLSI Design

Lecture 5: Basic CMOS Inverter

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Review of Last Lecture

- **Short Channel Effects**
  - Source-Drain resistance
  - Subthreshold conduction
  - Velocity saturation
  - Mobility degradation
  - Threshold voltage rolloff
  - DIBL effect
  - Punch through
  - Hot electron
  - Narrow channel effect
- **Device Scaling Issues**

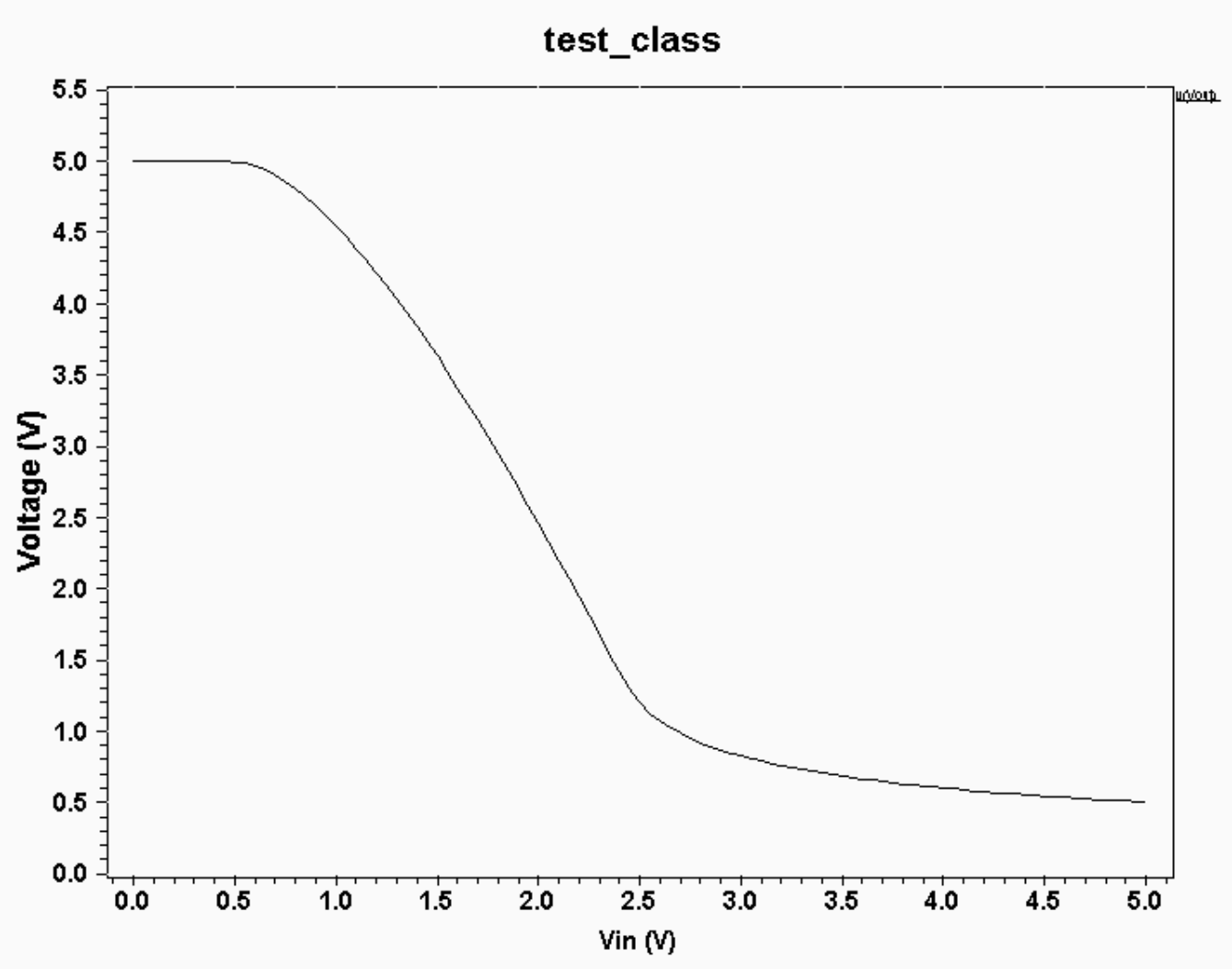
Today's Lecture

- **Overview of T-SPICE**
- **BASIC CMOS Inverter**
  - Resistive load inverter
  - VTC curves
  - Power dissipation estimation
- **Static Behavior of CMOS Inverter**
  - Switching threshold
  - Noise margin
  - CMOS Voltage-Transfer Characteristic (VTC)
- **CMOS Inverter Robustness**
  - Device variations
  - V_{dd} scaling (minimum supply voltage)

Overview of TSPICE (input file)

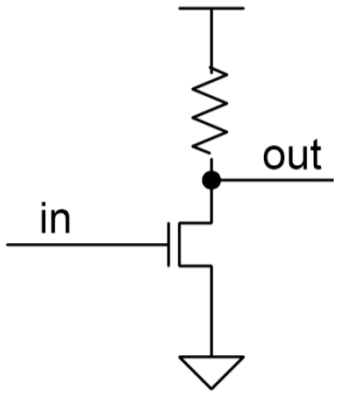
```
* Test Circuit for VLSI Class

Vdd   Vp   gnd   DC   5V
RL    Vp   Vout  10K
M1    Vout Vin   gnd  gnd CMOSN  W=8um  L=1.6um
Vin   Vin  gnd   DC  5V

.DC Vin 0 5 0.05
.plot Vout
.include 'device_model.modlib'
.end
```

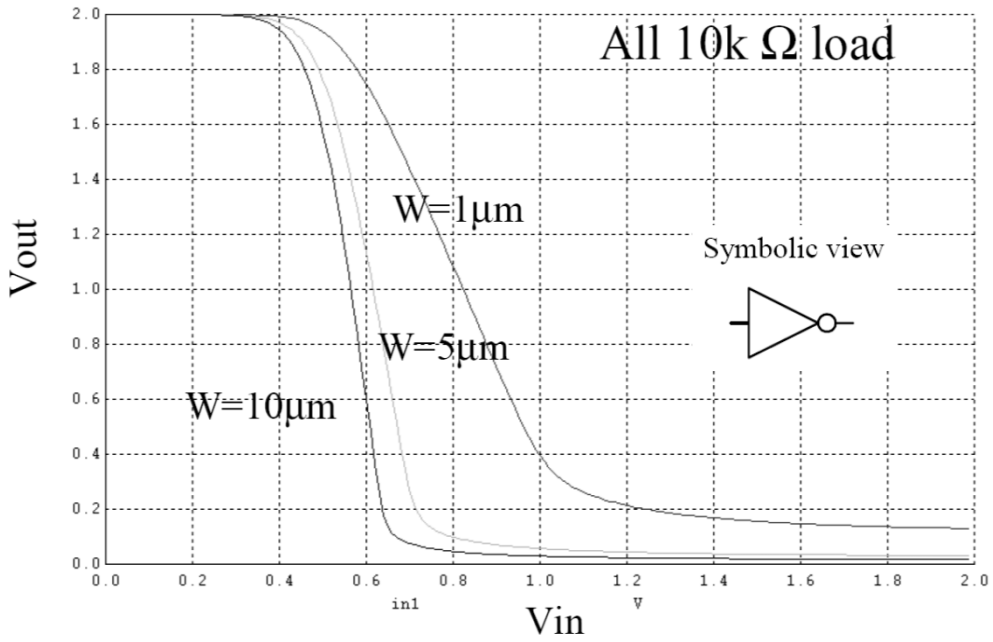
Overview of TSPICE (output waveform)



Resistive Load Inverter

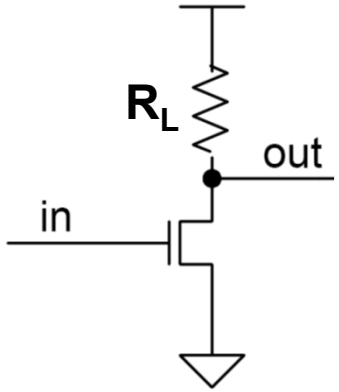
- A resistive load inverter consists of a pull down NMOS and a pull up resistor
  - Voltage Transfer Characteristic (VTC) is a function of transistor size and resistor value
  - A good inverter provide a fast transition in VTC curve





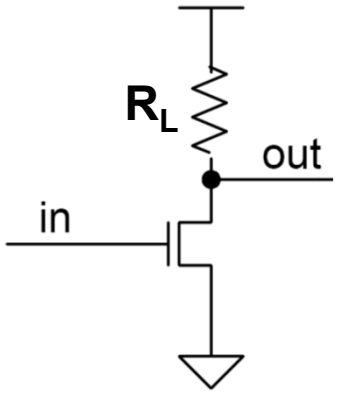
Resistive Load Inverter Design

- The pull up resistor must be calculated to maintain a specific low level voltage (V_{OL}) at the output
- Example:
  - $K'_n = 100\ uA/V^2$
  - $V_{T0} = 0.7\ V$
  - $V_{OL} = 0.25\ V$
- How to compute R_L as a function of (W/L)?
- How much is R_L for (W/L)=5 ?



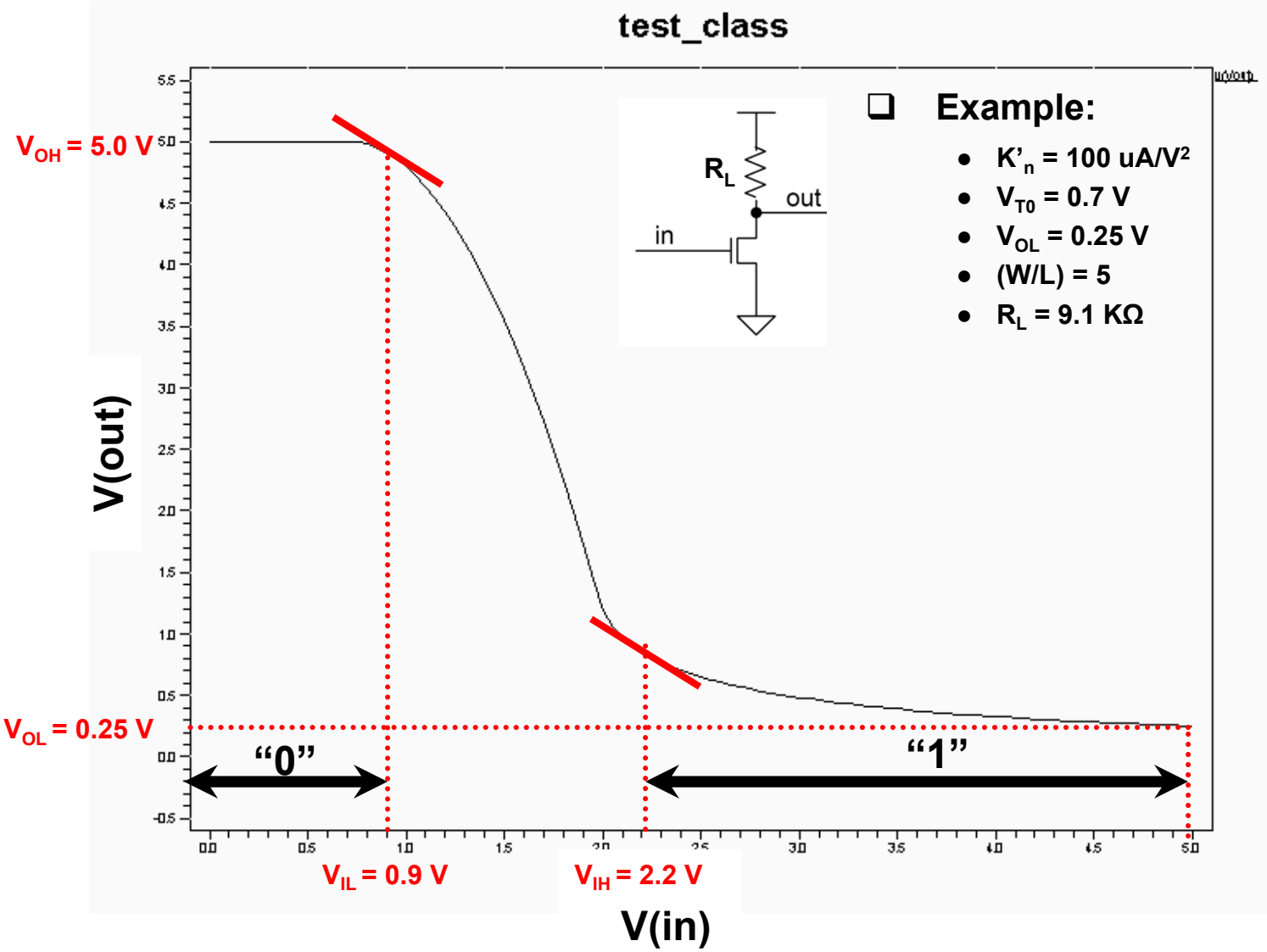
Power in Resistive Load Inverter

- When the output is high, there is no current drawn from V_{DD}
- When the output is low, a DC current is drawn from V_{DD}
- Assuming probability is 50% for logic high and logic low
- How to compute Power in the previous example?

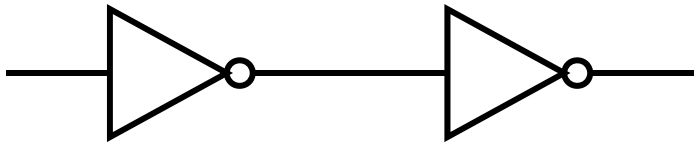


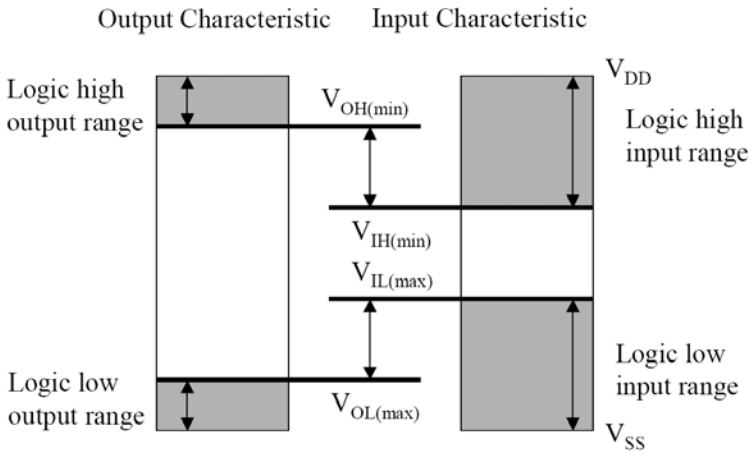
- How much is the power for a design with 100K similar resistive load logic gate?

Review of Resistive Load Inverter



Noise Margin





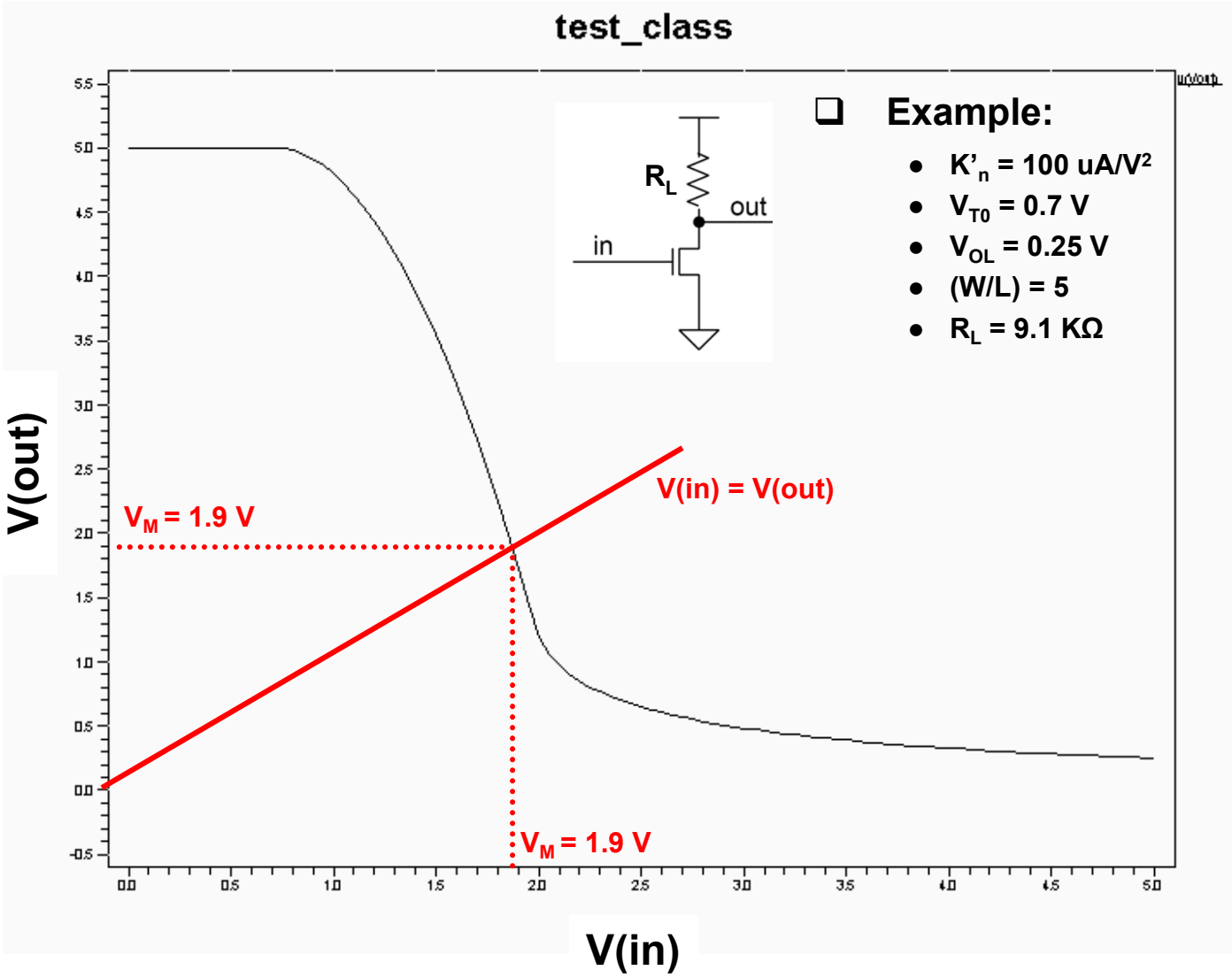
- **Noise Margin**

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

- **It is better to have:**
  - $V_{OH} = V_{DD}$
  - $V_{OL} = V_{SS}$
  - Large NM_H
  - Large NM_L

Switching Threshold Voltage

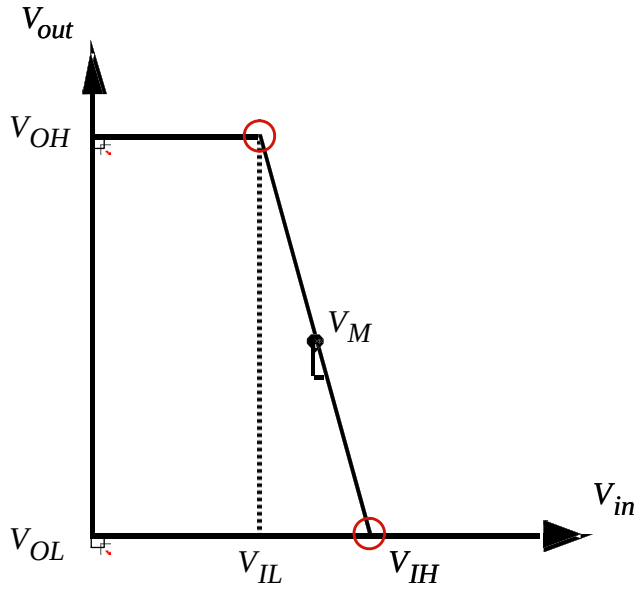


Switching Threshold Voltage Calculation

- How to compute V_M
  - Connect output to the input pin
  - Find out MOS operating region
  - Write the equations for current
  - Calculate V_M
- Example:
  - V_M in resistive load inverter

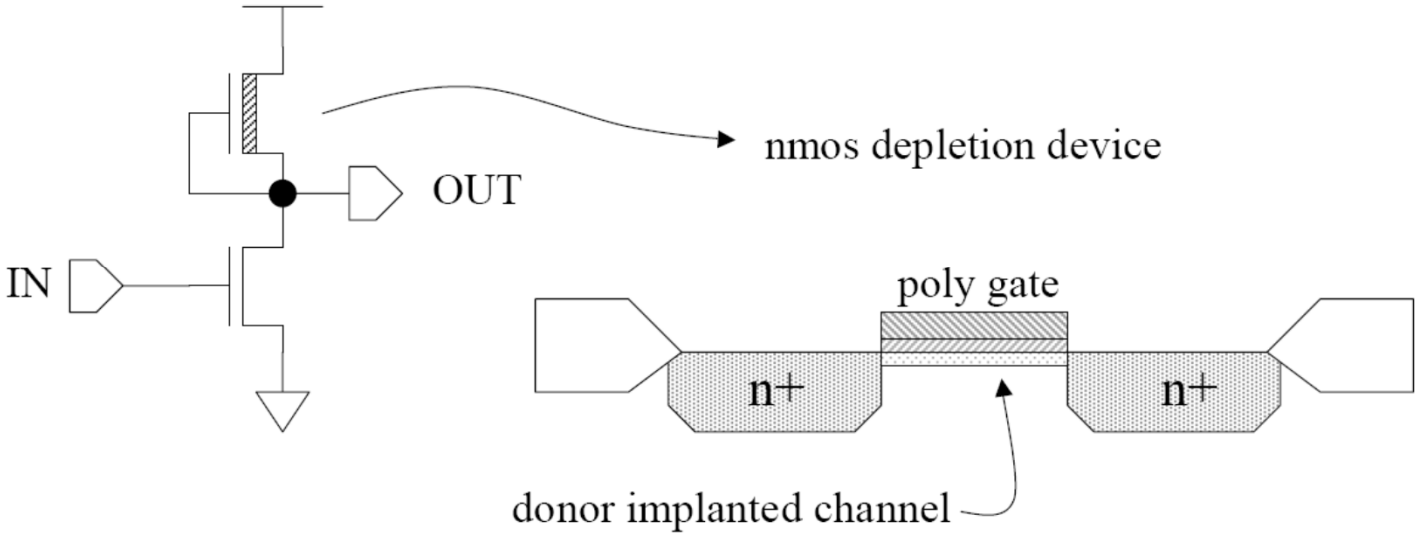
Noise Margin Estimation

- **How to compute Noise Margin**
  - Usually it is harder to compute the exact value of NM
  - Use approximation (gain factor)
  - Determine gain at V_M
  - Extrapolate V_{IL} and V_{IH}
  - V_{OL} and V_{OH} are easy to compute
- **Example:**
  - NM_L and NM_H in resistive load inverter



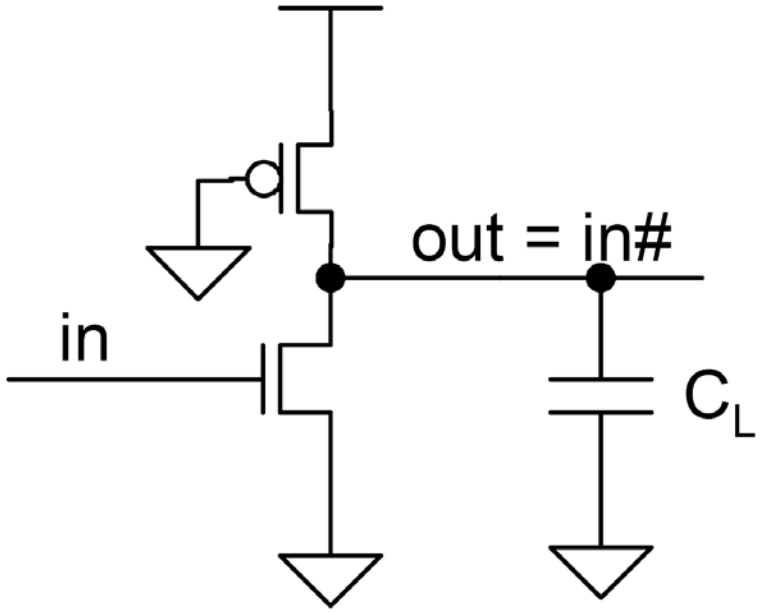
NMOS Inverter

- Large pull up resistor was a problem for resistive load inverter
- Depletion mode NMOS was an efficient way to implement a resistive pull up
  - Depletion device has an implant in the channel to give it a negative V_T and so it is always on — it was a very effective non-linear load device
  - This solved the area, but not the noise margin or power problems



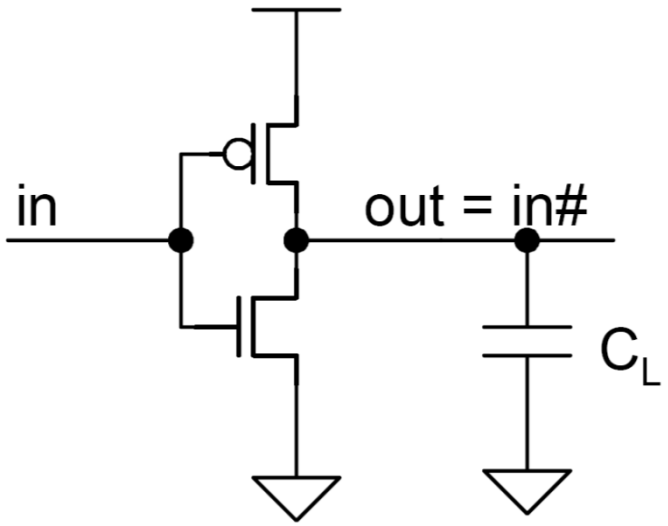
Pseudo NMOS Inverter

- Since a resistor is so big, it's better to use a single PMOS transistor that is always on:
  - PMOS pull up
  - NMOS pull down
- Why don't we use NMOS pull up?



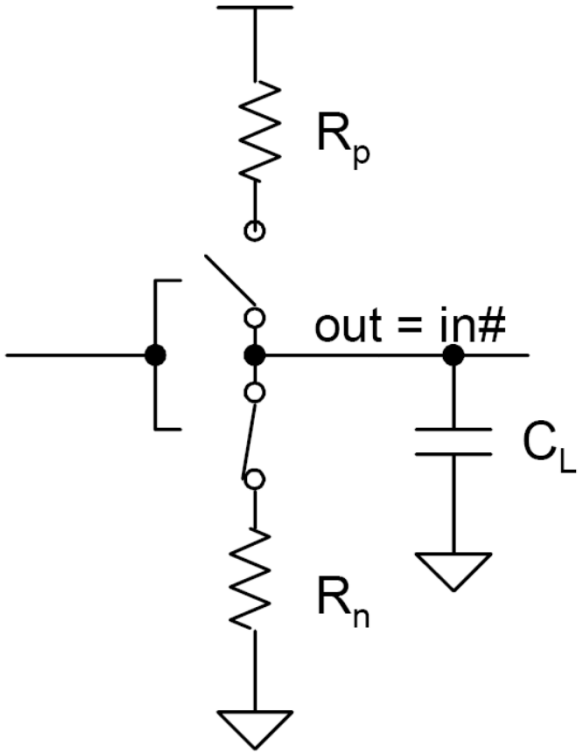
CMOS Inverter

- CMOS inverter is comprised of
  - PMOS pull up
  - NMOS pull down
- Advantages
  - No direct path from V_{DD} to GND (zero static power - except for leakage)
  - Better noise margin (Rail-to-rail output swing)
  - Ratio-less logic (output level not depend on gate size)
  - Always finite resistance to V_{DD} or GND
  - Very high input impedance

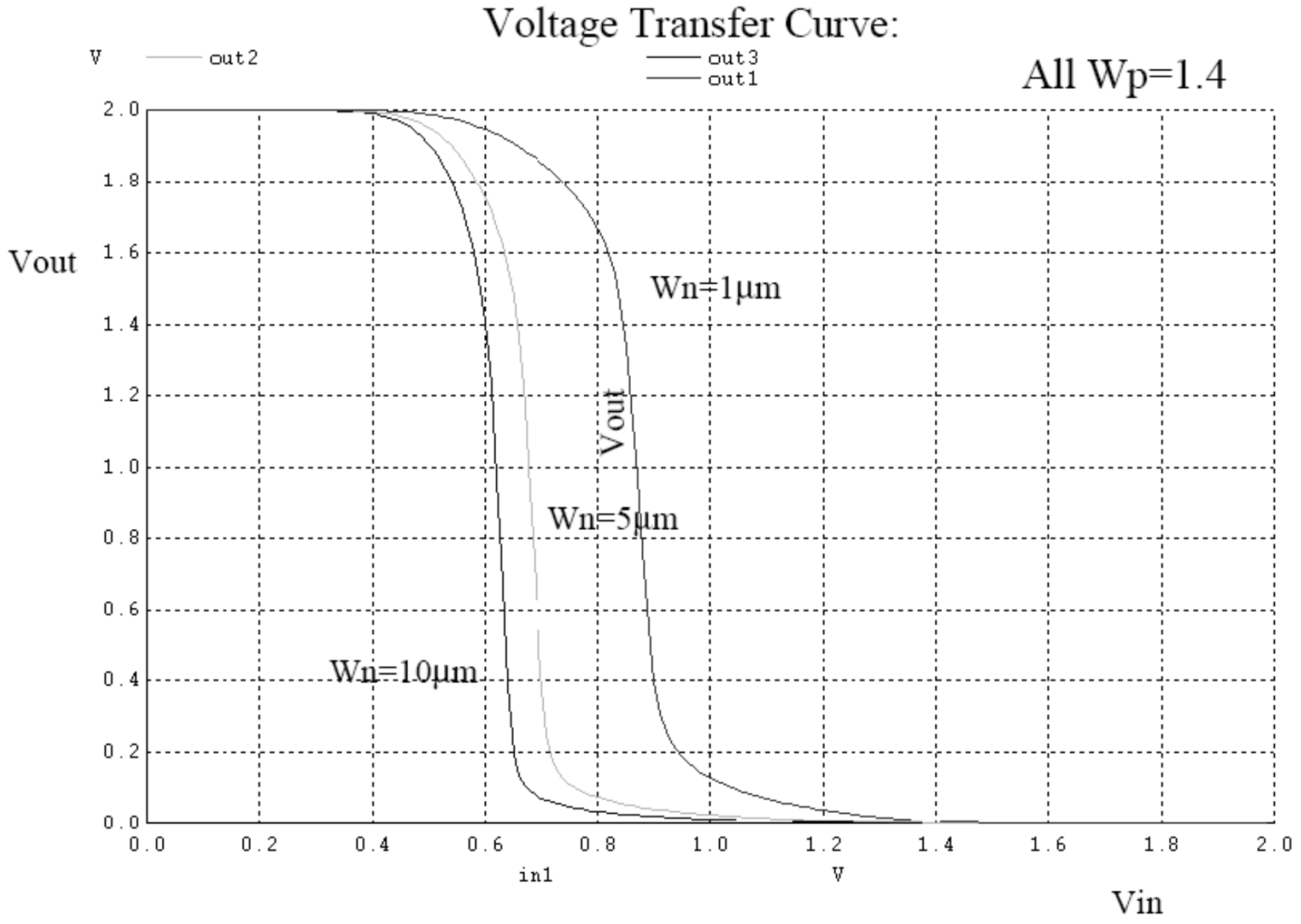


Switching model of CMOS Inverter

- Treat each transistor as either on or off
- Each transistor has an on resistance
  - This isn't a bad model as long as the input transition is quite a bit faster than the output transition and it's very intuitive
- Delay of the gate depends of the effective transistor resistant and load capacitance



CMOS Inverter VTC



CMOS Inverter Switching Threshold

- **How to compute V_M in CMOS logic gate?**
  - **Use the previous method to compute V_M**
  - **Assume velocity saturation model**

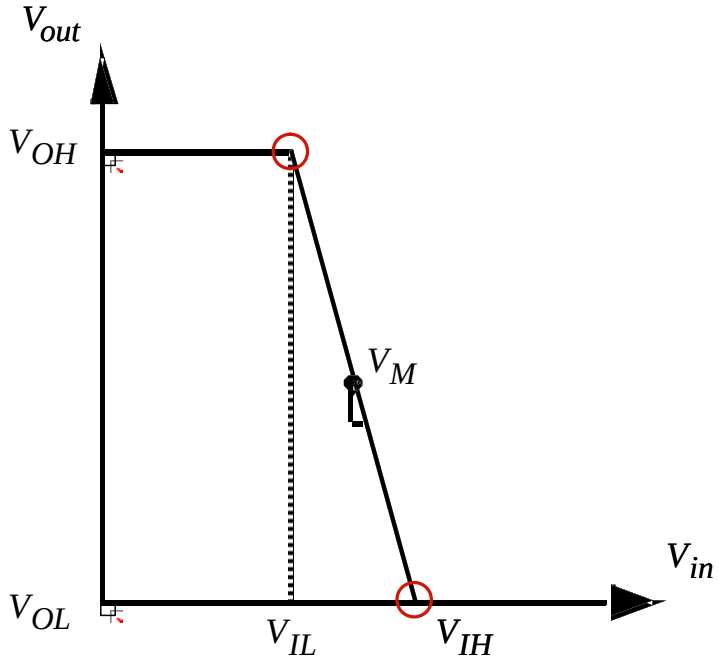
$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

  - **Assume long channel model**

$$V_M = \frac{\sqrt{\frac{k_p}{k_n}} V_{DD} + V_t\left(1 - \sqrt{\frac{k_p}{k_n}}\right)}{\left(1 + \sqrt{\frac{k_p}{k_n}}\right)}$$

CMOS Inverter Noise Margin

- **How to compute noise margin in CMOS logic gate?**
  - **Use the previous method to approximate Noise Margin**



$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

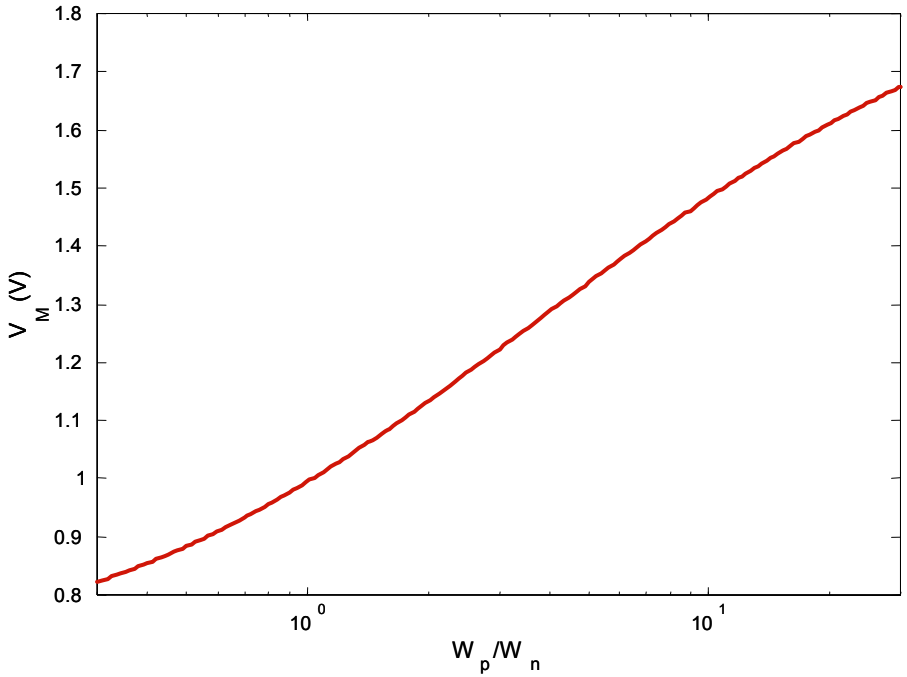
where

$$g = -\frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$\approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

Design of CMOS Inverter

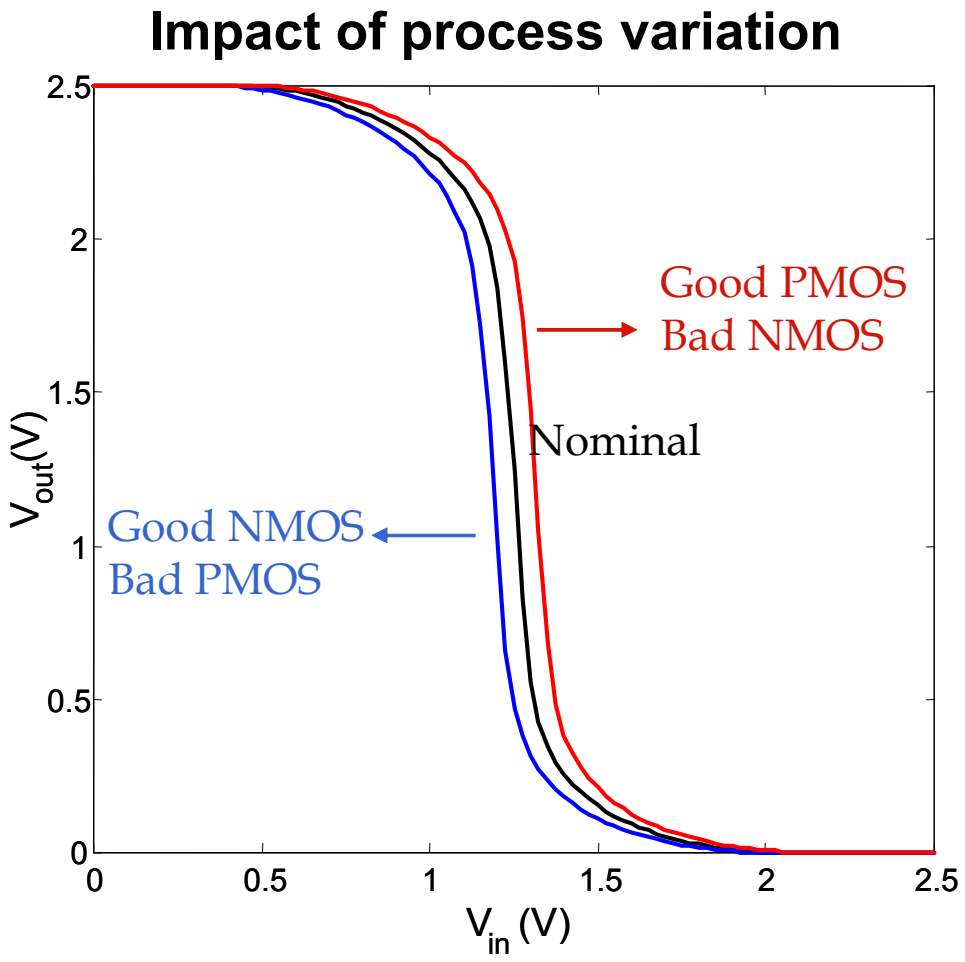
- For typical CMOS processes, μ_n = 2 to 3 times μ_p
  - To get maximum noise margin we can make $W_p = 2.5W_n$
  - We don't actually implement this ideal case…
- Switching threshold voltage is not sensitive to (W_p/W_n) ratio
  - This means NM's are not seriously compromised by (w_p/w_n) ratios not equal to 1



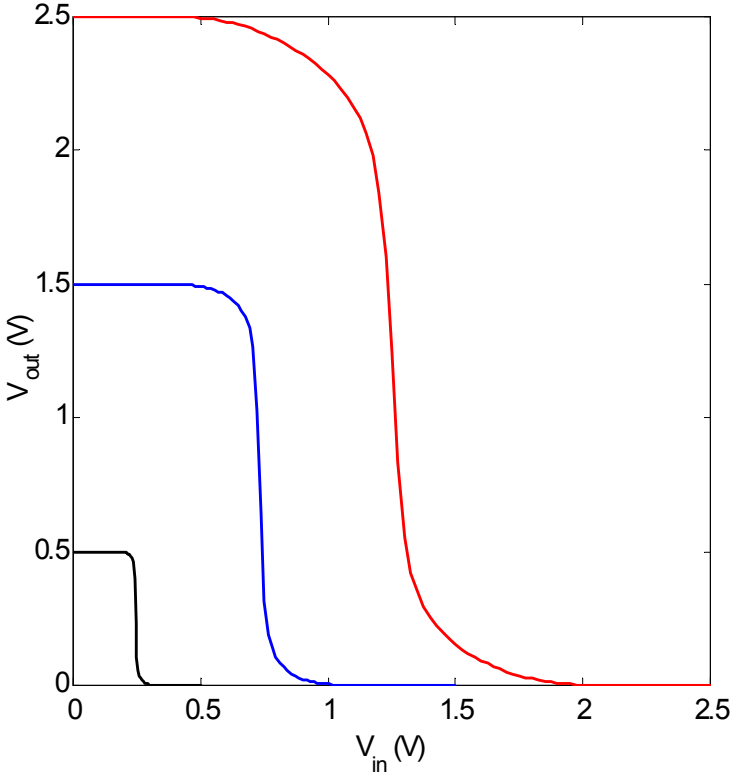
What (W_p/W_n) Ratio to Use?

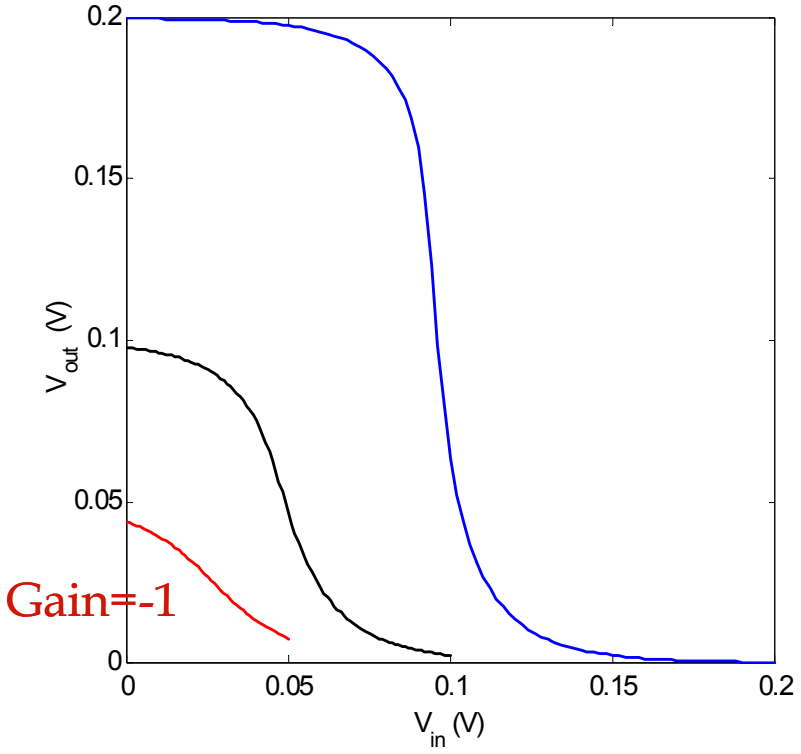
- We really want the best speed/power ratio
- At $W_p = 2.5\ W_n$ the rise and fall times for the gate (assuming that they are equal at the input) will be equal
- Each gate is a load for a preceding gate
- As we widen the PMOS we slow down the previous gate
  - Every increment of width adds C
  - C is important term in power (the one we can control!)
- It turns out that it's best to use a ratio of about 1.5 rather than 2.5-3 that would give us equal rise and fall times
- In this case, NMOS are faster and PMOS slower, but the faster falling input helps make up for the slower rising output and the overall C

Robustness of CMOS Inverter



Minimum Supply Voltage





Minimum Supply Voltage

- Once V_{DD} drops below threshold voltage, the transistors operate in the subthreshold region.
- Using equation for subthreshold region we can prove:

$$g = -\left(\frac{1}{n}\right)\left(e^{V_{DD}/2\varphi_T} - 1\right)$$