ECE520 – VLSI Design

Lecture 7: CMOS Manufacturing Process

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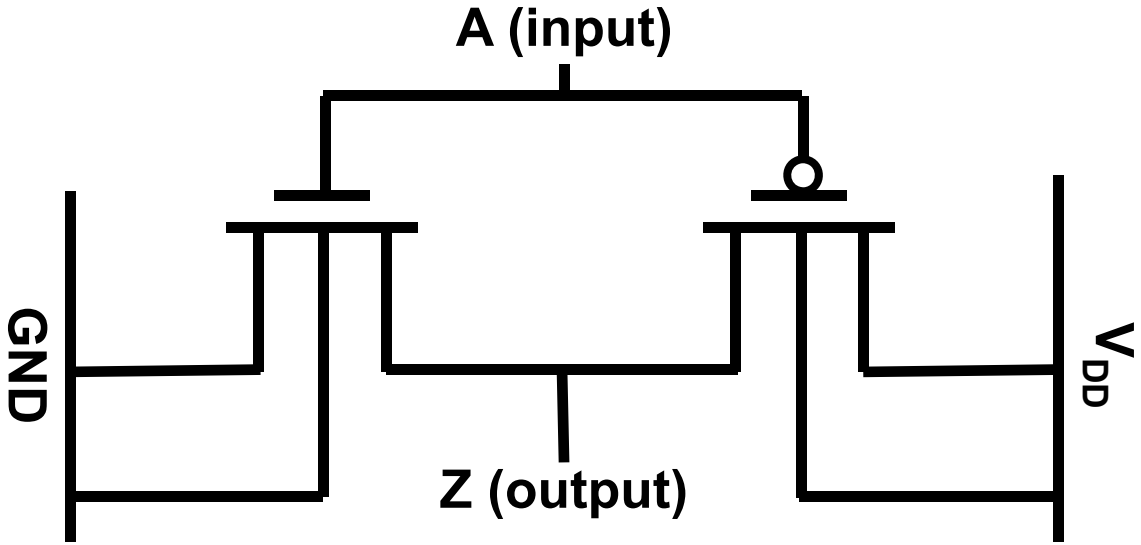
Review of Last Lecture

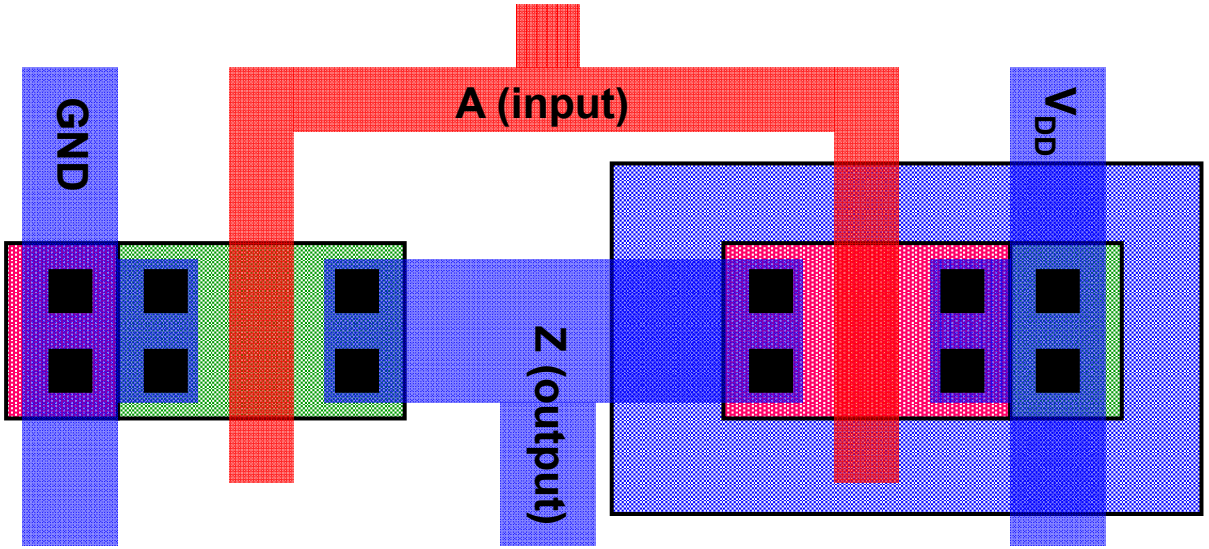
- **Dynamic Behavior of CMOS Inverter**
  - **Computing the capacitances**
  - **Propagation delay model**
  - **Dynamic power**
  - **Power due to direct-path current**
  - **Leakage power**
  - **Some design techniques**

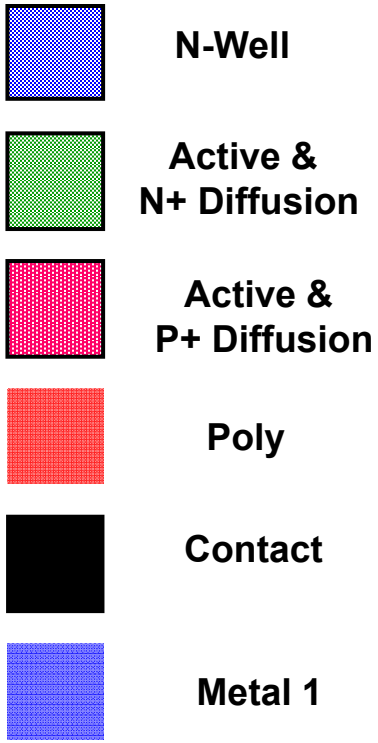
Today's Lecture

- **CMOS Manufacturing Process**
  - **Front-end Process**
  - **Back-end Process (will be covered in "interconnect" lecture)**
- **Modern CMOS Process**
  - **Salisidation**
  - **Low Doped Drain (LDD)**
  - **Shallow Trench Isolation (STI)**

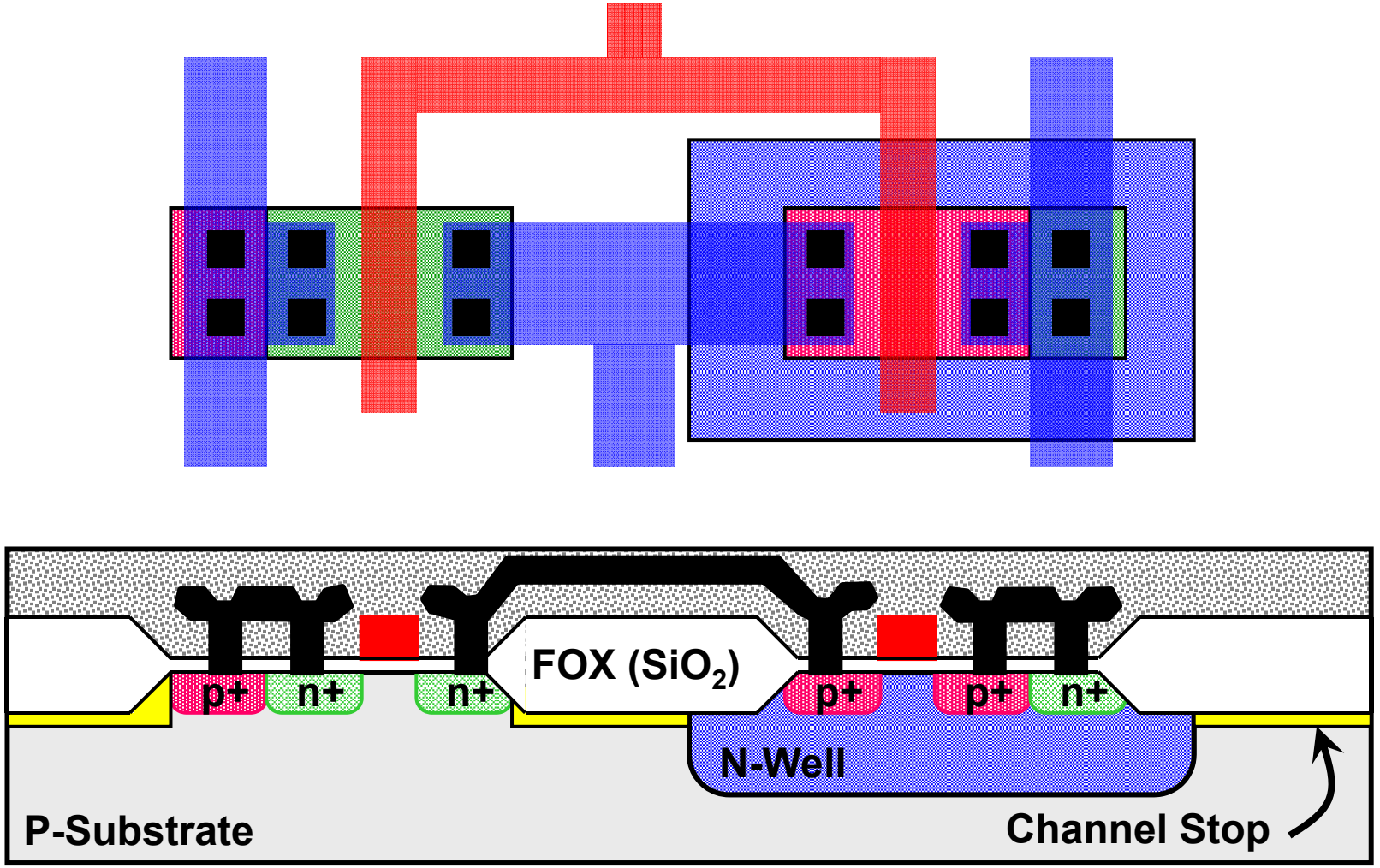
Inverter Schematic & Layout





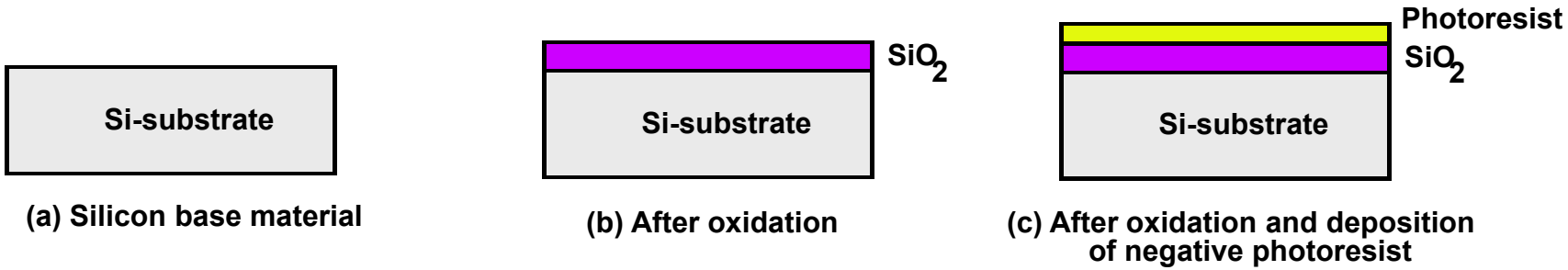


Cross Section of CMOS Inverter



Overview of Lithography

- In order to etch a window opening in a SiO_2 layer on a Si substrate the first step is to spin on a photoresist
- Photoresist is a light sensitive and acid resistant polymer
  - Positive photoresist is initially insoluble to developing agent and becomes soluble when exposed to UV light
  - Negative photoresist is initially soluble and becomes resistant to the developing agent when exposed to UV light

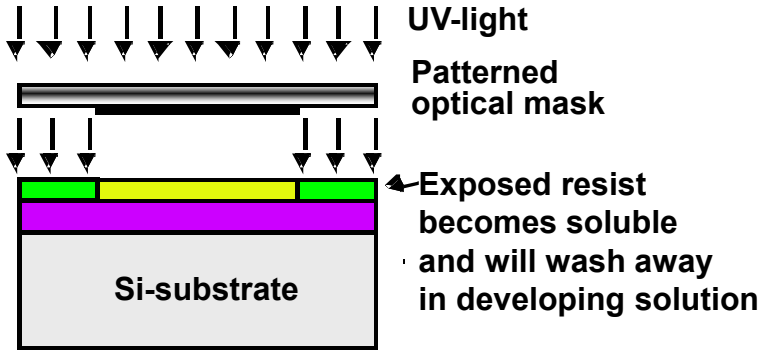


(a) Silicon base material

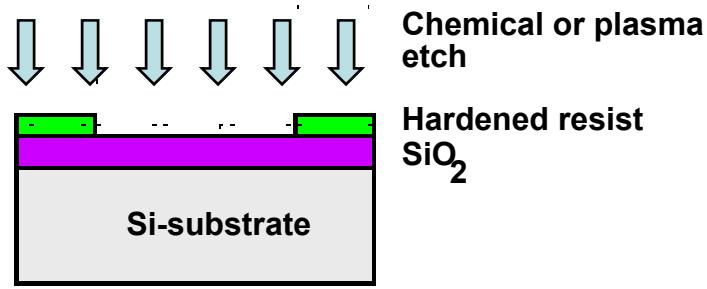
(b) After oxidation

(c) After oxidation and deposition of negative photoresist

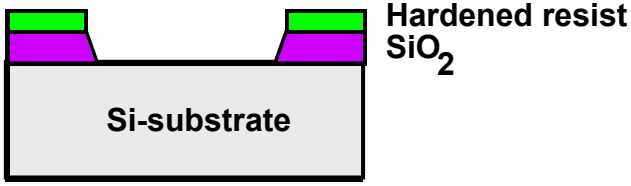
Lithography Process



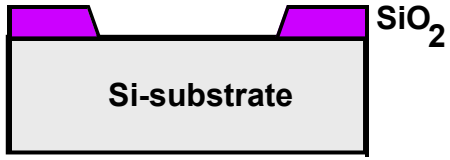
(d) Stepper exposure



(e) After development and etching of resist, chemical or plasma etch of SiO_2



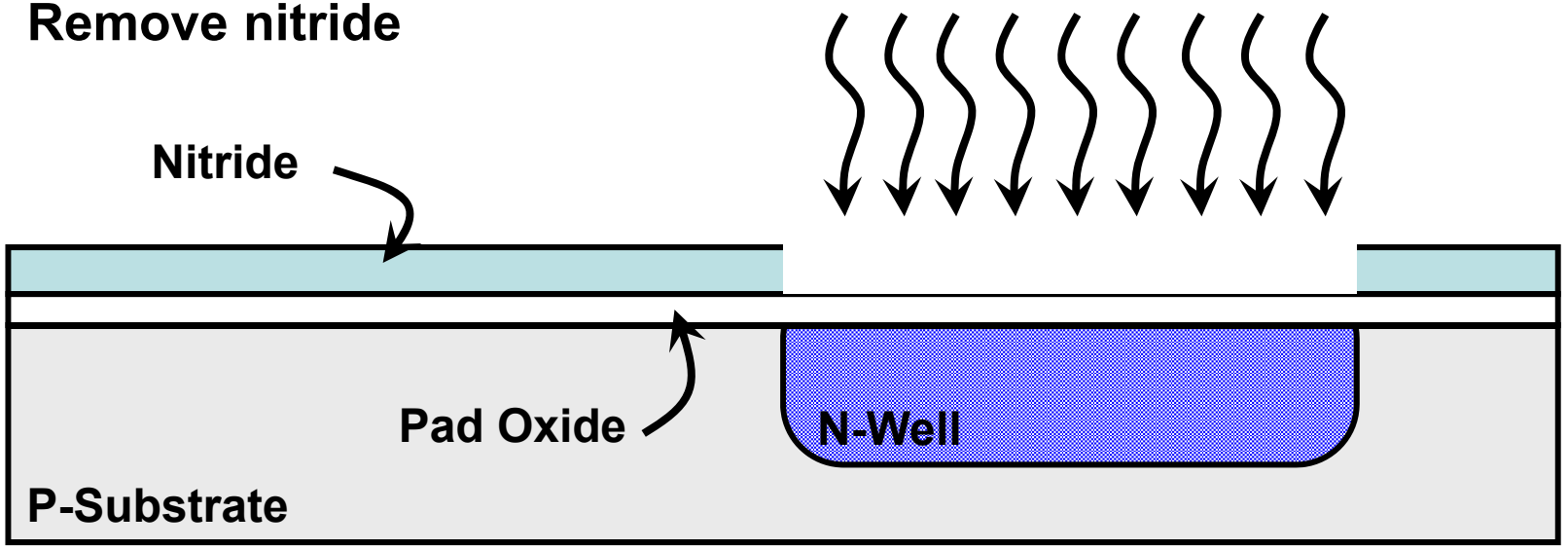
(f) After etching



(g) Final result after removal of resist

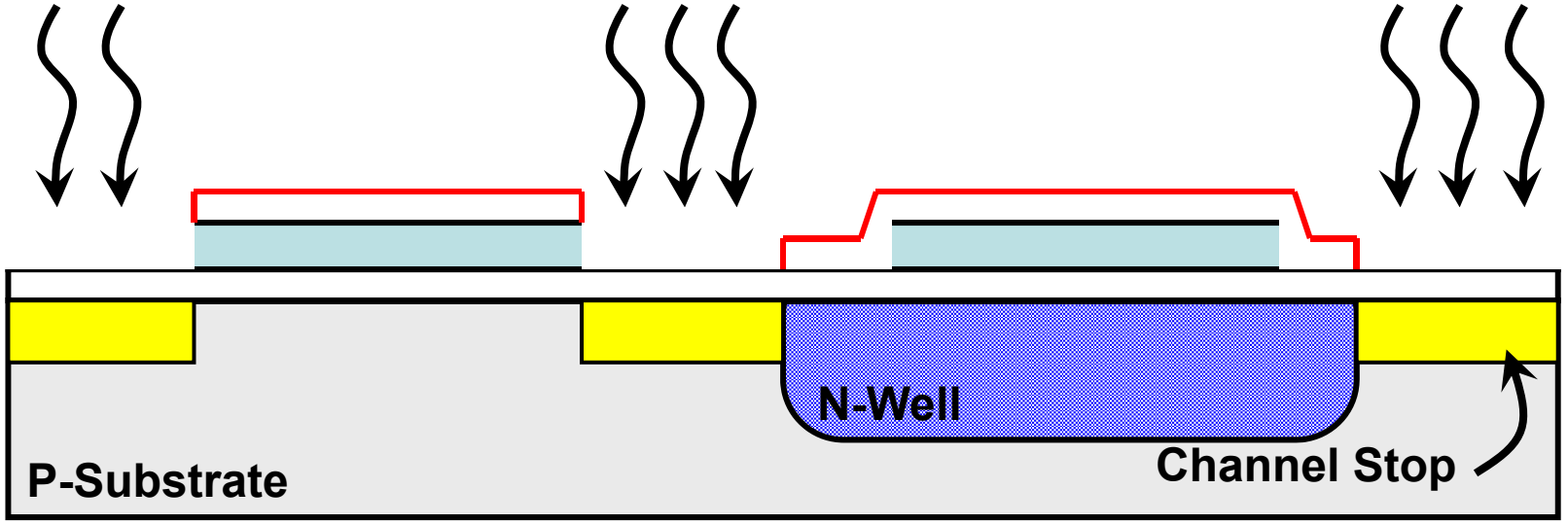
CMOS Process (N-Well)

1. Start with p-doped substrate
2. Deposit pad ox (stress relief) and Si_3N_4 (implant block)
3. Pattern nitride (Si_3N_4)
4. Implant N-type impurities (phosphorous) with high energy, low doping
5. Remove nitride



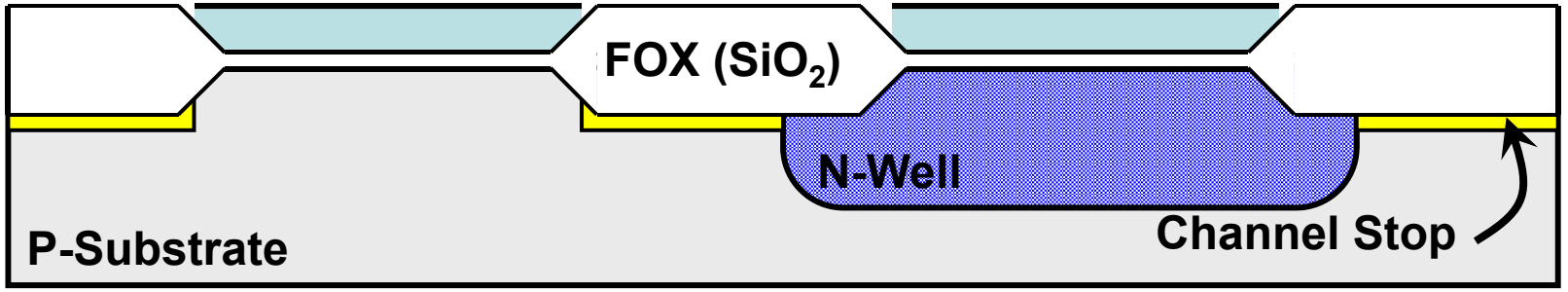
CMOS Process (Channel Stop)

6. Deposit new pax ox/nitride and pattern using active where "active = (n+ mask) + (p+ mask)"
7. Apply p-field resist and pattern using inverse N-well
8. Implant P-type impurities low energy (channel stop)



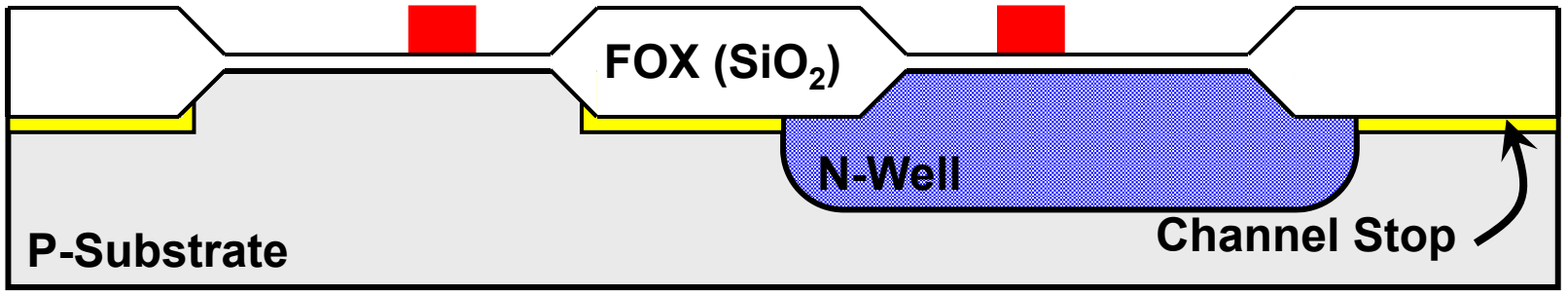
CMOS Process (FOX)

9. Grow field oxide (SiO2)
   - Nitride prevents oxidation => Local Oxidation of Silicon (LOCOS)
   - Oxidation consumes silicon => Silicon recessed
10. Remove nitride



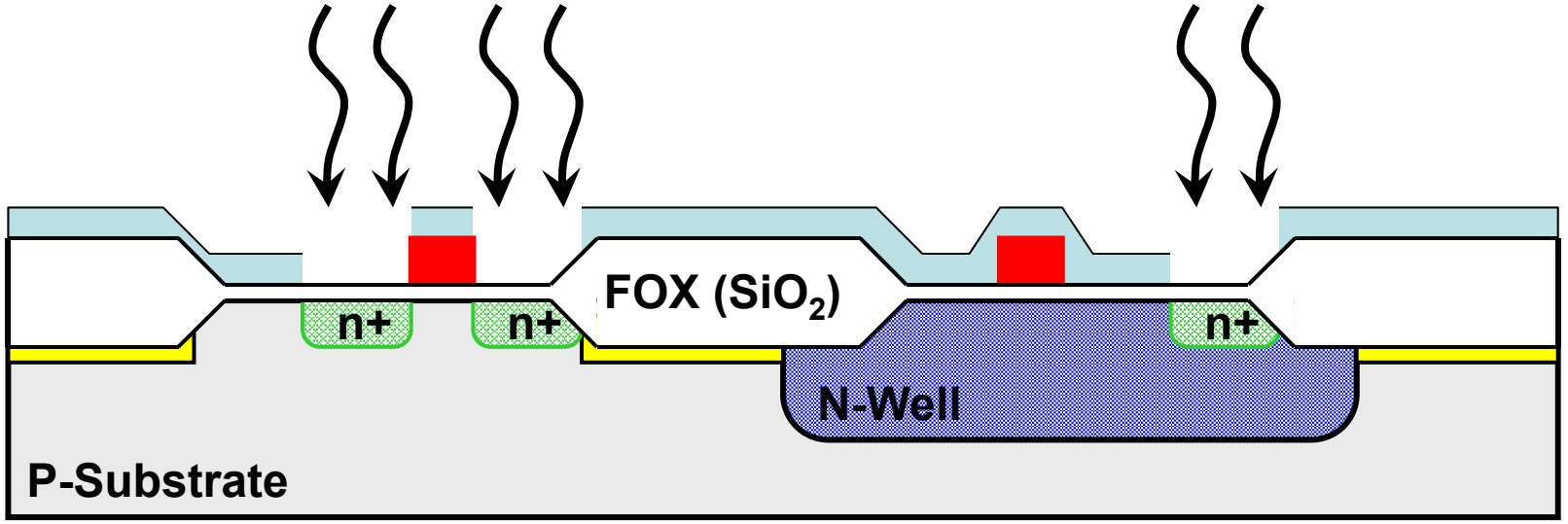
CMOS Process (Poly Gate)

11. Oxidize entire wafer (this forms gate oxide)
12. Deposit polysilicon (CVD)
13. Dope Poly Heavily
14. Pattern polysilicon (Plasma Etch)



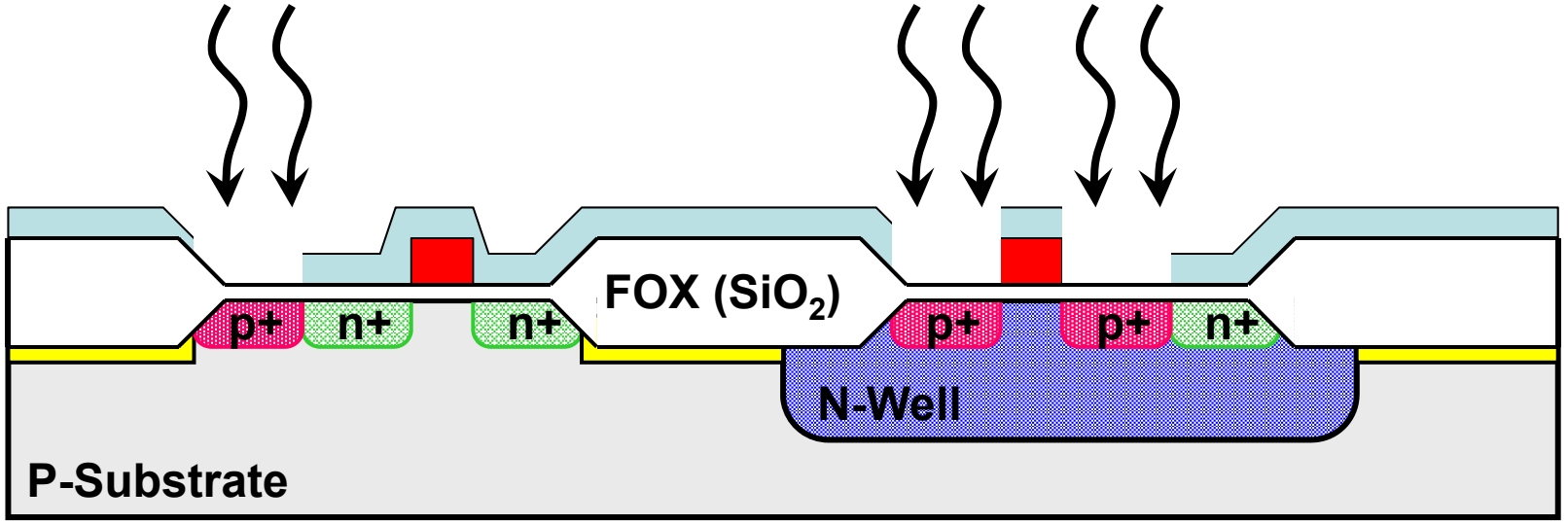
CMOS Process (n+ implants)

15. Deposit and pattern another nitride layer to expose n+ Source/Drain implant
16. Implant p+ source/drain dopants (high dose, med energy)
17. Remove nitride



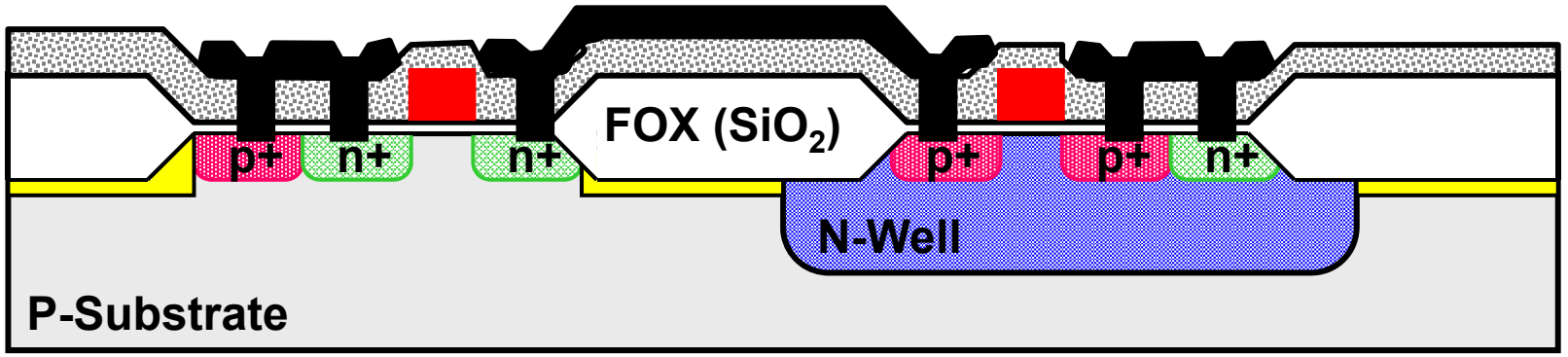
CMOS Process (p+ implants)

18. Deposit and pattern another nitride layer to expose p+ Source/Drain implant
19. Implant n+ source/drain dopants (high dose, med energy)
20. Remove nitride



CMOS Process (Contacts & M1)

21. Deposit ILD (SiO_2)
22. Pattern and etch contact holes
23. Sputter on M1
24. Pattern and etch M1



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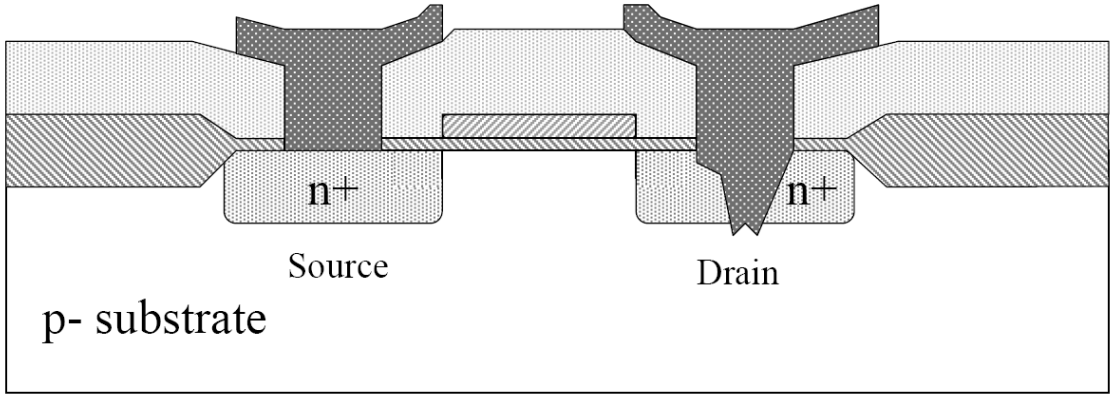
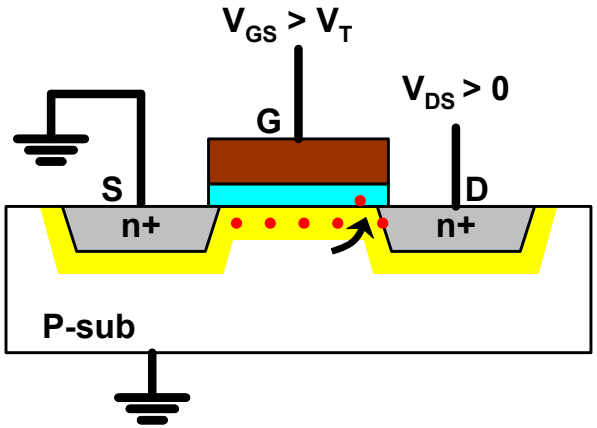
Contact Spiking

- **Contact spiking is a source of process failure**
  - **Aluminum can diffuse into silicon**
  - **If it diffuses a distance greater than the junction depth then a drain can get shorted to the substrate**
  - **A thin layer of Titanium is usually deposited first as a "barrier metal"**

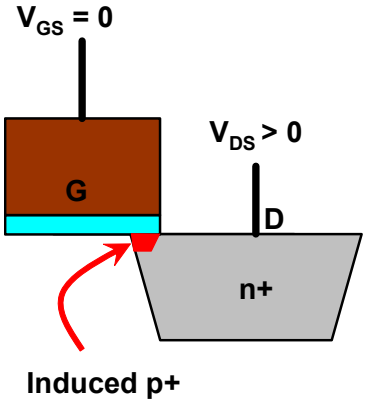


Short Channel Effects

- Device scaling and high electric field cause new issues such as "hot electron" and "Gate Induced Drain Leakage (GIDL)" (refer to lecture 4)
- Those issues can be relieved if drain doping can be reduced
- But drain doping cannot be reduced too much, because it increases the parasitic resistance (refer to lecture 4)



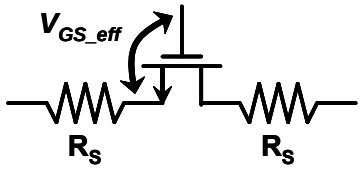
Hot electron

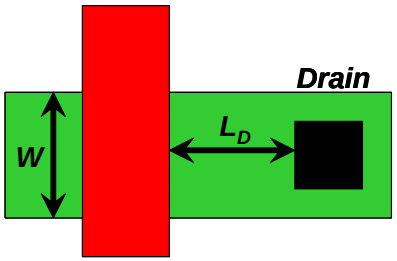


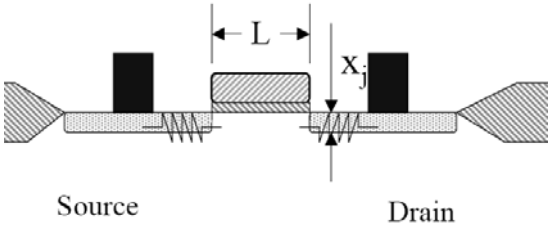
GIDL

Source/Drain/Gate Parasitic Resistance

- As L is scaled down it is desirable to scale x_j down as well
- However, currents are not necessarily scaling down at the same rate, so the drain resistance is becoming more significant
  - Implanted junctions will have a resistance of around 30-100Ω/square
- A similar problem exists for poly gate
  - Doped poly resistance can still have a resistance of about 30Ω/square
- How can we solve these problems?

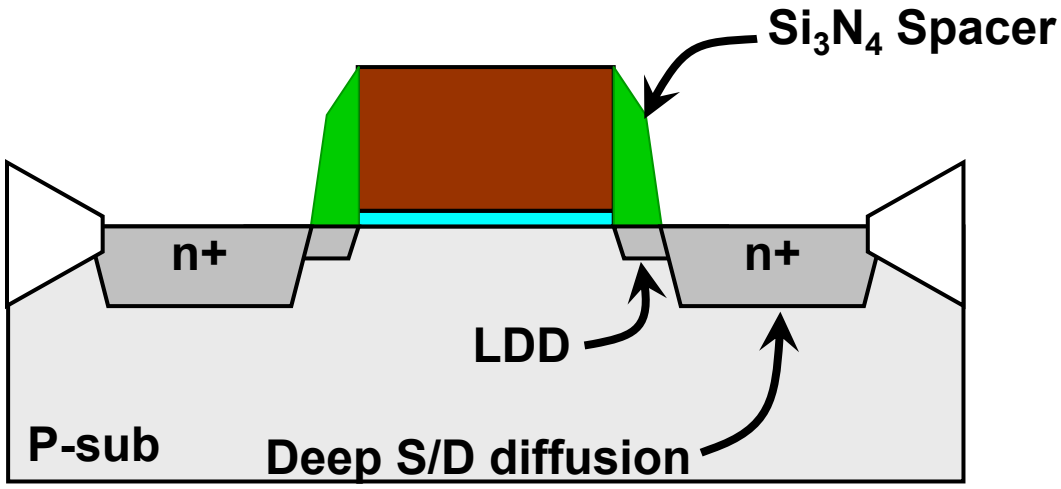






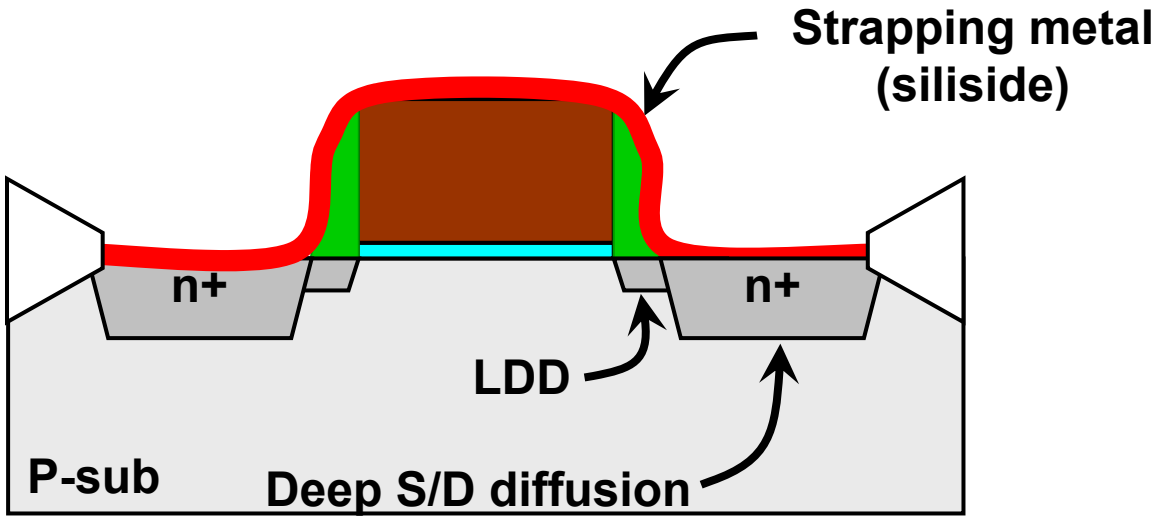
Lightly Doped Drain (LDD)

- **Use of two drain diffusions:**
  - One forming a lightly doped drift region near the edge of the gate.
  - The other forming a more heavily doped region beneath the contact, this will reduce the drain resistance of the structure and allows the transistor to retain most of the performance of a conventional single doped drain device.



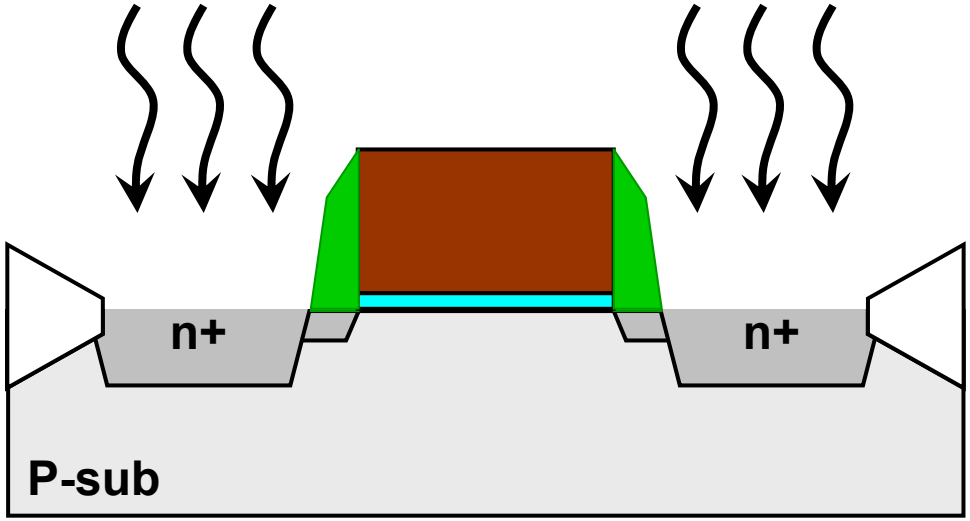
Salicidation

- To reduce the parasitic resistance further more, a layer of conducting metal could be laid down and patterned over the source, drain, and gate area, thus "strapping" it with a parallel low resistance path.
- What problem does it create?



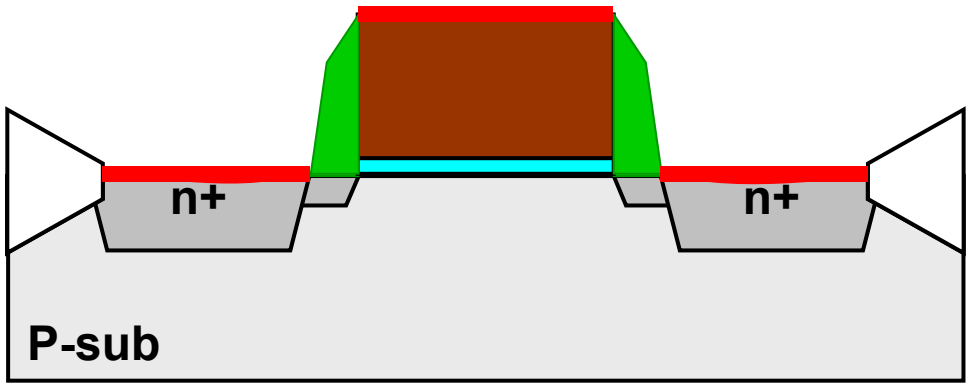
Self-Aligned Silicide

- Implant shallow Source/Drains (these will form “tips” of the S/D)
- Deposit Si_3N_4. Nitride will naturally form thicker (like a snow drift) around the poly gate
- Uniformly etch the nitride
- Now implant source drains again with more energy. The nitride spacers will block the implant and “tips” are real (shallow) S/D’s



Self-Aligned Silicide

- With the spacers in place, we deposit a thin layer of conducting material to “strap” the source/drains and gate. Titanium is typically used.
- As heat is applied the Titanium reacts with Silicon and forms Titanium-Silicide.
- Now a selective etch that will etch titanium and not titanium-silicide is applied. This leaves the desired “strapped” source/drain and gate with no shorts



Shallow Trench Isolation (STI)

- Problem with Local Oxidation of Silicon (LOCOS) : "Bird's beak" intrudes into the active area
- Sharp point of the "beak" causes high fields, crystal Lattice damage, and can be a magnet for defects & leakage
- Can not grow the SiO_2 on a small scale, hence isolation distances were limiting the effectiveness of scaling. A new type of isolation was needed.
- Shallow Trench Isolation (STI) is the solution. Silicon is etched using plasma etch, then SiO_2 is deposited into the trench.