ECE520 – VLSI Design

Lecture 9: Design Rules

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

Review of Last Lecture

- ☐ **Interconnect Manufacturing Process**
  - **Back-end Process (Conventional)**
  - **Back-end Process (Modern – Dual Damascene)**
- ☐ **Interconnect Modeling**
  - **Parasitic Capacitance**
  - **Parasitic Resistance**
  - **Parasitic Inductance**
  - **Delay Estimation Techniques**

Today's Lecture

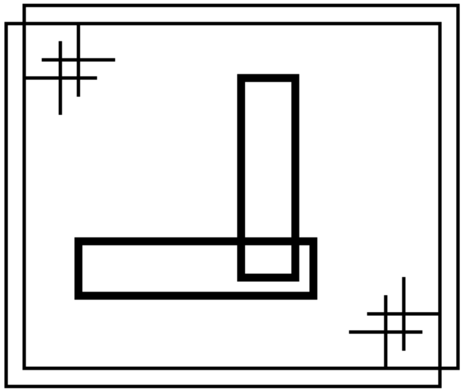
- **Review of output resistance of an inverter**
- **Overview of Design Rules**
  - **What are design rules?**
  - **Why have design rules?**
  - **Typical design rules**

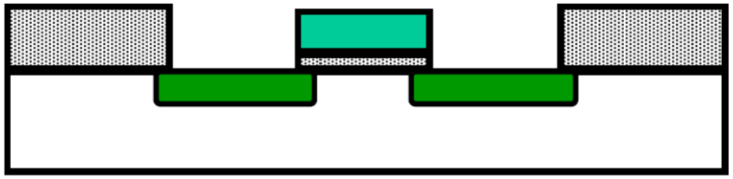
What Are Design Rules?

- ❑ **Interface between the circuit designer and process engineer**
- ❑ **Guidelines for constructing process masks**
- ❑ **Unit dimension: minimum feature size (transistor gate length)**
  - **scalable design rules: lambda parameter**
  - **absolute dimensions: micron rules**
- ❑ **Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur**
- ❑ **A complete set includes**
  - **set of layers**
  - **intra-layer: relations between objects in the same layer**
  - **inter-layer: relations between objects on different layers**

Why Have Design Rules?

- ☐ **To be able to tolerate some level of fabrication errors such as**
  - **Mask misalignment**
  - **Dust**
  - **Process parameters (e.g., lateral diffusion)**
  - **Rough surfaces**





Typical CMOS Process Layers

Layers:

N-Well

Active Area

Select (n+,p+)

Polysilicon

Metal1

Metal2

Contact To Poly

Contact To Diffusion

Via

❑ **Points:**

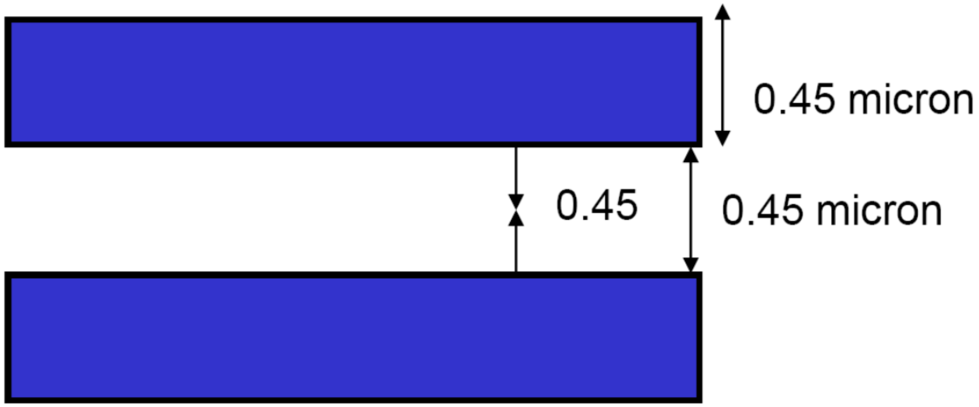
- N-well process p-type wafer (no p-well)
- Active area determines where transistors may go
- Poly overlapping with active = transistor
- Select is where n+ and p+ ion implantation occurs; it can be used to place an opposite type region (e.g., put p+ select within n-well to create a p+ well plug, more later)
- All contacts/vias are the same size (eases processing)
- Advanced technology is more complex and has more layers (e.g. Thick Oxide, Thin Oxide, VT_high, VT_low, LI, etc.)

CMOS Process Layers in Layout Tools

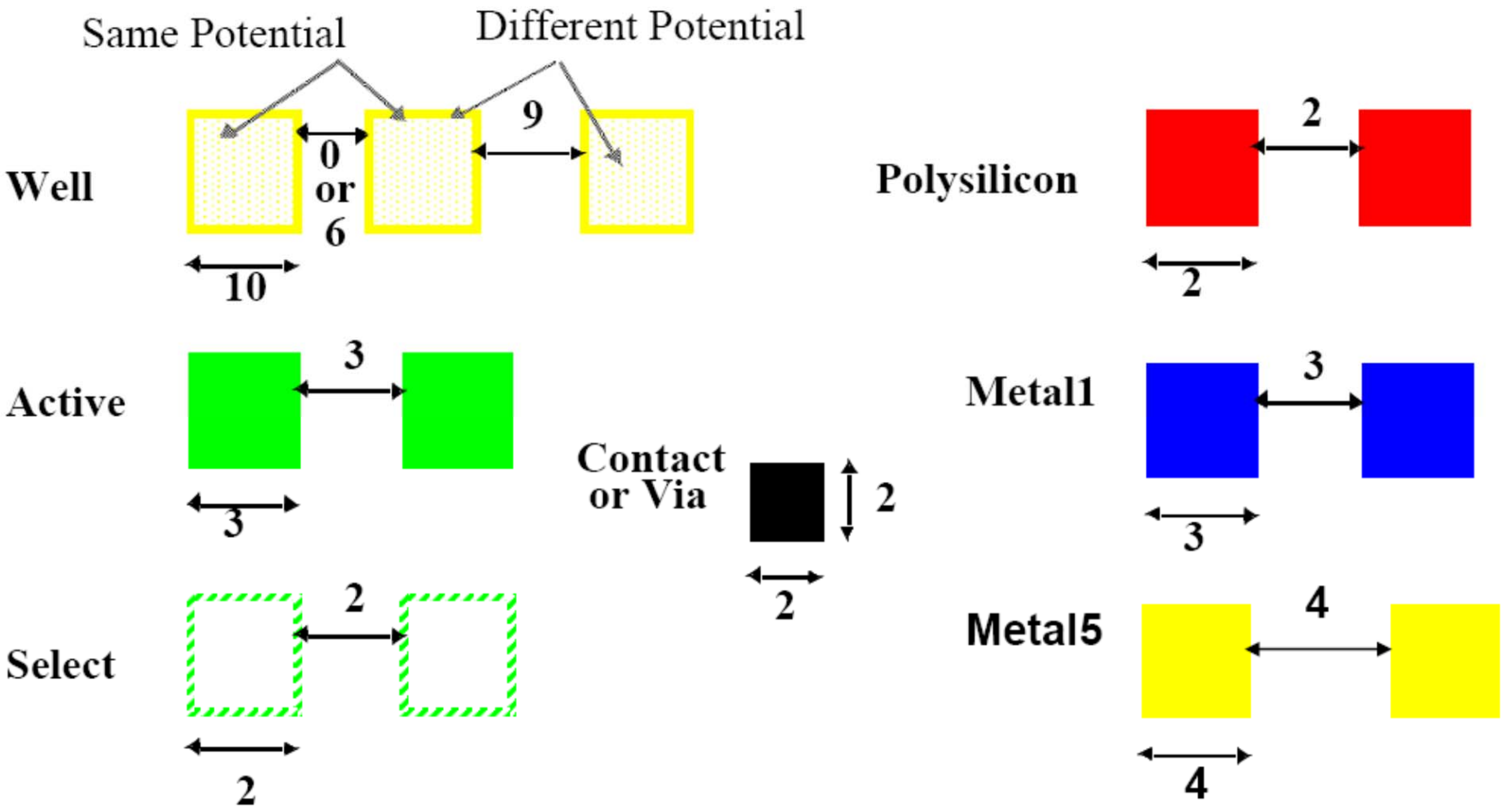
Layer	**Color**	**Representation**
Well (p,n)	Yellow	🟨
Active Area (n+,p+)	Green	🟩
Select (p+,n+)	Green	⬚
Polysilicon	Red	🟥
Metal1	Blue	🟦
Metal2	Magenta	🟪
Contact To Poly	Black	⬛
Contact To Diffusion	Black	⬛
Via	Black	⬛

Intra-Layer Design Rule Origins

- ☐ **Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab**
  - **minimum line width is set by the resolution of the patterning process (photolithography)**
- ☐ **Minimum spaces between objects (that are not related) on the same layer to ensure they will not short after fab**

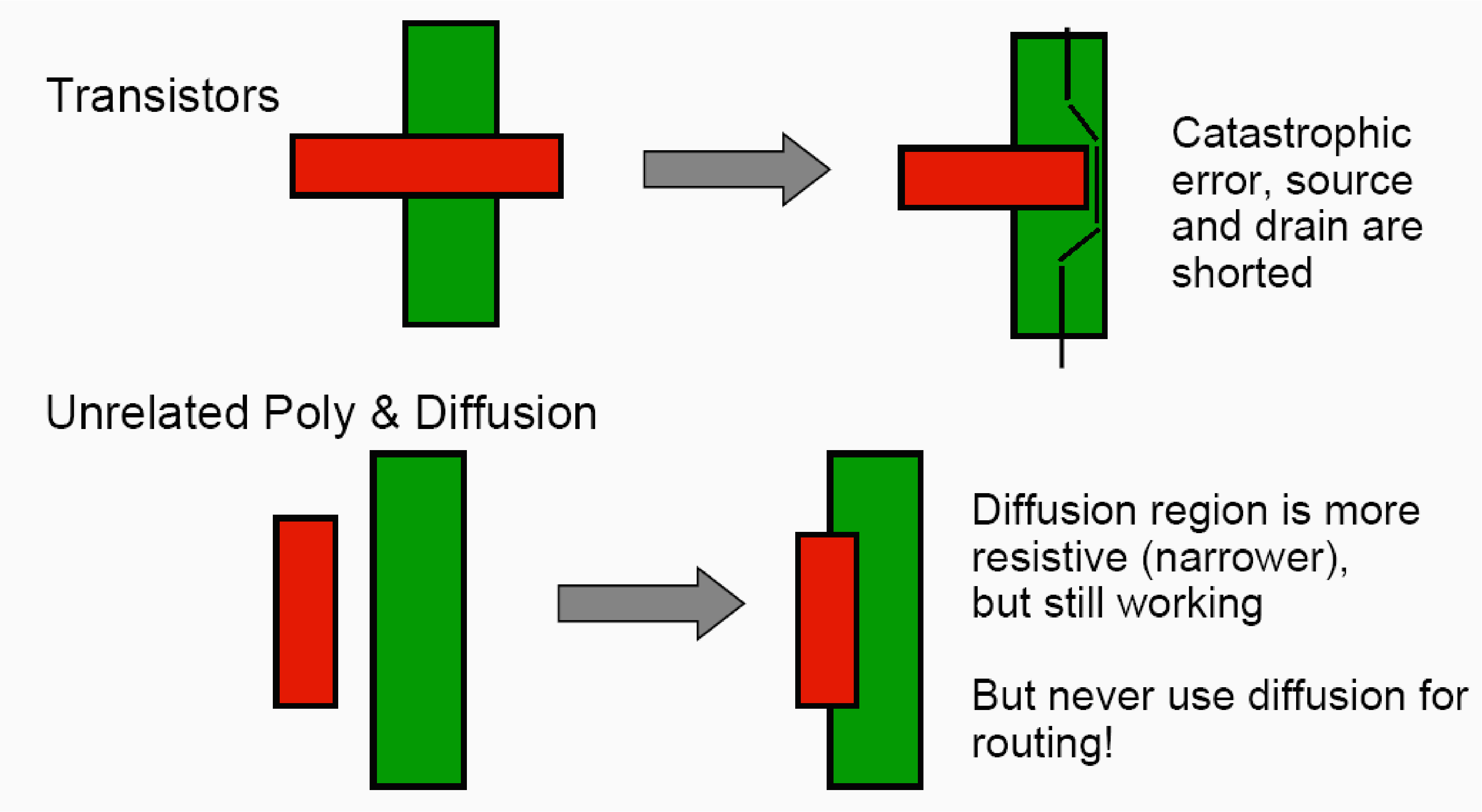


Intra-Layer Design Rules



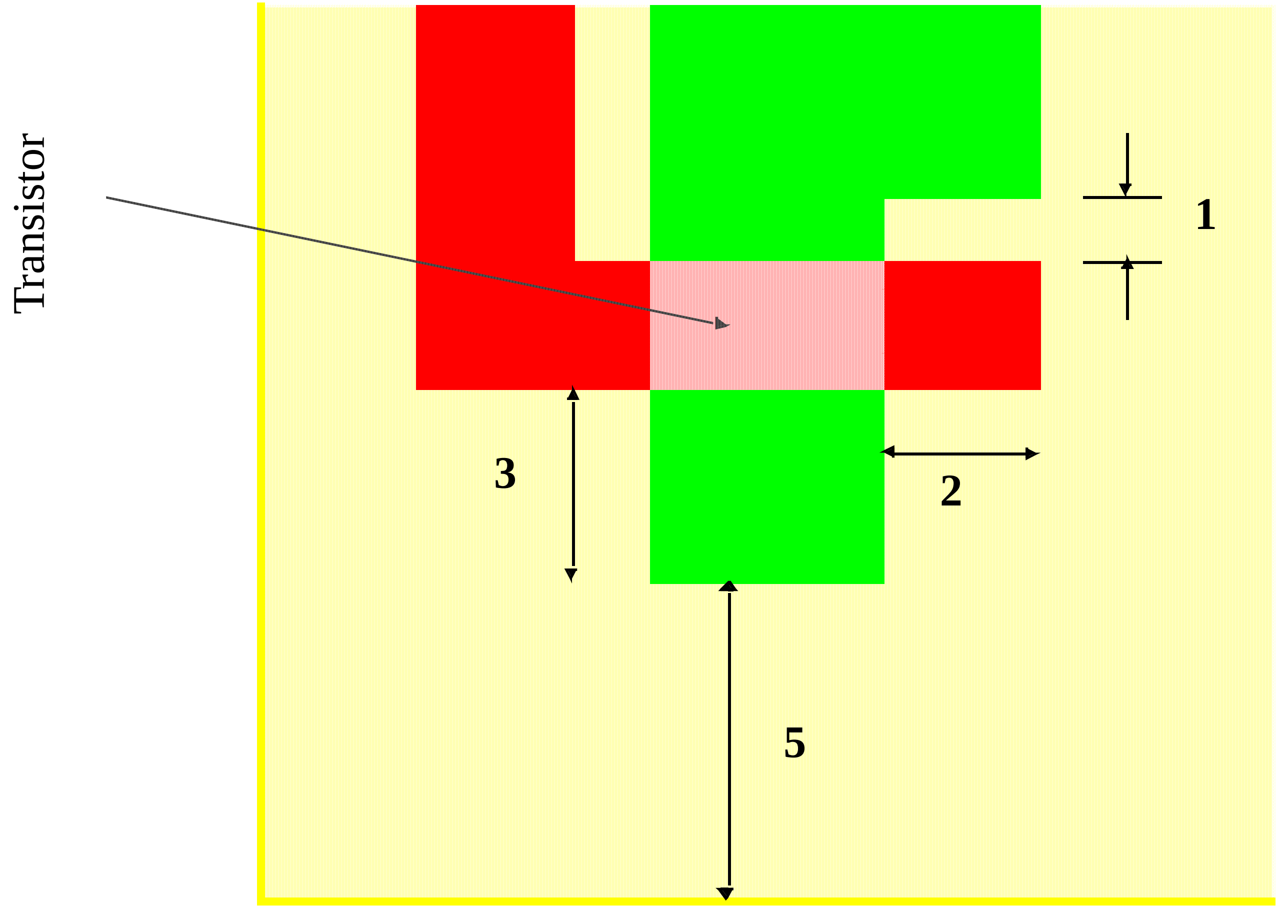
Inter-Layer Design Rule Origins

- **Transistor rules – transistor formed by overlap of diffusion (also called active) and poly layers**



Transistor Layout

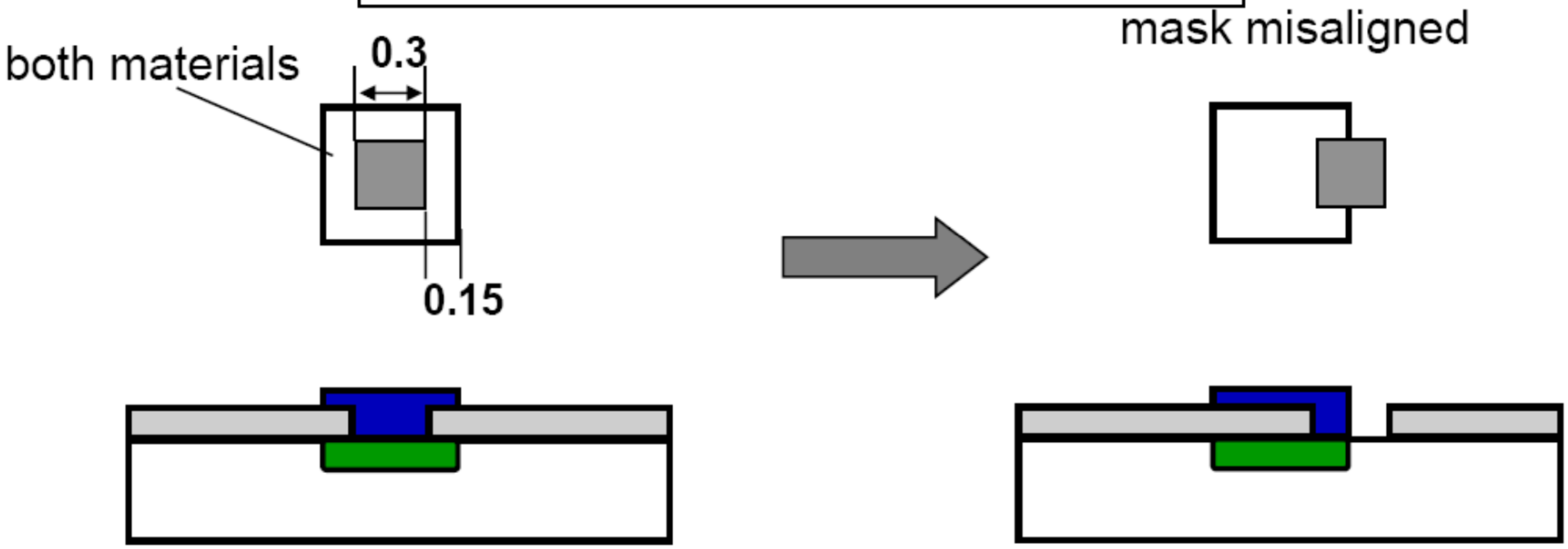
- **We will almost always use minimum L device**



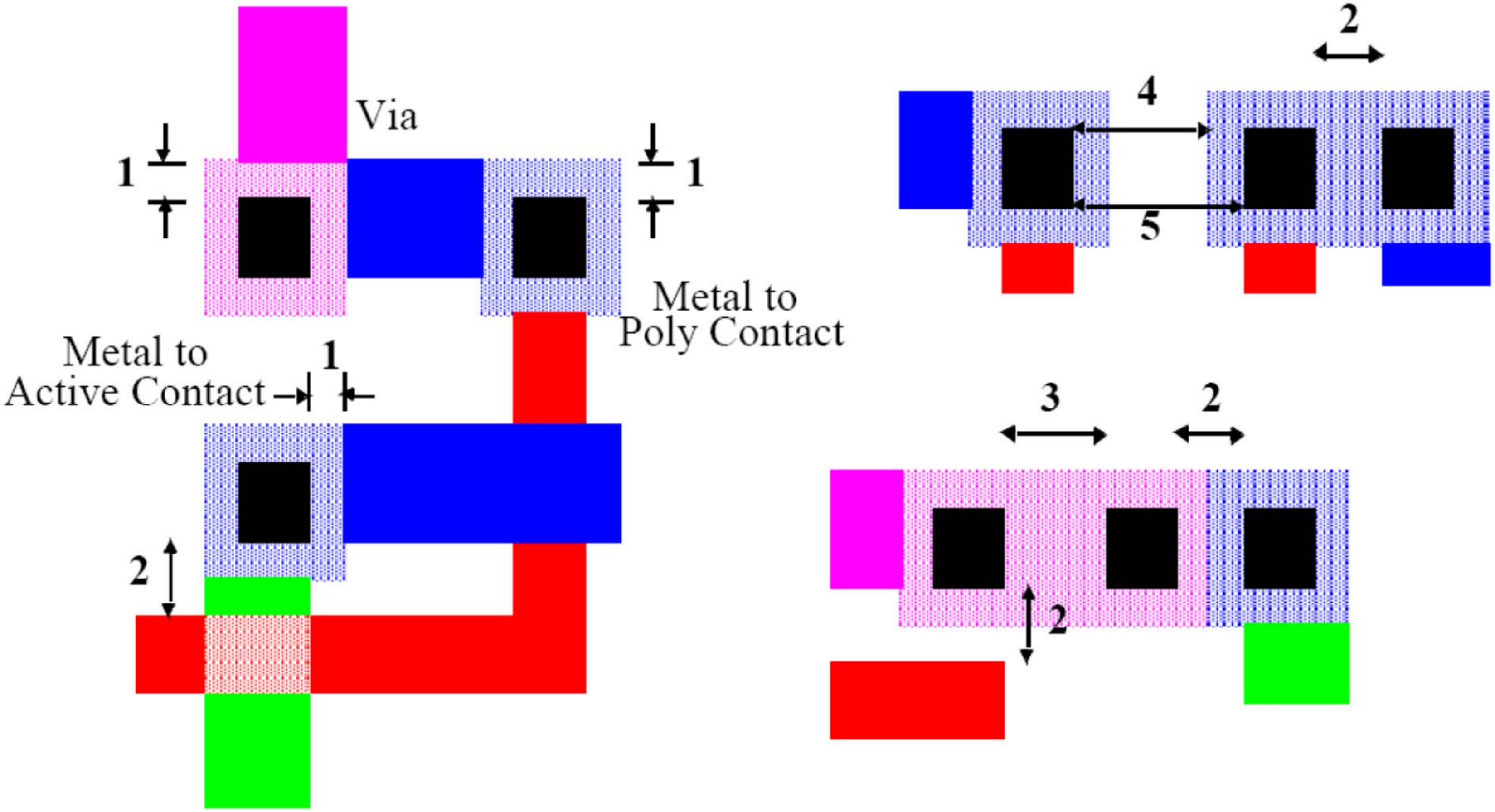
Inter-Layer Design Rule Origins

Contact
and via rules

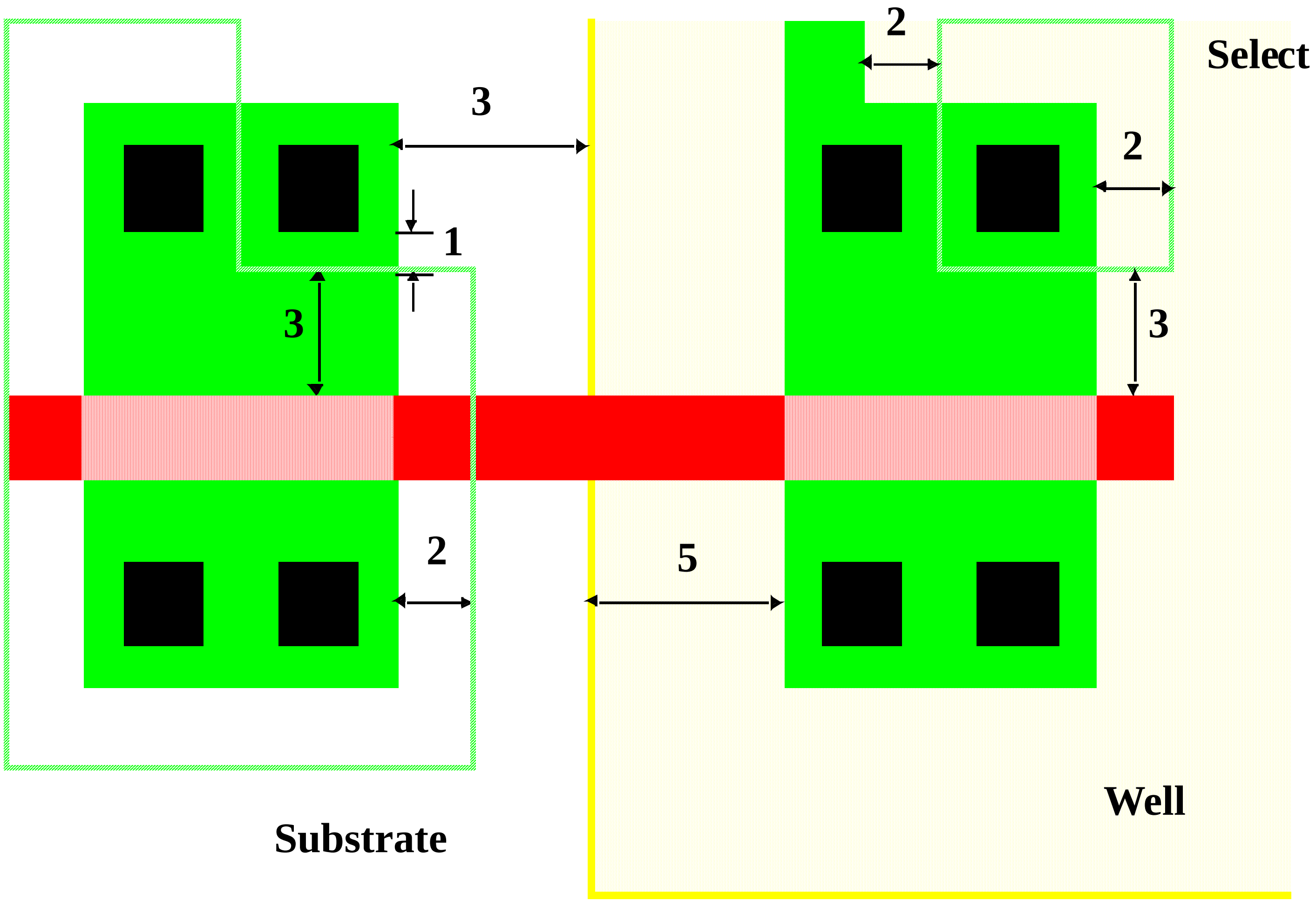
M1 contact to p-diffusion M1 contact to n-diffusion M1 contact to poly	Contact Mask
Mx contact to My	Via Masks



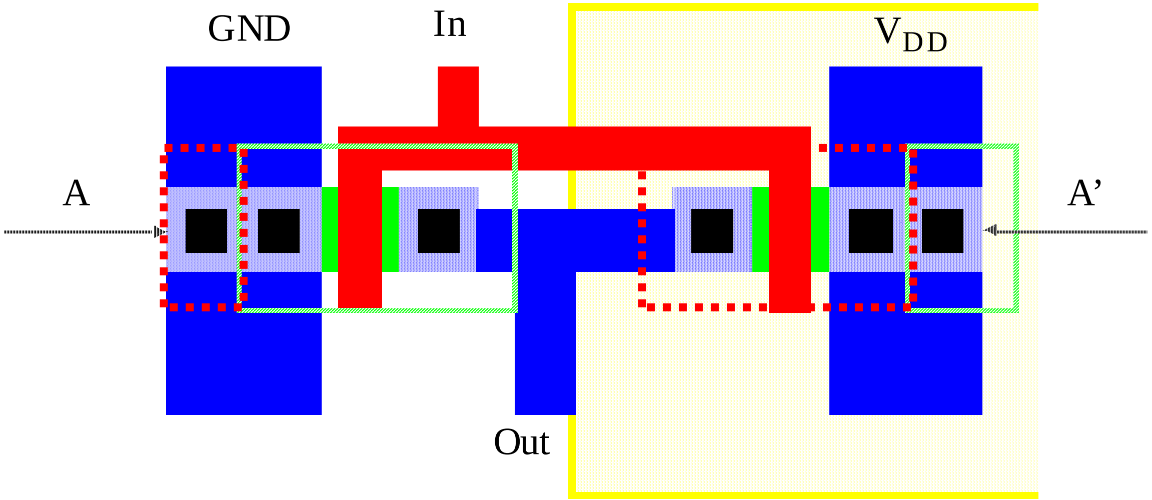
Vias and Contacts Design Rules



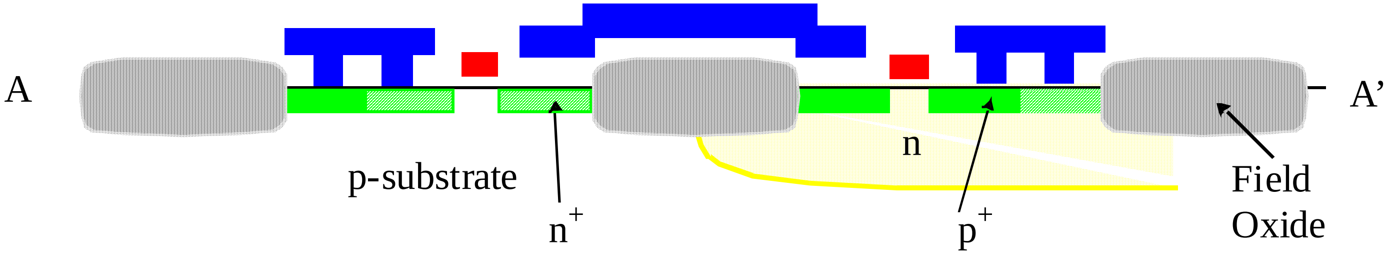
n+ or p+ Select Design Rules



Example: CMOS Inverter Layout

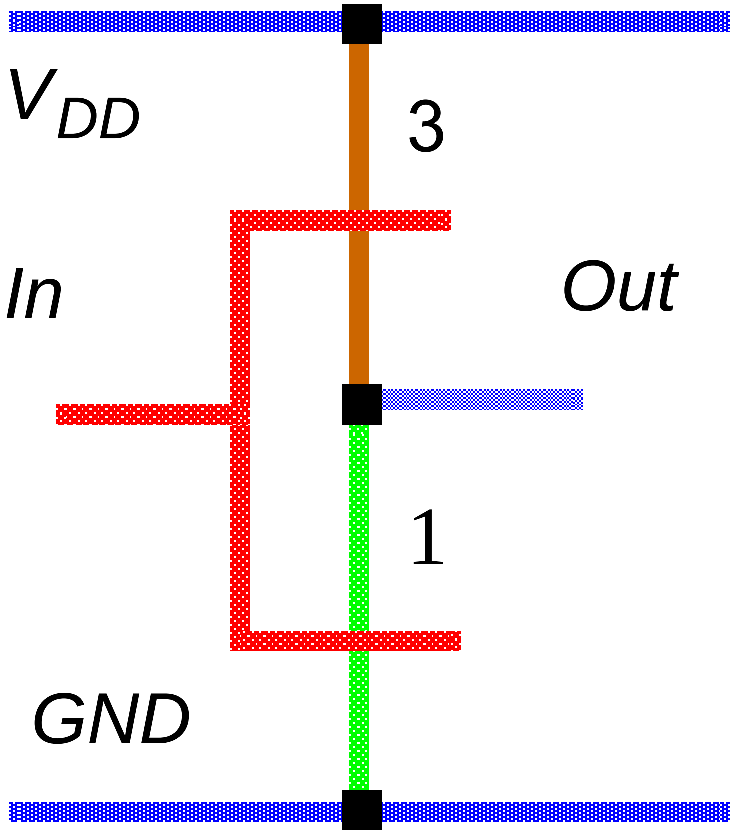


(a) Layout



(b) Cross-Section along A-A'

CMOS Inverter Layout Sticks Diagram



Stick diagram of inverter

- ❑ **Dimensionless layout entities**
- ❑ **Only topology is important**

Design Rules Note

- ☐ **The book’s process is NOT exactly the same as the one we will be using**
- ☐ **In general the numbers in previous slides are not the numbers you will use, they are simply representative of what Design Rules are like**