University of New Mexico

Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2007) Midterm Exam

Name: _____ Date: March 7, 2007

Note: Only one 8½ inch by 11 inch page equation sheet, ruler, calculator, pencils, and pens are allowed.

1. (10 points) The following figure is cross section view of an MOS device.

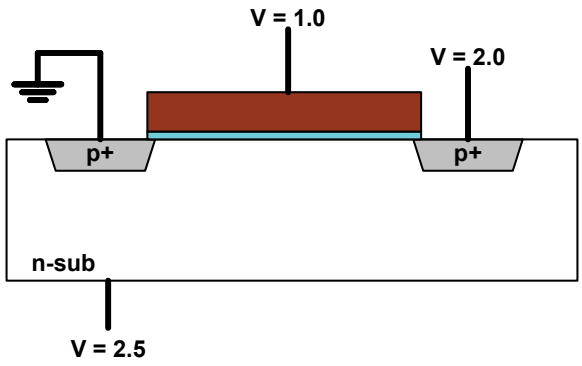
(a) What type is this device (NMOS or PMOS)?

(b) Considering the potential of each terminal in this figure, determine Source, Drain, Gate, and Substrate terminals and label them on the diagram.

(c) Assuming that $|V_T| = 0.5$ v and $|V_{DSAT}| = 1.5$ v. Find the region of operation of the device. Ignore body effect.

(d) Determine drain current if $|K'| = 100\ \mu A/v^2$, $(W/L) = 10$, and $|\lambda| = 0.1\ v^{-1}$.

(f) Draw ***depletion region*** and the ***channel*** on the diagram. What is the potential ***across the channel*** in this device?

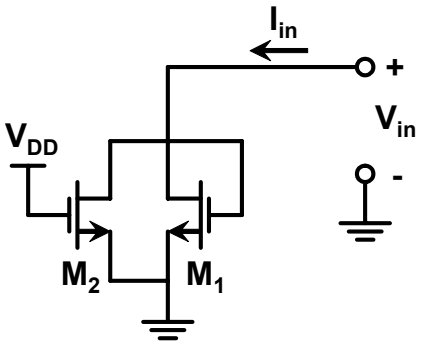


2. (15 points) The following circuit is a ***linear*** resistor implemented by NMOS only. Assume that M1 and M2 are identical.

(a) Find I_{in} as a function of V_{in} assuming $V_T < V_{in} < V_{DD}-V_T$ (assume long channel device and ignore channel length modulation).

(b) What is the dynamic resistance of this active resistor ($R_d = \partial V_{in} / \partial I_{in}$)?

(c) What is the expression for total parasitic capacitance of this active resistor as a function of C_{OX}, C_J, C_{JSW}, A_D, P_D, C_{GSOV}, C_{GDOV} of M_1 and M_2?



3. (15 points) For a MOSFET operating in the subthreshold regime ($V_{GS} < V_T$), the reduction in gate voltage needed to reduce the drain current by one decade is defined as the "subthreshold swing" where

$$S = \frac{kT}{q} Ln(10)\left(1 + \frac{C_{Dep}}{C_{OX}}\right)$$

The unit of S is mV/decade.

(a) Find S at room temperature for an NMOS with $t_{OX} = 2\ nm$, $W_{Dep} = 40\ nm$ ($\varepsilon_{sio2} = 3.9$ and $\varepsilon_{si} = 11.9$).

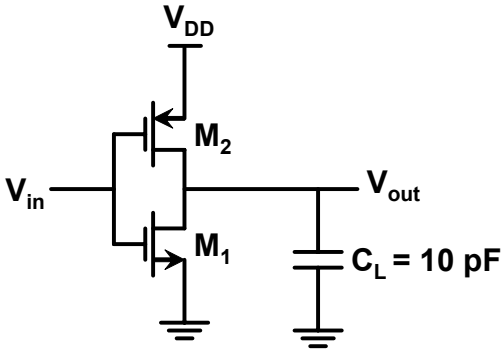
(b) The threshold voltage for this device is defined to V_{GS} at which the normalized drain current $I_{DS}/(W/L)$ reaches $100\ nA$, with $V_{DS} = V_{DD} = 2.5\ V$. We would like to set the leakage current to be $1nA$ when $V_{GS} = 0\ V$ and $V_{DS} = V_{DD} = 2.5\ V$ for a device with $(W/L)=5$. What is the minimum threshold voltage this device can have?

(c) This device is used in a circuit that can go to standby mode. To meet the power dissipation requirement in standby mode, a body bias is applied. Considering that the zero bias threshold voltage of the device is $0.1\ v$, find the body bias that is needed to be applied. Draw a circuit diagram of the NMOS and Indicate the polarity of body bias voltage on your diagram. Assume $\gamma = 0.4\ v^{1/2}$ and $2\varphi_f = 0.6\ v$.

4. (20 points) We would like to design an inverter to drive a long interconnect (clock line) with effective capacitance of ***10 pF***. By computing the average current used to charge/discharge C_L, determine W_P such that t_{PLH} **= 250 ps**. Notice that the load capacitance is substantially larger than the internal capacitance of the gate. To reduce the parasitics, use minimum length for all transistors (***L=0.25 um***). Supply voltage V_{DD} is ***2.5 v***.

Use the following data table for all transistors. Watch for *channel length modulation* and *velocity saturation*!

$K'_p = -60\ \mu A/v^2$
$V_{Tp0} = -0.4\ v$
$\lambda_p = -0.15\ v^{-1}$
$V_{DSATp} = -1\ v$



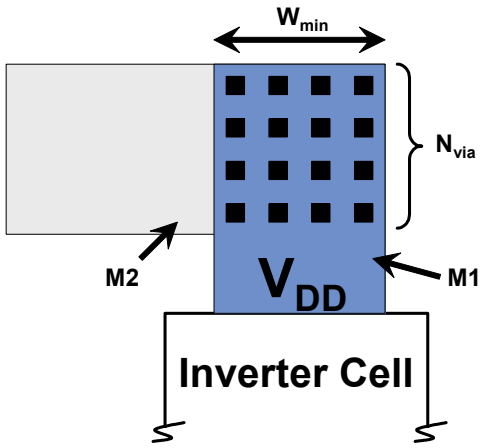
5. (10 points) We would like to design the layout of the clock driver designed in the previous problem.

(a) Determine the dynamic power dissipation of the inverter assuming the clock frequency of 1GHz. Ignore the device internal capacitances.

(b) Determine the average current of the clock driver.

(c) Determine the minimum width of power and ground strap, W_{min}, (shown below) to prevent electromigration. Assume that metal thickness is 0.4 μm and maximum current density $J_{max} = 2x10^6$ A/cm^2 for copper.

(d) Determine the minimum number of vias, N_{via}, (shown below) to prevent electromigration. Assume that via size is 0.25 μm x 0.25 μm.



6. (15 points) The circuit in Figure 5-A is used to balance delay from the inverter to block A and B. Since the input capacitance of block B is smaller than that of block A, we try to match the delay by routing a longer wire to block B. Figure 5-B is the equivalent circuit of Figure 5-A.

(a) Using π-model for wires (see Figure 5-C), determine all R and C values of the equivalent circuit shown in Figure 5-B. Note that C_0, R_2, and C_2 will be as a function of L_2. Assume interconnect resistance is 5 Ω/μm and interconnect capacitance is 0.2 fF/μm.

(b) Using the Elmore delay model, write equations for propagation delays from V_{in} to terminal points A and B.

(c) Find the length of wire, L_2, such that the propagation delays become equal.

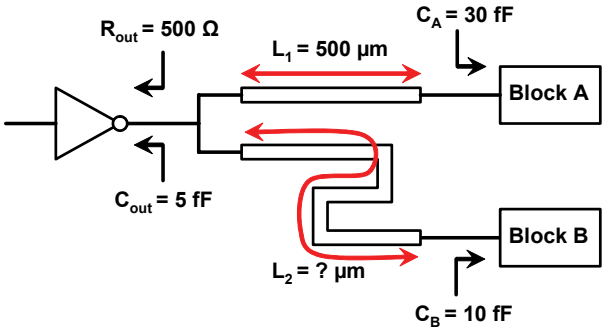


Figure 5-A

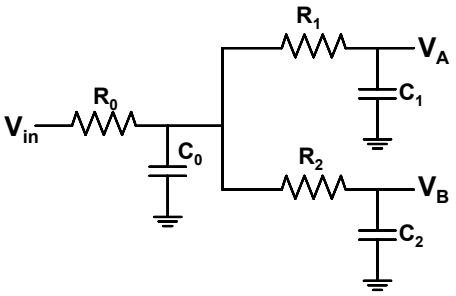


Figure 5-B

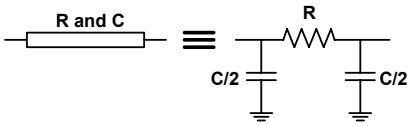


Figure 5-C

7. (3 points) What is the depletion mode transistor? What would be the characteristic of an NMOS depletion model device?

8. (3 points – *multiple choice*) Due to DIBLE effect, by increasing Drain voltage of an NMOS, the threshold voltage ….

A- increases.
B- decreases.
C- doesn't change.

Explain why?

9. (3 points – *multiple choice*) In order to increase the noise margin of a CMOS inverter, the size of ….

A- both NMOS and PMOS should decrease.
B- both NMOS and PMOS should increase.
C- transistors doesn't affect noise margin.
D- PMOS should increase and NMOS should decrease.
F- PMOS should decrease and NMOS should increase.

Explain why?

10. (3 points) Intel has recently announced that their fab is capable of implementing metal gate and high-k dielectric in their CMOS processes. Explain how metal gate and high-k dielectric improves VLSI technology.

11. (3 points) What is Salicidation in CMOS process? How does it improve the device performance?