University of New Mexico
Department of Electrical and Computer Engineering

ECE 523/421 – Analog Electronics (Fall 2013) Exam 2

Name: Answers

Date: Dec. 9, 2013

Note: Only two 8½ inch by 11 inch page equation sheet, calculator, pencils, and pens are allowed.

1. (10 points) Fill in the blank:

(a) If the CMRR of a CMOS opamp is 60dB and the differential gain is 10,000, then the common mode gain is ….10…..

(b) The 3-dB low frequency of an amplifier with three low frequency poles: 2Hz, 10Hz, and 15Hz, is approximately ……27….. Hz.

(c) The 3-dB high frequency of an amplifier with three poles: 2MHz, 250MHz, and 1GHz is approximately ……1.98…. MHz.

(d) The low frequency dominant pole in an amplifier is generally associated to the node with …lowest….. (lowest/highest) resistance.

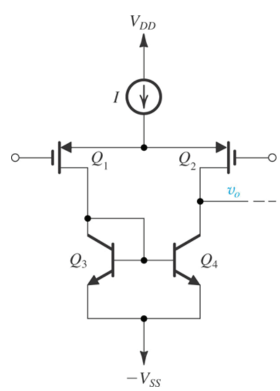
(e) The high frequency dominant pole in an amplifier is generally associated to the node with …highest.. (lowest/highest) resistance.

2. (15 points) For the BiCMOS differential amplifier below let V_{DD}=V_{SS}=3V, I=0.4mA, K'_pW/L=6.4mA/V^2, $|V_A|$ for PMOS is 10V, and $|V_A|$ for NPN transistors is 30V. Find G_m, R_o, and A_d.

$G_m = 1.6$ mA/V

$R_o = 37.5$ KΩ

$A_d = 60$



3. (30 points) The following differential amplifier utilizes a resistor to the negative power supply to establish the bias current I.

(a) For $V_{B1}=V_{id}/2$ and $V_{B2}=-V_{id}/2$, where V_{id} is a small signal with zero average, find the magnitude of the differential gain, $|V_o/V_{id}|$.

(b) For $V_{B1}=V_{B2}=V_{icm}$, where V_{icm} has a zero average, find the magnitude of the common-mode gain, $|V_o/V_{icm}|$.

(c) Calculate CMRR.

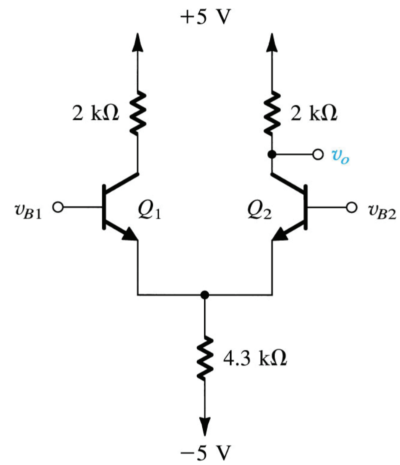
(d) If $V_{B1}=0.1\sin2\pi\times60t+0.005\sin2\pi\times1000t$ volts, and $V_{B2}=0.1\sin2\pi\times60t-0.005\sin2\pi\times1000t$ volts, find V_o.

$A_d = 20$

$A_{CM} = 2.3\times10^{-3}$

CMRR = 78.8 dB

$v_o = 2.3\times10^{-4}\sin2\pi60t + 0.1\sin2\pi1000t$



4. (30 points) The following circuit is a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies.

(a) Find the DC bias current in each of the three transistors. Also, find the DC voltage at the output. Assume β=100 and neglect Early effect.

(b) Find the input resistance and the output resistance.

(c) Select values for C_1, C_2, and C_3 to place each pole a decade apart from the other and to obtain a lower 3-dB frequency of 100Hz, while minimizing the total capacitance.

$I_{C_1} \approx I_{C_2} \approx I_{C_3} \approx 1$ mA

$v_o \approx 0$ V

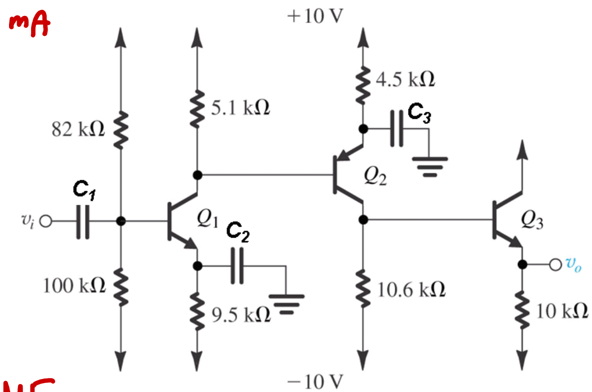
$R_{in} = 2.37$ kΩ

$R_{out} = 128.3$ Ω

$C_1 = 67.15$ μF

$C_2 = 35.46$ μF

$C_3 = 21.43$ μF

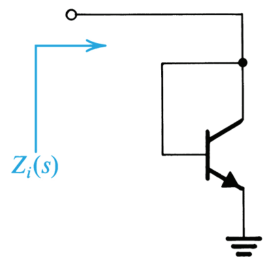


5. (15 points) Consider the diode configuration NPN below.

(a) Derive an expression for $Z_i(s)$ as a function of β, g_m, r_o, and C_π.

(b) Find the expression for the frequency of the pole in this circuit.

(c) Determine the high frequency bandwidth of this device when β=100, g_m=40mA/V, r_o=10KΩ, and C_π=1pF.



$$Z(s) = \frac{1}{sC_\pi} \| \frac{\beta}{g_m} \| \frac{1}{g_m} \| r_o$$

$$f_p \approx \frac{1}{2\pi C_\pi \left(\frac{\beta}{g_m} \| \frac{1}{g_m} \| r_o\right)}$$

$$f_p \approx 6.44 \text{ GHz}$$