Computer Simulations Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSPice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 5.1: Device Structure and Physical Operation

5.1 MOS technology is used to fabricate a capacitor, utilizing the gate metallization and the substrate as the capacitor electrodes. Find the area required per 1-pF capacitance for oxide thickness ranging from 2 nm to 10 nm. For a square plate capacitor of 10 pF, what dimensions are needed?

5.2 Calculate the total charge stored in the channel of an NMOS transistor having $C_{ox} = 9$ fF/μm^2, $L = 0.36$ μm, and $W = 3.6$ μm, and operated at $V_{OV} = 0.2$ V and $V_{DS} = 0$ V.

5.3 Use dimensional analysis to show that the units of the process transconductance parameter k_n' are A/V^2. What are the dimensions of the MOSFET transconductance parameter k_n?

5.4 An NMOS transistor that is operated with a small v_{DS} is found to exhibit a resistance r_{DS}. By what factor will r_{DS} change in each of the following situations?

(a) V_{OV} is doubled.
(b) The device is replaced with another fabricated in the same technology but with double the width.
(c) The device is replaced with another fabricated in the same technology but with both the width and length doubled.
(d) The device is replaced with another fabricated in a more advanced technology for which the oxide thickness is halved and similarly for W and L (assume μ_n remains unchanged).

D 5.5 An NMOS transistor fabricated in a technology for which $k_n' = 400$ μA/V^2 and $V_t = 0.5$ V is required to operate with a small v_{DS} as a variable resistor ranging in value from 250 Ω to 1 kΩ. Specify the range required for the control voltage V_{GS} and the required transistor width W. It is required to use the smallest possible device, as limited by the minimum channel length of this technology ($L_{min} = 0.18$ μm) and the maximum allowed voltage of 1.8 V.

5.6 Sketch a set of $i_D - v_{DS}$ characteristic curves for an NMOS transistor operating with a small v_{DS} (in the manner shown in Fig. 5.4). Let the MOSFET have $k_n = 5$ mA/V^2 and $V_{tn} = 0.5$ V. Sketch and clearly label the graphs for $V_{GS} = 0.5$, 1.0, 1.5, 2.0, and 2.5 V. Let V_{DS} be in the range 0 to 50 mV. Give the value of r_{DS} obtained for each of the five values of V_{GS}. Although only a sketch, your diagram should be drawn to scale as much as possible.

D 5.7 An n-channel MOS device in a technology for which oxide thickness is 4 nm, minimum channel length is 0.18 μm, $k_n' = 400$ μA/V^2, and $V_t = 0.5$ V operates in the triode region, with small v_{DS} and with the gate–source voltage in the range 0 V to +1.8 V. What device width is needed to ensure that the minimum available resistance is 1 kΩ?

5.8 Consider an NMOS transistor operating in the triode region with an overdrive voltage V_{OV}. Find an expression for the incremental resistance

$$r_{ds} \equiv 1 \Big/ \frac{\partial i_D}{\partial v_{DS}}\Big|_{v_{DS}=V_{DS}}$$

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

5.19 A particular n-channel MOSFET is measured to have a drain current of 0.4 mA at $V_{GS} = V_{DS} = 1$ V and of 0.1 mA at $V_{GS} = V_{DS} = 0.8$ V. What are the values of k_n and V_t for this device?

D 5.20 For a particular IC-fabrication process, the transconductance parameter $k_n' = 400\ \mu A/V^2$, and $V_t = 0.5$ V. In an application in which $v_{GS} = v_{DS} = V_{supply} = 1.8$ V, a drain current of 2 mA is required of a device of minimum length of 0.18 μm. What value of channel width must the design use?

5.21 An NMOS transistor, operating in the linear-resistance region with $v_{DS} = 50$ mV, is found to conduct 25 μA for $v_{GS} = 1$ V and 50 μA for $v_{GS} = 1.5$ V. What is the apparent value of threshold voltage V_t? If $k_n' = 50\ \mu A/V^2$, what is the device W/L ratio? What current would you expect to flow with $v_{GS} = 2$ V and $v_{DS} = 0.1$ V? If the device is operated at $v_{GS} = 2$ V, at what value of v_{DS} will the drain end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?

5.22 For an NMOS transistor, for which $V_t = 0.4$ V, operating with v_{GS} in the range of 1.0 V to 1.8 V, what is the largest value of v_{DS} for which the channel remains continuous?

5.23 An NMOS transistor, fabricated with $W = 20\ \mu m$ and $L = 1\ \mu m$ in a technology for which $k_n' = 100\ \mu A/V^2$ and $V_t = 0.8$ V, is to be operated at very low values of v_{DS} as a linear resistor. For v_{GS} varying from 1.0 V to 4.8 V, what range of resistor values can be obtained? What is the available range if

(a) the device width is halved?
(b) the device length is halved?
(c) both the width and length are halved?

5.24 When the drain and gate of a MOSFET are connected together, a two-terminal device known as a "diode-connected transistor" results. Figure P5.24 shows such devices obtained from MOS transistors of both polarities. Show that

(a) the i–v relationship is given by

$$i = \frac{1}{2}k'\frac{W}{L}(v - |V_t|)^2$$

(b) the incremental resistance r for a device biased to operate at $v = |V_t| + V_{ov}$ is given by

$$r \equiv 1\Big/\left[\frac{\partial i}{\partial v}\right] = 1\Big/\left(k'\frac{W}{L}V_{ov}\right)$$

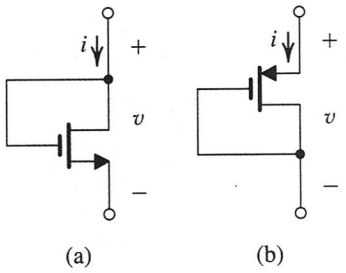

Figure P5.24

5.25 For the circuit in Fig. P5.25, sketch i_D versus v_S for v_S varying from 0 to V_{DD}. Clearly label your sketch.

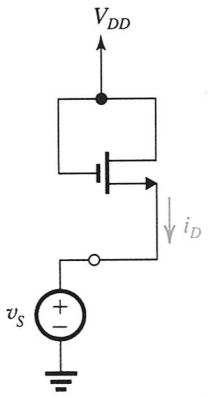

Figure P5.25

5.26 For the circuit in Fig. P5.26, find an expression for v_{DS} in terms of i_D. Sketch and clearly label a graph for v_{DS} versus i_D.

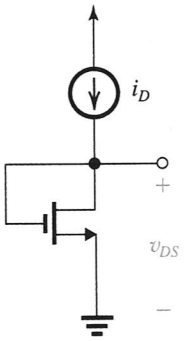

Figure P5.26

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5.30 For a particular MOSFET operating in the saturation region at a constant v_{GS}, i_D is found to be 0.5 mA for $v_{DS} = 1$ V and 0.52 mA for $v_{DS} = 2$ V. What values of r_o, V_A, and λ correspond?

5.31 A particular MOSFET has $V_A = 20$ V. For operation at 0.1 mA and 1 mA, what are the expected output resistances? In each case, for a change in v_{DS} of 1 V, what percentage change in drain current would you expect?

D 5.32 In a particular IC design in which the standard channel length is 1 μm, an NMOS device with W/L of 10 operating at 200 μA is found to have an output resistance of 100 kΩ, about $\frac{1}{5}$ of that needed. What dimensional change can be made to solve the problem? What is the new device length? The new device width? The new W/L ratio? What is V_A for the standard device in this IC? The new device?

D 5.33 For a particular n-channel MOS technology, in which the minimum channel length is 0.5 μm, the associated value of λ is 0.03 V^{-1}. If a particular device for which L is 1.5 μm operates in saturation at $v_{DS} = 1$ V with a drain current of 100 μA, what does the drain current become if v_{DS} is raised to 5 V? What percentage change does this represent? What can be done to reduce the percentage by a factor of 2?

5.34 An NMOS transistor is fabricated in a 0.5-μm process having $k_n' = 200$ μA/V^2 and $V_A' = 20$ V/μm of channel length. If $L = 1.5$ μm and $W = 15$ μm, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage of 0.5 V and $V_{DS} = 2$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 1 V, what is the corresponding change in I_D?

5.35 If in an NMOS transistor, both W and L are quadrupled and V_{OV} is halved, by what factor does r_o change?

D 5.36 Consider the circuit in Fig. P5.29 with both transistors perfectly matched but with the dc voltage at the drain of Q_1 lowered to +2 V. If the two drain currents are to be matched within 1% (i.e., the maximum difference allowed between the two currents is 1%), what is the minimum required value of V_A'? If the technology is specified to have $V_A' = 100$ V/μm, what is the minimum channel length the designer must use?

5.37 Complete the missing entries in the following table, which describes characteristics of suitably biased NMOS transistors:

MOS	1	2	3	4
λ (V^{-1})		0.02		
V_A (V)	20			100
I_D (mA)	0.5		0.1	
r_o (kΩ)		25	100	500

5.38 A PMOS transistor has $k_p'(W/L) = 100$ μA/V^2, $V_t = -1.0$ V, and $\lambda = -0.02$ V^{-1}. The gate is connected to ground and the source to +5 V. Find the drain current for $v_D = +4$ V, +2 V, +1 V, 0 V, and –5 V.

5.39 A p-channel transistor for which $|V_t| = 0.8$ V and $|V_A| = 40$ V operates in saturation with $|v_{GS}| = 3$ V, $|v_{DS}| = 4$ V, and $i_D = 3$ mA. Find corresponding signed values for v_{GS}, v_{SG}, v_{DS}, v_{SD}, V_t, V_A, λ, and $k_p'(W/L)$.

5.40 The table below lists the terminal voltages of a PMOS transistor in six cases, labeled a, b, c, d, e, and f. The transistor has $V_{tp} = -1$ V. Complete the table entries.

	V_S	V_G	V_D	V_{SG}	$\lvert V_{OV}\rvert$	V_{SD}	Region of operation
a	+2	+2	0				
b	+2	+1	0				
c	+2	0	0				
d	+2	0	+1				
e	+2	0	+1.5				
f	+2	0	+2				

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Section 5.3: MOSFET Circuits at DC

Note: If λ is not specified, assume it is zero.

D 5.44 Design the circuit of Fig. P5.44 to establish a drain current of 0.1 mA and a drain voltage of +0.3 V. The MOSFET has $V_t = 0.5$ V, $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$, $L = 0.4\ \mu\text{m}$, and $W = 5\ \mu\text{m}$. Specify the required values for R_S and R_D.

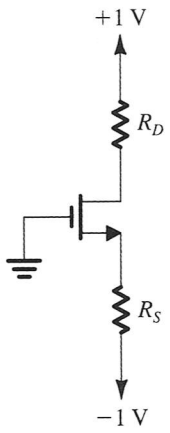

Figure P5.44

5.45 The NMOS transistor in the circuit of Fig. P5.44 has $V_t = 0.4$ V and $k_n = 4\ \text{mA/V}^2$. The voltages at the source and the drain are measured and found to be −0.6 V and +0.2 V, respectively. What current I_D is flowing, and what must the values of R_D and R_S be? What is the largest value for R_D for which I_D remains unchanged from the value found?

D 5.46 For the circuit in Fig. E5.10, assume that Q_1 and Q_2 are matched except for having different widths, W_1 and W_2. Let $V_t = 0.5$ V, $k_n' = 0.4\ \text{mA/V}^2$, $L_1 = L_2 = 0.36\ \mu\text{m}$, $W_1 = 1.44\ \mu\text{m}$, and $\lambda = 0$.

(a) Find the value of R required to establish a current of 50 μA in Q_1.
(b) Find W_2 and R_2 so that Q_2 operates at the edge of saturation with a current of 0.5 mA.

5.47 The transistor in the circuit of Fig. P5.47 has $k_n' = 0.4\ \text{mA/V}^2$, $V_t = 0.4$ V, and $\lambda = 0$. Show that operation at the edge of saturation is obtained when the following condition is satisfied:

$$\left(\frac{W}{L}\right) R_D \simeq 2.5\ \text{k}\Omega$$

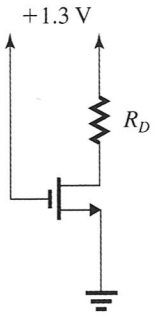

Figure P5.47

D 5.48 It is required to operate the transistor in the circuit of Fig. P5.47 at the edge of saturation with $I_D = 0.1$ mA. If $V_t = 0.4$ V, find the required value of R_D.

D 5.49 The PMOS transistor in the circuit of Fig. P5.49 has $V_t = -0.5$ V, $\mu_p C_{ox} = 100\ \mu\text{A/V}^2$, $L = 0.18\ \mu\text{m}$, and $\lambda = 0$. Find the values required for W and R in order to establish a drain current of 180 μA and a voltage V_D of 1 V.

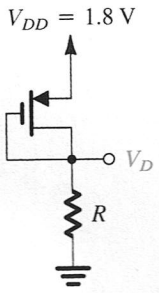

Figure P5.49

D 5.50 The NMOS transistors in the circuit of Fig. P5.50 have $V_t = 0.5$ V, $\mu_n C_{ox} = 250\ \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = 0.25\ \mu\text{m}$. Find the required values of gate width for each of Q_1

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