Section 5.3: MOSFET Circuits at DC

Note: If λ is not specified, assume it is zero.

D 5.44 Design the circuit of Fig. P5.44 to establish a drain current of 0.1 mA and a drain voltage of +0.3 V. The MOSFET has $V_t = 0.5$ V, $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$, $L = 0.4\ \mu$m, and $W = 5\ \mu$m. Specify the required values for R_S and R_D.

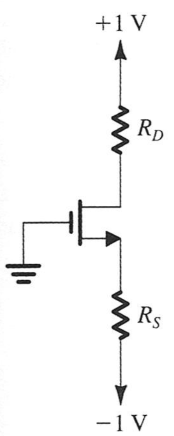

Figure P5.44

5.45 The NMOS transistor in the circuit of Fig. P5.44 has $V_t = 0.4$ V and $k_n = 4\ \text{mA/V}^2$. The voltages at the source and the drain are measured and found to be −0.6 V and +0.2 V, respectively. What current I_D is flowing, and what must the values of R_D and R_S be? What is the largest value for R_D for which I_D remains unchanged from the value found?

D 5.46 For the circuit in Fig. E5.10, assume that Q_1 and Q_2 are matched except for having different widths, W_1 and W_2. Let $V_t = 0.5$ V, $k_n' = 0.4\ \text{mA/V}^2$, $L_1 = L_2 = 0.36\ \mu$m, $W_1 = 1.44\ \mu$m, and $\lambda = 0$.

(a) Find the value of R required to establish a current of 50 μA in Q_1.
(b) Find W_2 and R_2 so that Q_2 operates at the edge of saturation with a current of 0.5 mA.

5.47 The transistor in the circuit of Fig. P5.47 has $k_n' = 0.4\ \text{mA/V}^2$, $V_t = 0.4$ V, and $\lambda = 0$. Show that operation at the edge of saturation is obtained when the following condition is satisfied:

$$\left(\frac{W}{L}\right) R_D \simeq 2.5\ \text{k}\Omega$$

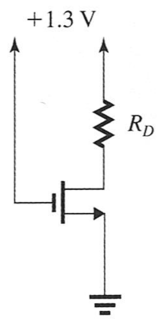

Figure P5.47

D 5.48 It is required to operate the transistor in the circuit of Fig. P5.47 at the edge of saturation with $I_D = 0.1$ mA. If $V_t = 0.4$ V, find the required value of R_D.

D 5.49 The PMOS transistor in the circuit of Fig. P5.49 has $V_t = -0.5$ V, $\mu_p C_{ox} = 100\ \mu\text{A/V}^2$, $L = 0.18\ \mu$m, and $\lambda = 0$. Find the values required for W and R in order to establish a drain current of 180 μA and a voltage V_D of 1 V.

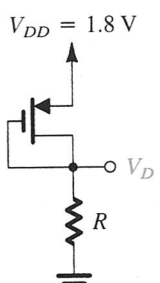

Figure P5.49

D 5.50 The NMOS transistors in the circuit of Fig. P5.50 have $V_t = 0.5$ V, $\mu_n C_{ox} = 250\ \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = 0.25\ \mu$m. Find the required values of gate width for each of Q_1

and Q_2, and the value of R, to obtain the voltage and current values indicated.

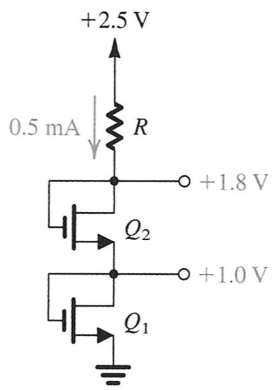

Figure P5.50

D 5.51 The NMOS transistors in the circuit of Fig. P5.51 have $V_t = 0.5$ V, $\mu_n C_{ox} = 90\ \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = L_3 = 0.5\ \mu$m. Find the required values of gate width for each of Q_1, Q_2, and Q_3 to obtain the voltage and current values indicated.

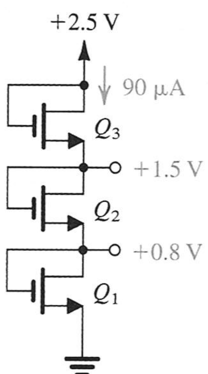

Figure P5.51

5.52 Consider the circuit of Fig. 5.24(a). In Example 5.5 it was found that when $V_t = 1$ V and $k_n'(W/L) = 1\ \text{mA/V}^2$, the drain current is 0.5 mA and the drain voltage is +7 V. If the transistor is replaced with another having $V_t = 1.5$ V with $k_n'(W/L) = 1.5\ \text{mA/V}^2$, find the new values of I_D and V_D. Comment on how tolerant (or intolerant) the circuit is to changes in device parameters.

D 5.53 Using a PMOS transistor with $V_t = -1.5$ V, $k_p'(W/L) = 4\ \text{mA/V}^2$, and $\lambda = 0$, design a circuit that resembles that in Fig. 5.24(a). Using a 10-V supply, design for a gate voltage of +6 V, a drain current of 0.5 mA, and a drain voltage of +5 V. Find the values of R_S and R_D. Also, find the values of the resistances in the voltage divider feeding the gate, assuming a 1-μA current in the divider.

5.54 The MOSFET in Fig. P5.54 has $V_t = 0.4$ V, $k_n' = 500\ \mu\text{A/V}^2$, and $\lambda = 0$. Find the required values of W/L and of R so that when $v_I = V_{DD} = +1.3$ V, $r_{DS} = 50\ \Omega$ and $v_O = 50$ mV.

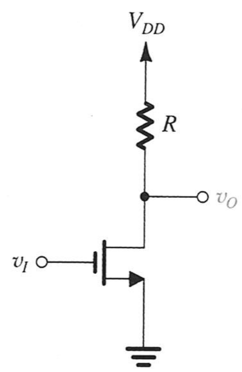

Figure P5.54

5.55 In the circuits shown in Fig. P5.55, transistors are characterized by $|V_t| = 1$ V, $k'W/L = 4\ \text{mA/V}^2$, and $\lambda = 0$.

(a) Find the labeled voltages V_1 through V_7.

(b) In each of the circuits, replace the current source with a resistor. Select the resistor value to yield a current as close to that of the current source as possible, while using resistors specified in the 1% table provided in Appendix J.

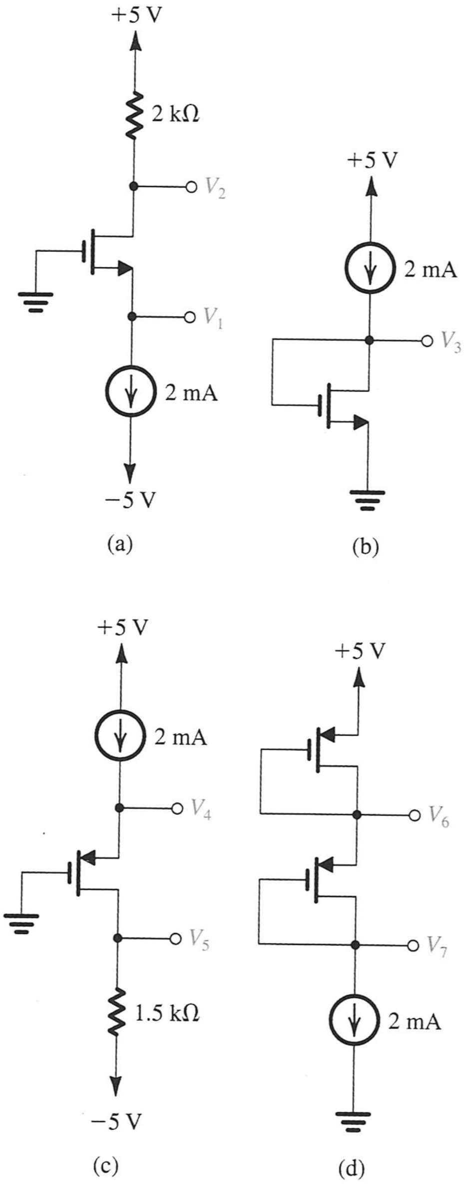

Figure P5.55

5.56 For each of the circuits in Fig. P5.56, find the labeled node voltages. For all transistors, $k_n'(W/L) = 0.5\ \text{mA/V}^2$, $V_t = 0.8$ V, and $\lambda = 0$.

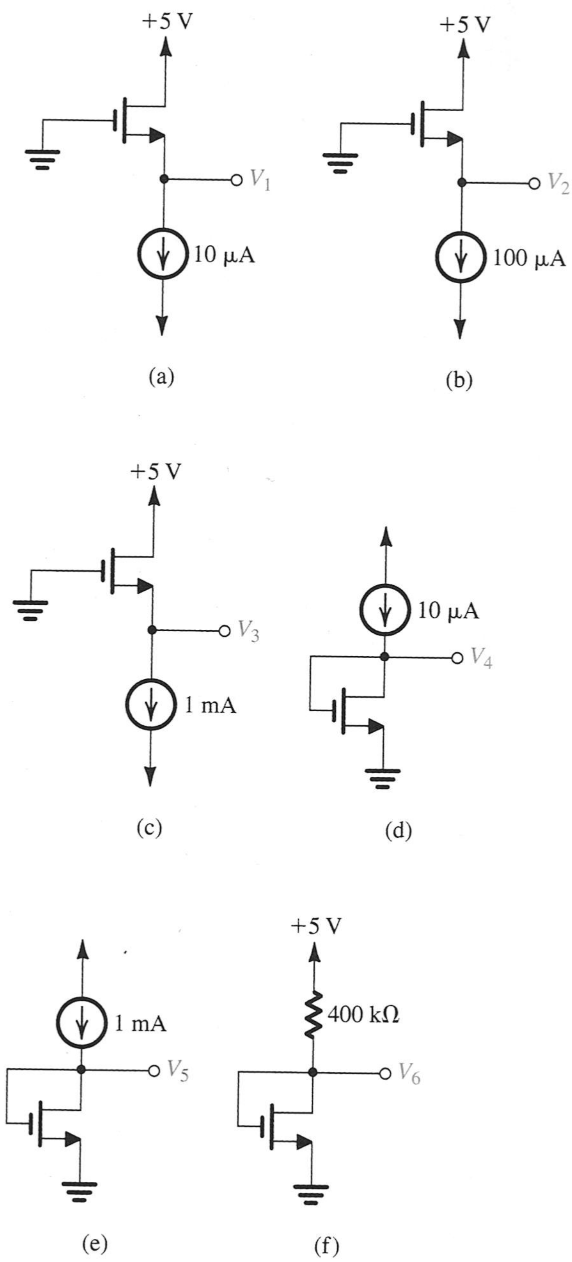

Figure P5.56 *continued*

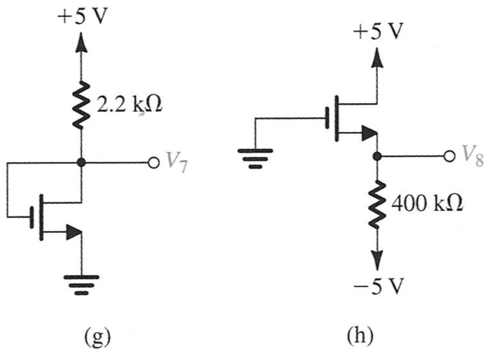

Figure P5.56 *continued*

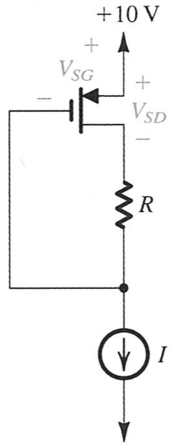

Figure P5.58

5.57 For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have $V_t = 0.9$ V and $k_n'(W/L) = 1.5$ mA/V^2.

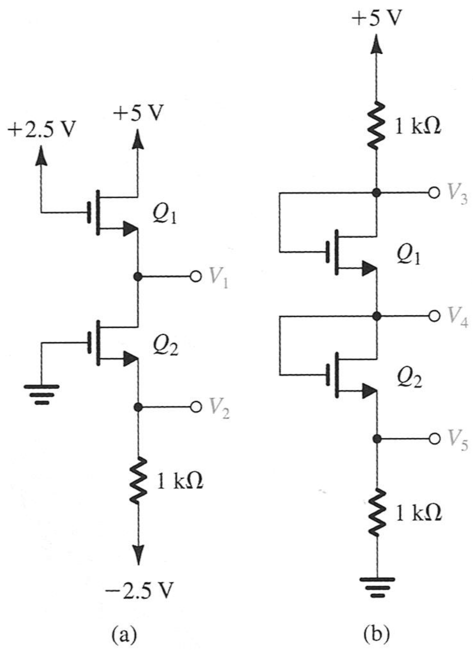

Figure P5.57

***5.58** For the circuit in Fig. P5.58:

(a) Show that for the PMOS transistor to operate in saturation, the following condition must be satisfied:

$$IR \leq |V_{tp}|$$

(b) If the transistor is specified to have $|V_{tp}| = 1$ V and $k_p = 0.2$ mA/V^2, and for $I = 0.1$ mA, find the voltages V_{SD} and V_{SG} for $R = 0$, 10 kΩ, 30 kΩ, and 100 kΩ.

5.59 For the circuits in Fig. P5.59, $\mu_n C_{ox} = 3\mu_p C_{ox} = 270\ \mu\text{A/V}^2$, $|V_t| = 0.5$ V, $\lambda = 0$, $L = 1\ \mu$m, and $W = 3\ \mu$m, unless otherwise specified. Find the labeled currents and voltages.

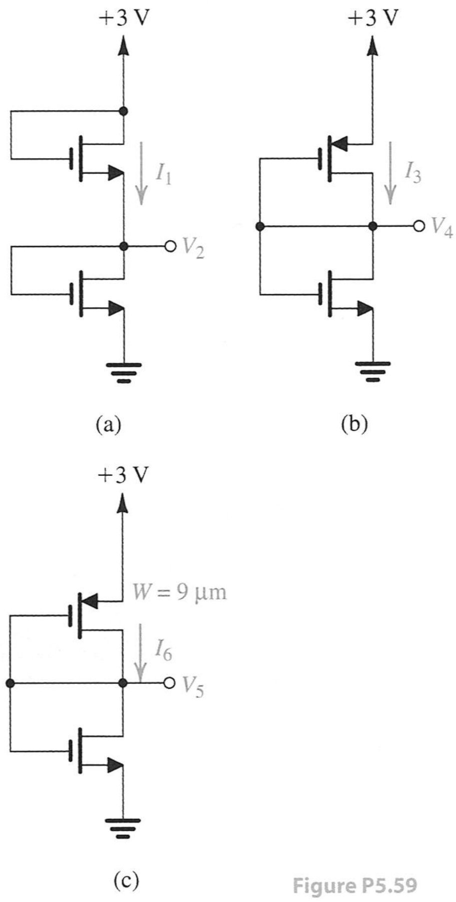

Figure P5.59

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

SIM *5.60 For the devices in the circuit of Fig. P5.60, $|V_t| = 1$ V, $\lambda = 0$, $\mu_n C_{ox} = 50\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 10\ \mu$m. Find V_2 and I_2. How do these values change if Q_3 and Q_4 are made to have $W = 100\ \mu$m?

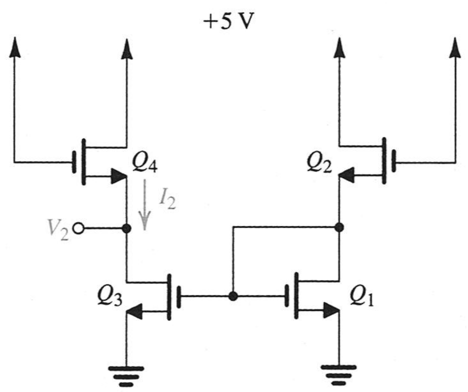

Figure P5.60

5.61 In the circuit of Fig. P5.61, transistors Q_1 and Q_2 have $V_t = 0.7$ V, and the process transconductance parameter $k_n' = 125\ \mu\text{A/V}^2$. Find V_1, V_2, and V_3 for each of the following cases:

(a) $(W/L)_1 = (W/L)_2 = 20$
(b) $(W/L)_1 = 1.5(W/L)_2 = 20$

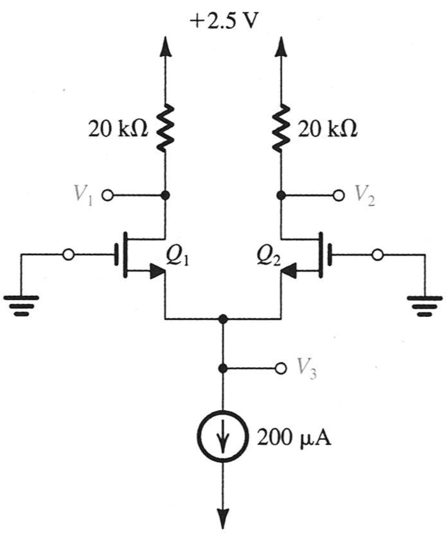

Figure P5.61

Section 5.4: The Body Effect and Other Topics

5.62 In a particular application, an n-channel MOSFET operates with V_{SB} in the range 0 V to 4 V. If V_{t0} is nominally 1.0 V, find the range of V_t that results if $\gamma = 0.5\ \text{V}^{1/2}$ and $2\phi_f = 0.6$ V. If the gate oxide thickness is increased by a factor of 4, what does the threshold voltage become?

5.63 A p-channel transistor operates in saturation with its source voltage 3 V lower than its substrate. For $\gamma = 0.5\ \text{V}^{1/2}$, $2\phi_f = 0.75$ V, and $V_{t0} = -0.7$ V, find V_t.

*5.64 (a) Using the expression for i_D in saturation and neglecting the channel-length modulation effect (i.e., let $\lambda = 0$), derive an expression for the per unit change in i_D per °C $\left[(\partial i_D/i_D)/\partial T\right]$ in terms of the per unit change in k_n' per °C $\left[(\partial k_n'/k_n')/\partial T\right]$, the temperature coefficient of V_t in V/°C $(\partial V_t/\partial T)$, and V_{GS} and V_t.
(b) If V_t decreases by 2 mV for every °C rise in temperature, find the temperature coefficient of k_n' that results in i_D decreasing by 0.2%/°C when the NMOS transistor with $V_t = 1$ V is operated at $V_{GS} = 5$ V.

5.65 A depletion-type n-channel MOSFET with $k_n' W/L = 2\ \text{mA/V}^2$ and $V_t = -3$ V has its source and gate grounded. Find the region of operation and the drain current for $v_D = 0.1$ V, 1 V, 3 V, and 5 V. Neglect the channel-length-modulation effect.

5.66 For a particular depletion-mode NMOS device, $V_t = -2$ V, $k_n' W/L = 200\ \mu\text{A/V}^2$, and $\lambda = 0.02\ \text{V}^{-1}$. When operated at $v_{GS} = 0$, what is the drain current that flows for $v_{DS} = 1$ V, 2 V, 3 V, and 10 V? What does each of these currents become if the device width is doubled with L the same? With L also doubled?

*5.67 Neglecting the channel-length-modulation effect, show that for the depletion-type NMOS transistor of Fig. P5.67, the i–v relationship is given by

$$i = \frac{1}{2}k_n'(W/L)\left(v^2 - 2V_t v\right) \qquad \text{for } v \geq V_t$$
$$i = -\frac{1}{2}k_n'(W/L)V_t^2 \qquad \text{for } v \leq V_t$$

(Recall that V_t is negative.) Sketch the i–v relationship for the case: $V_t = -2$ V and $k_n'(W/L) = 2\ \text{mA/V}^2$.

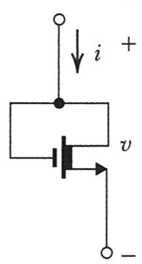

Figure P5.67