transistor β is specified to lie in the range 50 to 150, find the corresponding range of R_{out} and G_v.

7.87 An emitter follower, when driven from a 5-kΩ source, was found to have an output resistance R_{out} of 150 Ω. The output resistance increased to 250 Ω when the source resistance was increased to 10 kΩ. Find the overall voltage gain when the follower is driven by a 10-kΩ source and loaded by a 1-kΩ resistor.

7.88 For the general amplifier circuit shown in Fig. P7.88 neglect the Early effect.

(a) Find expressions for v_c/v_{sig} and v_e/v_{sig}.
(b) If v_{sig} is disconnected from node X, node X is grounded, and node Y is disconnected from ground and connected to v_{sig}, find the new expression for v_c/v_{sig}.

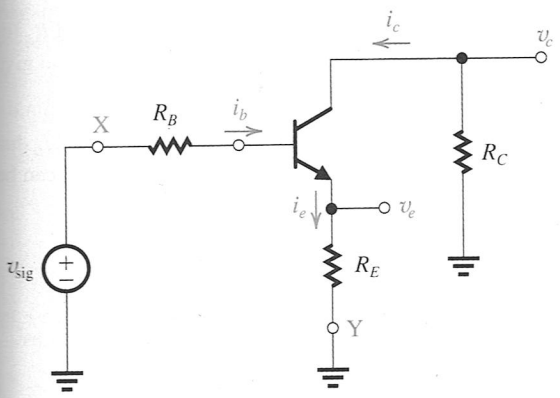

Figure P7.88

7.89 When the Early effect is neglected, the overall voltage gain of a CE amplifier with a collector resistance $R_C = 10$ kΩ is calculated to be −100 V/V. If the BJT is biased at $I_C = 1$ mA and the Early voltage is 100 V, provide a better estimate of the voltage gain G_v.

***7.90** Show that when r_o is taken into account, the voltage gain of the source follower becomes

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

Now, with R_L removed, the voltage gain is carefully measured and found to be 0.98. Then, when R_L is connected and its value is varied, it is found that the gain is halved at $R_L = 500$ Ω. If the amplifier remained linear throughout this measurement, what must the values of g_m and r_o be?

D 7.91 In this problem, we investigate the effect of changing the bias current I_C on the overall voltage gain G_v of a CE amplifier. Consider the situation of a CE amplifier operating with a signal source having $R_{sig} = 10$ kΩ and having $R_C \| R_L = 10$ kΩ. The BJT is specified to have $\beta = 100$ and $V_A = 25$ V. Use Eq. (7.114) (with r_o included in parallel with R_C and R_L in the numerator) to find $|G_v|$ at $I_C = 0.1$ mA, 0.2 mA, 0.5 mA, 1.0 mA, and 1.25 mA. Observe the effect of r_o on limiting $|G_v|$ as I_C is increased. Find the value of I_C that results in $|G_v| = 50$ V/V.

Section 7.4: Biasing

D 7.92 Consider the classical biasing scheme shown in Fig. 7.48(c), using a 9-V supply. For the MOSFET, $V_t = 1$ V, $\lambda = 0$, and $k_n = 2$ mA/V^2. Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of R_S and R_D. Use 22 MΩ for the larger of R_{G1} and R_{G2}. What are the values of R_{G1}, R_{G2}, R_S, and R_D that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

D 7.93 Using the circuit topology displayed in Fig. 7.48(e), arrange to bias the NMOS transistor at $I_D = 0.5$ mA with V_D midway between cutoff and the beginning of triode operation. The available supplies are ±5 V. For the NMOS transistor, $V_t = 1.0$ V, $\lambda = 0$, and $k_n = 1$ mA/V^2. Use a gate-bias resistor of 10 MΩ. Specify R_S and R_D to two significant digits.

D *7.94 In an electronic instrument using the biasing scheme shown in Fig. 7.48(c), a manufacturing error reduces R_S to zero. Let $V_{DD} = 15$ V, $R_{G1} = 10$ MΩ, and $R_{G2} = 5.1$ MΩ. What is the value of V_G created? If supplier specifications allow k_n to vary from 0.2 to 0.3 mA/V^2 and V_t to vary from 1.0 V to 1.5 V, what are the extreme values of I_D that may result? What value of R_S should have been installed to limit the maximum value of I_D to 1.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix J). What extreme values of current now result?

7.95 An NMOS transistor is connected in the bias circuit of Fig. 7.48(c), with $V_G = 5$ V and $R_S = 3$ kΩ. The transistor has $V_t = 1$ V and $k_n = 2$ mA/V^2. What bias current results? If a transistor for which k_n is 50% higher is used, what is the resulting percentage increase in I_D?

SIM 7.96 The bias circuit of Fig. 7.48(c) is used in a design with $V_G = 5$ V and $R_S = 2$ kΩ. For a MOSFET with

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

SIM **7.101** In the circuit of Fig. 7.50, let $R_G = 10\ \text{M}\Omega$, $R_D = 10\ \text{k}\Omega$, and $V_{DD} = 10\ \text{V}$. For each of the following two transistors, find the voltages V_D and V_G.

(a) $V_t = 1\ \text{V}$ and $k_n = 0.5\ \text{mA/V}^2$
(b) $V_t = 2\ \text{V}$ and $k_n = 1.25\ \text{mA/V}^2$

D 7.102 Using the feedback bias arrangement shown in Fig. 7.50 with a 5-V supply and an NMOS device for which $V_t = 1\ \text{V}$ and $k_n = 10\ \text{mA/V}^2$, find R_D to establish a drain current of 0.2 mA.

D 7.103 Figure P7.103 shows a variation of the feedback-bias circuit of Fig. 7.50. Using a 5-V supply with an NMOS transistor for which $V_t = 0.8\ \text{V}$, $k_n = 8\ \text{mA/V}^2$, and $\lambda = 0$, provide a design that biases the transistor at $I_D = 1\ \text{mA}$, with V_{DS} large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use 22 MΩ as the largest resistor in the feedback-bias network. What values of R_D, R_{G1}, and R_{G2} have you chosen? Specify all resistors to two significant digits.

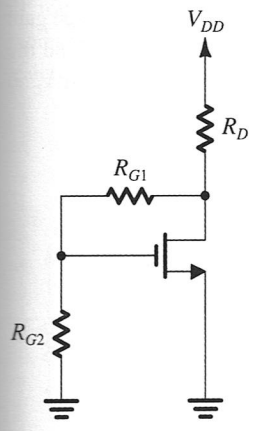

Figure P7.103

D 7.104 For the circuit in Fig. 7.51(a), neglect the base current I_B in comparison with the current in the voltage divider. It is required to bias the transistor at $I_C = 1\ \text{mA}$, which requires selecting R_{B1} and R_{B2} so that $V_{BE} = 0.710\ \text{V}$. If $V_{CC} = 3\ \text{V}$, what must the ratio R_{B1}/R_{B2} be? Now, if R_{B1} and R_{B2} are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for V_{BE}? What is the corresponding range of I_C? If $R_C = 2\ \text{k}\Omega$, what is the range obtained for V_{CE}? Comment on the efficacy of this biasing arrangement.

D 7.105 It is required to bias the transistor in the circuit of Fig. 7.51(b) at $I_C = 1\ \text{mA}$. The transistor β is specified to be nominally 100, but it can fall in the range of 50 to 150. For $V_{CC} = +3\ \text{V}$ and $R_C = 2\ \text{k}\Omega$, find the required value of R_B to achieve $I_C = 1\ \text{mA}$ for the "nominal" transistor. What is the expected range for I_C and V_{CE}? Comment on the efficacy of this bias design.

D 7.106 Consider the single-supply bias network shown in Fig. 7.52(a). Provide a design using a 9-V supply in which the supply voltage is equally split between R_C, V_{CE}, and R_E with a collector current of 0.6 mA. The transistor β is specified to have a minimum value of 90. Use a voltage-divider current of $I_E/10$, or slightly higher. Since a reasonable design should operate for the best transistors for which β is very high, do your initial design with $\beta = \infty$. Then choose suitable 5% resistors (see Appendix J), making the choice in a way that will result in a V_{BB} that is slightly higher than the ideal value. Specify the values you have chosen for R_E, R_C, R_1, and R_2. Now, find V_B, V_E, V_C, and I_C for your final design using $\beta = 90$.

D 7.107 Repeat Problem 7.106, but use a voltage-divider current that is $I_E/2$. Check your design at $\beta = 90$. If you have the data available, find how low β can be while the value of I_C does not fall below that obtained with the design of Problem 7.106 for $\beta = 90$.

D *7.108 It is required to design the bias circuit of Fig. 7.52 for a BJT whose nominal $\beta = 100$.

(a) Find the largest ratio (R_B/R_E) that will guarantee I_E remains within ±5% of its nominal value for β as low as 50 and as high as 150.
(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BB} \equiv V_{CC}R_2/(R_1 + R_2)$ that will result in a voltage drop of $V_{CC}/3$ across R_E.
(c) For $V_{CC} = 5\ \text{V}$, find the required values of R_1, R_2, and R_E to obtain $I_E = 0.5\ \text{mA}$ and to satisfy the requirement for stability of I_E in (a).
(d) Find R_C so that $V_{CE} = 1.0\ \text{V}$ for β equal to its nominal value.

Check your design by evaluating the resulting range of I_E.

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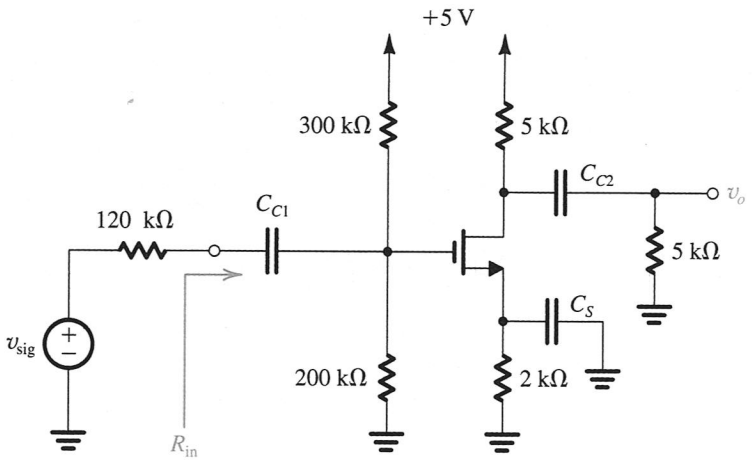


Figure P7.118

(d) What is the value of resistance R_s that needs to be inserted in series with capacitor C_S in order to allow us to double the input signal $\hat{v}_{sig}$? What output voltage now results?

SIM **D *7.119** The PMOS transistor in the CS amplifier of Fig. P7.119 has $V_{tp} = -0.7$ V and a very large $|V_A|$.

(a) Select a value for R_S to bias the transistor at $I_D = 0.3$ mA and $|V_{OV}| = 0.3$ V. Assume v_{sig} to have a zero dc component.

(b) Select a value for R_D that results in $G_v = -10$ V/V.

(c) Find the largest sinusoid $\hat{v}_{sig}$ that the amplifier can handle while remaining in the saturation region. What is the corresponding signal at the output?

(d) If to obtain reasonably linear operation, $\hat{v}_{sig}$ is limited to 50 mV, what value can R_D be increased to while maintaining saturation-region operation? What is the new value of G_v?

7.120 Figure P7.120 shows a scheme for coupling and amplifying a high-frequency pulse signal. The circuit utilizes

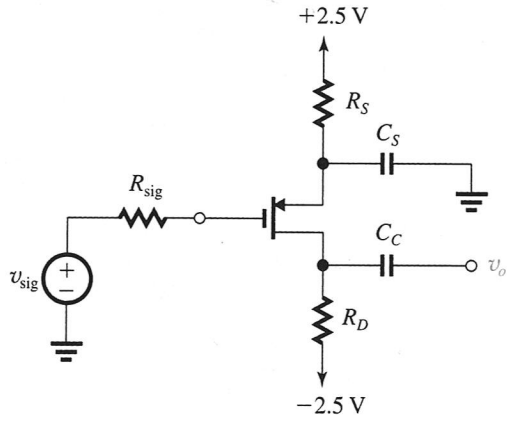


Figure P7.119

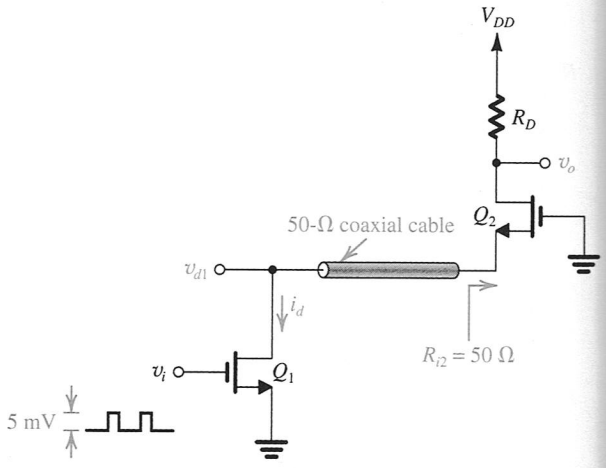


Figure P7.120

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

two MOSFETs whose bias details are not shown and a 50-Ω coaxial cable. Transistor Q_1 operates as a CS amplifier and Q_2 as a CG amplifier. For proper operation, transistor Q_2 is required to present a 50-Ω resistance to the cable. This situation is known as "proper termination" of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is 50 Ω. What must g_{m2} be? If Q_1 is biased at the same point as Q_2, what is the amplitude of the current pulses in the drain of Q_1? What is the amplitude of the voltage pulses at the drain of Q_1? What value of R_D is required to provide 1-V pulses at the drain of Q_2?

D ***7.121** The MOSFET in the circuit of Fig. P7.121 has $V_t = 0.8$ V, $k_n = 5$ mA/V^2, and $V_A = 40$ V.

(a) Find the values of R_S, R_D, and R_G so that $I_D = 0.4$ mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ±0.8 V is possible, and the input resistance at the gate is 10 MΩ. Neglect the Early effect.

(b) Find the values of g_m and r_o at the bias point.

(c) If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 MΩ, and terminal Y is connected to a load resistance of 10 kΩ, find the voltage gain from signal source to load.

(d) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?

(e) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 50 μA and having a resistance of 100 kΩ, find the voltage signal that can be measured at Y. For simplicity, neglect the effect of r_o.

***7.122**

(a) The NMOS transistor in the source-follower circuit of Fig. P7.122(a) has $g_m = 10$ mA/V and a large r_o. Find the open-circuit voltage gain and the output resistance.

(b) The NMOS transistor in the common-gate amplifier of Fig. P7.122(b) has $g_m = 10$ mA/V and a large r_o. Find the input resistance and the voltage gain.

(c) If the output of the source follower in (a) is connected to the input of the common-gate amplifier in (b), use the results of (a) and (b) to obtain the overall voltage gain v_o/v_i.

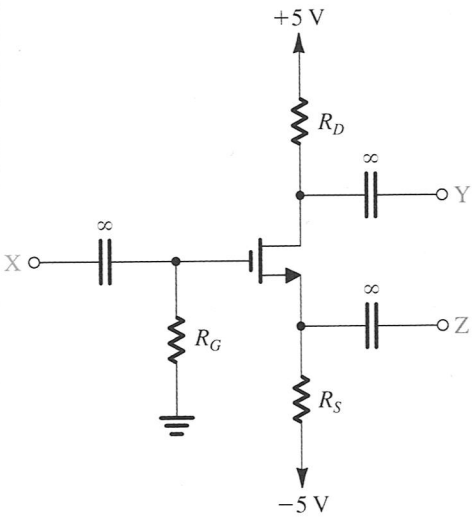
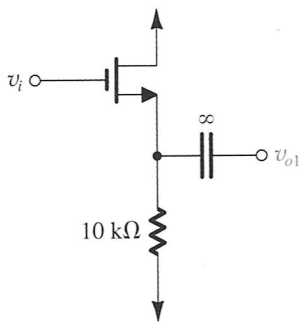
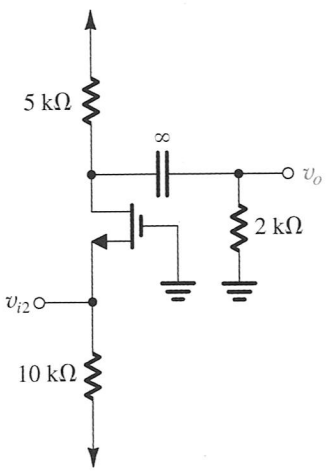


Figure P7.121



(a)



(b)

Figure P7.122

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

D **7.123 The MOSFET in the amplifier circuit of Fig. P7.123 has $V_t = 0.6$ V, $k_n = 5$ mA/V^2, and $V_A = 60$ V. The signal v_{sig} has a zero average.

(a) It is required to bias the transistor to operate at an overdrive voltage $V_{OV} = 0.2$ V. What must the dc voltage at the drain be? Calculate the dc drain current I_D taking into account V_A. Now, what value must the drain resistance R_D have?

(b) Calculate the values of g_m and r_o at the bias point established in (a).

(c) Using the small-signal equivalent circuit of the amplifier, show that the voltage gain is given by

$$\frac{v_o}{v_{sig}} = -\frac{R_2/R_1}{1+\dfrac{1+R_2/R_1}{g_m(R_D \parallel r_o \parallel R_2)(1-1/g_m R_2)}}$$

and find the value of the gain.

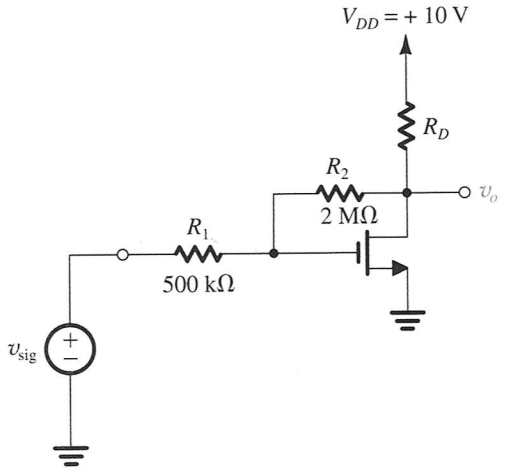


Figure P7.123

P.S. This feedback amplifier and the gain expression should remind you of an op amp utilized in the inverting configuration. We shall study feedback formally in Chapter 11.

D **7.124 The MOSFET in the amplifier circuit of Fig. P7.124 has $V_t = 0.6$ V and $k_n = 5$ mA/V^2. We shall assume that V_A is sufficiently large so that we can ignore the Early effect. The input signal v_{sig} has a zero average.

(a) It is required to bias the transistor to operate at an overdrive voltage $V_{OV} = 0.2$ V. What must the dc voltage at the drain be? Calculate the dc drain current I_D. What value must R_D have?

(b) Calculate the value of g_m at the bias point.

(c) Use the small-signal equivalent circuit of the amplifier to show that

$$\frac{v_o}{v_{sig}} = \frac{1+(R_2/R_1)}{1+\dfrac{(1+R_2/R_1)}{g_m R_D'}}$$

and

$$R_{in} = \frac{1}{g_m}\left(1+g_m R_D' \frac{R_1}{R_1+R_2}\right)$$

where

$$R_D' = R_D \parallel (R_1+R_2)$$

(d) Evaluate v_o/v_{sig} and R_{in}.

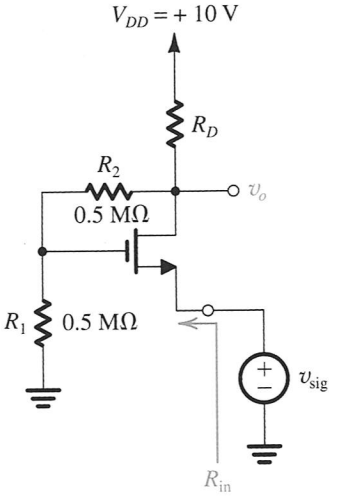


Figure P7.124

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem