P.S. This feedback amplifier circuit and the gain formula should remind you of an op amp connected in the noninverting configuration. We shall study feedback formally in Chapter 11.

7.125 For the common-emitter amplifier shown in Fig. P7.125, let $V_{CC} = 15$ V, $R_1 = 27$ kΩ, $R_2 = 15$ kΩ, $R_E = 2.4$ kΩ, and $R_C = 3.9$ kΩ. The transistor has $\beta = 100$. Calculate the dc bias current I_C. If the amplifier operates between a source for which $R_{sig} = 2$ kΩ and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, and the overall voltage gain v_o/v_{sig}.

D 7.126 Using the topology of Fig. P7.125, design an amplifier to operate between a 2-kΩ source and a 2-kΩ load with a gain v_o/v_{sig} of –40 V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has $\beta = 100$. Use standard 5% resistors (see Appendix J).

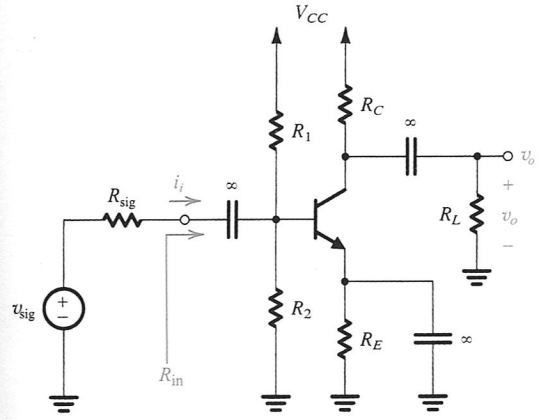

Figure P7.125

D 7.127 A designer, having examined the situation described in Problem 7.125 and estimating the available gain to be approximately –36.3 V/V, wants to explore the possibility of improvement by reducing the loading of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3: R_1 to 82 kΩ, R_2 to 47 kΩ, R_E to 7.2 kΩ, and R_C to 12 kΩ (standard values of 5%-tolerance resistors). With $V_{CC} = 15$ V, $R_{sig} = 2$ kΩ, $R_L = 2$ kΩ, and $\beta = 100$, what does the gain become? Comment.

D 7.128 The CE amplifier circuit of Fig. P7.128 is biased with a constant-current source I. It is required to design the circuit (i.e., find values for I, R_B, and R_C) to meet the following specifications:

(a) $R_{in} \simeq 10$ kΩ.
(b) The dc voltage drop across R_B is approximately 0.2 V.
(c) The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never fall by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that v_{sig} is a sinusoidal source, the available supply $V_{CC} = 5$ V, and the transistor has $\beta = 100$. Use standard 5% resistance values, and specify the value of I to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If $R_{sig} = R_L = 20$ kΩ, what is the overall voltage gain?

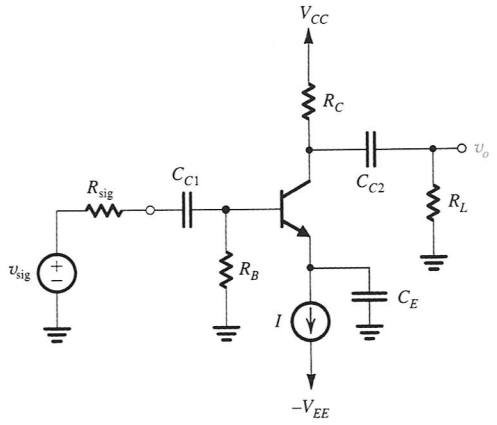

Figure P7.128

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

D 7.129 In the circuit of Fig. P7.129, v_{sig} is a small sine-wave signal with zero average. The transistor β is 100.

(a) Find the value of R_E to establish a dc emitter current of about 0.5 mA.

(b) Find R_C to establish a dc collector voltage of about +0.5 V.

(c) For $R_L = 10\ \text{k}\Omega$, draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

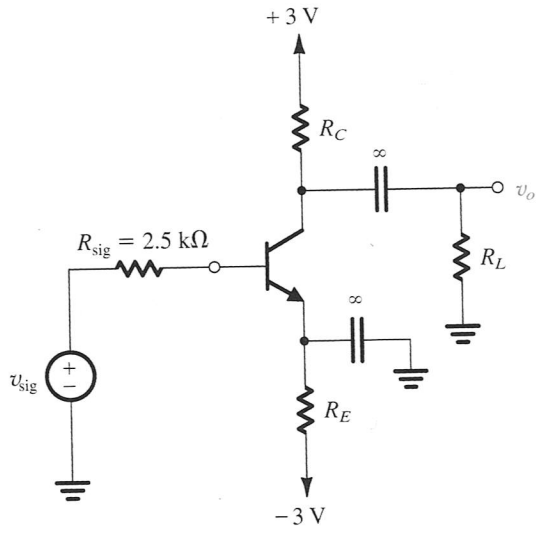

Figure P7.129

***7.130** The amplifier of Fig. P7.130 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage, R_{in2}, constitutes the load resistance of the first stage.

(a) For $V_{CC} = 15$ V, $R_1 = 100\ \text{k}\Omega$, $R_2 = 47\ \text{k}\Omega$, $R_E = 3.9\ \text{k}\Omega$, $R_C = 6.8\ \text{k}\Omega$, and $\beta = 100$, determine the dc collector current and dc collector voltage of each transistor.

(b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components.

(c) Find R_{in1} and v_{b1}/v_{sig} for $R_{sig} = 5\ \text{k}\Omega$.

(d) Find R_{in2} and v_{b2}/v_{b1}.

(e) For $R_L = 2\ \text{k}\Omega$, find v_o/v_{b2}.

(f) Find the overall voltage gain v_o/v_{sig}.

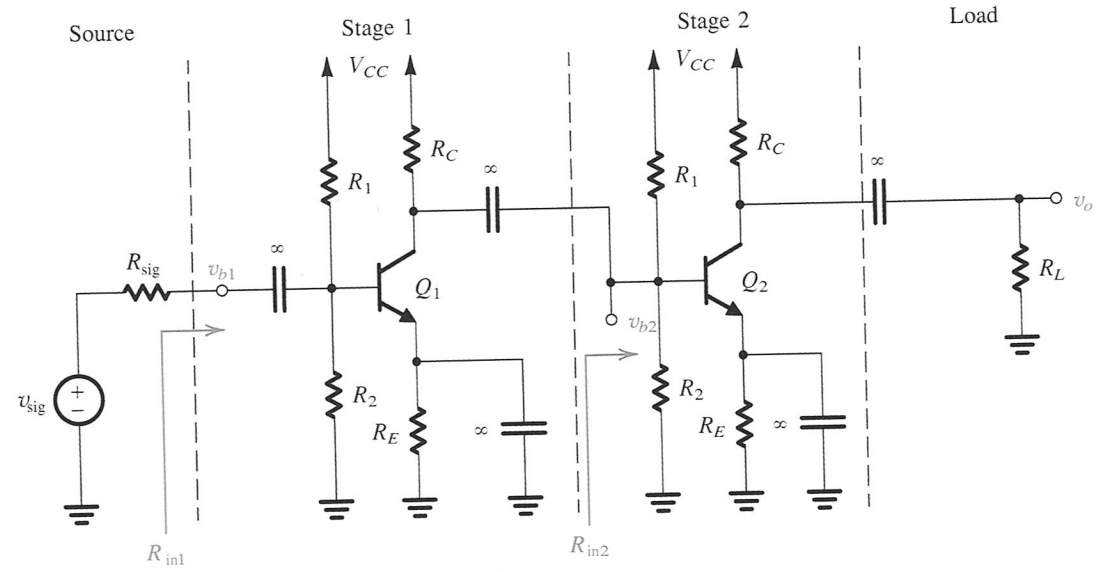

Figure P7.130

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

7.131 In the circuit of Fig. P7.131, the BJT is biased with a constant-current source, and v_{sig} is a small sine-wave signal. Find R_{in} and the gain v_o/v_{sig}. Assume $\beta = 100$. If the amplitude of the signal v_{be} is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

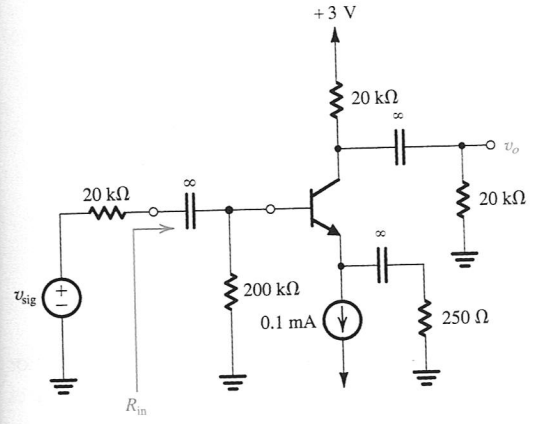

Figure P7.131

***7.132** The BJT in the circuit of Fig. P7.132 has $\beta = 100$.

(a) Find the dc collector current and the dc voltage at the collector.

(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_o/v_i.

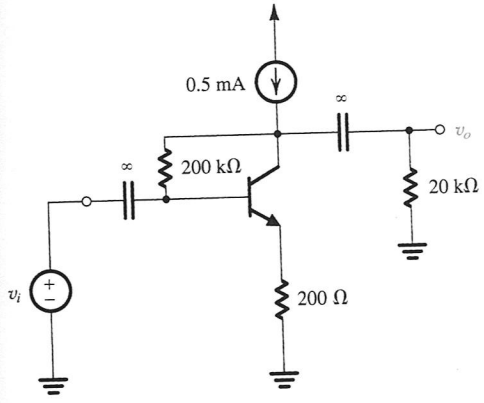

Figure P7.132

7.133 For the circuit in Fig. P7.133, find the input resistance R_{in} and the voltage gain v_o/v_{sig}. Assume that the source provides a small signal v_{sig} and that $\beta = 100$.

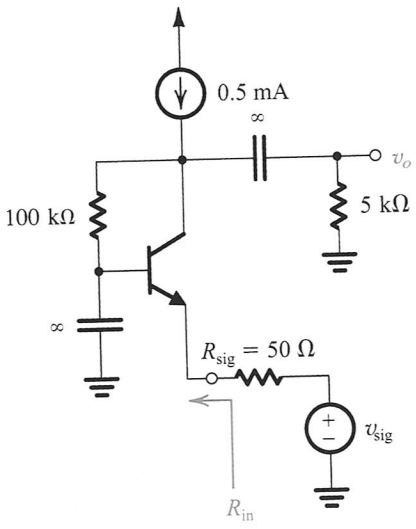

Figure P7.133

7.134 For the emitter-follower circuit shown in Fig. P7.134, the BJT used is specified to have β values in the range of 50 to 200 (a distressing situation for the circuit designer).

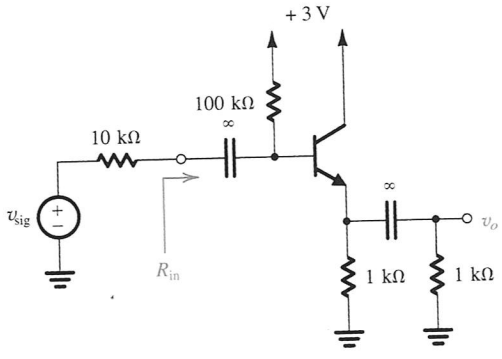

Figure P7.134

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

For the two extreme values of β ($\beta = 50$ and $\beta = 200$), find:

(a) I_E, V_E, and V_B
(b) the input resistance R_{in}
(c) the voltage gain v_o/v_{sig}

7.135 For the emitter follower in Fig. P7.135, the signal source is directly coupled to the transistor base. If the dc component of v_{sig} is zero, find the dc emitter current. Assume $\beta = 100$. Neglecting r_o, find R_{in}, the voltage gain v_o/v_{sig}, the current gain i_o/i_i, and the output resistance R_{out}.

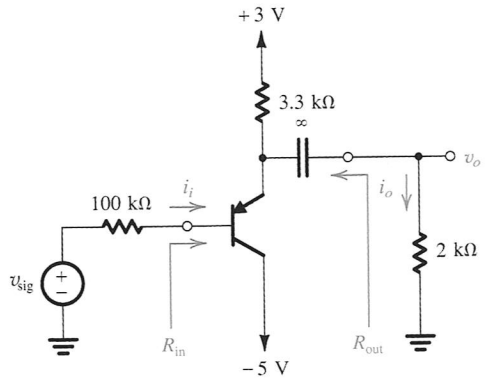

Figure P7.135

7.136 For the circuit in Fig. P7.136, called a **bootstrapped follower:**

(a) Find the dc emitter current and g_m, r_e, and r_π. Use $\beta = 100$.
(b) Replace the BJT with its T model (neglecting r_o), and analyze the circuit to determine the input resistance R_{in} and the voltage gain v_o/v_{sig}.
(c) Repeat (b) for the case when capacitor C_B is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

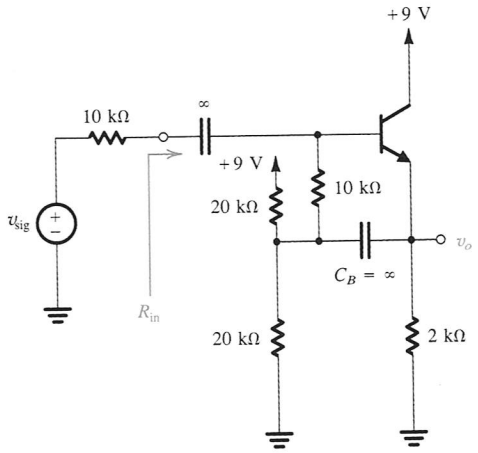

Figure P7.136

7.137 For the follower circuit in Fig. P7.137, let transistor Q_1 have $\beta = 50$ and transistor Q_2 have $\beta = 100$, and neglect the effect of r_o. Use $V_{BE} = 0.7$ V.

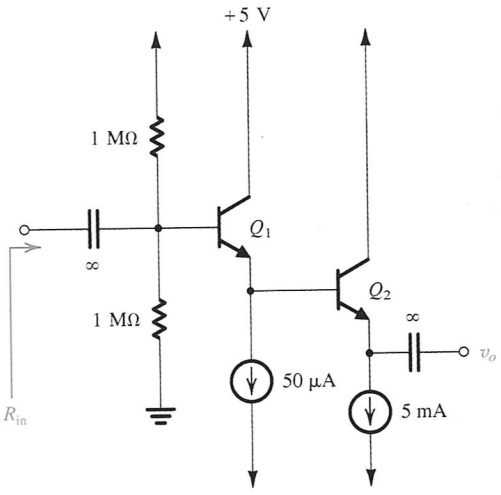

Figure P7.137

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem