8.34 Fill in the table below. For the BJT, let $\beta = 100$ and $V_A = 100$ V. For the MOSFET, let $\mu_n C_{ox} = 200\ \mu A/V^2$, $W/L = 40$, and $V_A = 10$ V.

	BJT Cell		MOSFET Cell	
Bias Current	$I_C = 0.1$ mA	$I_C = 1$ mA	$I_D = 0.1$ mA	$I_D = 1$ mA
g_m (mA/V)				
r_o (kΩ)				
A_0 (V/V)				
R_{in} (kΩ)				

8.35 A CS amplifier utilizes an NMOS transistor with $L = 0.54\ \mu m$ and $W/L = 8$. It was fabricated in a 0.18-μm CMOS process for which $\mu_n C_{ox} = 400\ \mu A/V^2$ and $V_A' = 5$ V/μm. What is the bias current of the transistor for which $A_0 = 18$ V/V?

8.36 A CS amplifier utilizes an NMOS transistor with $L = 0.36\ \mu m$ and $W/L = 8$. It was fabricated in a 0.18-μm CMOS process for which $\mu_n C_{ox} = 400\ \mu A/V^2$ and $V_A' = 5$ V/μm. Find the values of g_m and A_0 obtained at $I_D = 25\ \mu A$, 250 μA, and 2.5 mA.

D 8.37 An NMOS transistor is fabricated in the 0.18-μm process whose parameters are given in Table J.1 in Appendix J. The device has a channel length twice the minimum and is operated at $V_{OV} = 0.25$ V and $I_D = 10\ \mu A$.

(a) What values of g_m, r_o, and A_0 are obtained?
(b) If I_D is increased to 100 μA, what do V_{OV}, g_m, r_o, and A_0 become?
(c) If the device is redesigned with a new value of W so that it operates at $V_{OV} = 0.25$ V for $I_D = 100\ \mu A$, what do g_m, r_o, and A_0 become?
(d) If the redesigned device in (c) is operated at 10 μA, find V_{OV}, g_m, r_o, and A_0.
(e) Which designs and operating conditions produce the lowest and highest values of A_0? What are these values? In each of these two cases, if W/L is held at the same value but L is made 10 times larger, what gains result?

D 8.38 Find A_0 for an NMOS transistor fabricated in a CMOS process for which $k_n' = 400\ \mu A/V^2$ and $V_A' = 6$ V/μm. The transistor has a 0.5-μm channel length and is operated with an overdrive voltage of 0.15 V. What must W be for the NMOS transistor to operate at $I_D = 100\ \mu A$? Also, find the values of g_m and r_o.

D 8.39 Using a CMOS technology for which $k_n' = 200\ \mu A/V^2$ and $V_A' = 20$ V/μm, design a current-source-loaded CS amplifier for operation at $I = 50\ \mu A$ with $V_{OV} = 0.2$ V. The amplifier is to have an open-circuit voltage gain of −100 V/V. Assume that the current-source load is ideal. Specify L and W/L.

D 8.40 The circuit in Fig. 8.15(a) is fabricated in a process for which $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\ \mu A/V^2$, $V_{An}' = |V_{Ap}'| = 20$ V/μm, $V_{tn} = -V_{tp} = 0.5$ V, and $V_{DD} = 2.5$ V. The two transistors have $L = 0.5\ \mu m$ and are to be operated at $I_D = 100\ \mu A$ and $|V_{OV}| = 0.3$ V. Find the required values of V_G, $(W/L)_1$, $(W/L)_2$, and A_v.

D 8.41 The circuit in Fig. 8.15(a) is fabricated in a 0.18-μm CMOS technology for which $\mu_n C_{ox} = 400\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.5$ V, $V_{An}' = 5$ V/μm, $|V_{Ap}'| = 5$ V/μm, and $V_{DD} = 1.8$ V. It is required to design the circuit to obtain a voltage gain $A_v = -40$ V/V. Use devices of equal length L operating at $I = 100\ \mu A$ and $|V_{OV}| = 0.25$ V. Determine the required values of V_G, L, $(W/L)_1$, and $(W/L)_2$.

8.42 Figure P8.42 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2, find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2. If Q_1 and Q_2 are to be operated at equal overdrive voltages, $|V_{OV}|$, find the required value of $|V_{OV}|$ if $|V_A| = 5$ V and the gain required is 400 V/V.

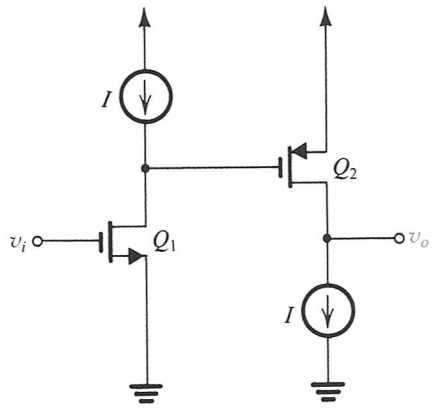

Figure P8.42

***8.43** The NMOS transistor in the circuit of Fig. P8.43 has $V_t = 0.5$ V, $k_n'W/L = 2$ mA/V², and $V_A = 20$ V.

(a) Neglecting the dc current in the feedback network and the effect of r_o, find V_{GS}. Then find the dc current in the feedback network and V_{DS}. Verify that you were justified in neglecting the current in the feedback network when you found V_{GS}.

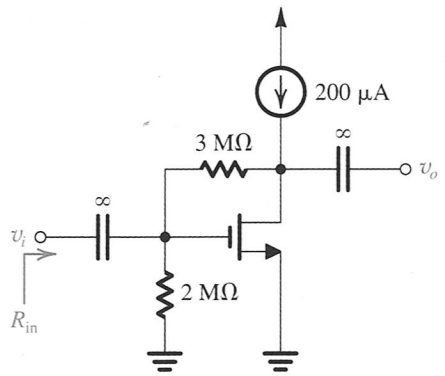

Figure P8.43

(b) Find the small-signal voltage gain, v_o/v_i. What is the peak of the largest output sine-wave signal that is possible while the NMOS transistor remains in saturation? What is the corresponding input signal?
(c) Find the small-signal input resistance R_{in}.

D 8.44 Consider the CMOS amplifier of Fig. 8.16(a) when fabricated with a process for which $k_n' = 4k_p' = 400\ \mu A/V^2$, $|V_t| = 0.5$ V, and $|V_A| = 5$ V. Find I_{REF} and $(W/L)_1$ to obtain a voltage gain of –40 V/V and an output resistance of 100 kΩ. Recall that Q_2 and Q_3 are matched. If Q_2 and Q_3 are to be operated at the same overdrive voltage as Q_1, what must their W/L ratios be?

8.45 Consider the CMOS amplifier analyzed in Example 8.4. If v_I consists of a dc bias component on which is superimposed a sinusoidal signal, find the value of the dc component that will result in the maximum possible signal swing at the output with almost-linear operation. What is the amplitude of the output sinusoid resulting? (*Note:* In practice, the amplifier would have a feedback circuit that caused it to operate at a point near the middle of its linear region.)

8.46 The power supply of the CMOS amplifier analyzed in Example 8.4 is increased to 5 V. What will the extent of the linear region at the output become?

****8.47** Consider the circuit shown in Fig. 8.16(a), using a 3.3-V supply and transistors for which $|V_t| = 0.8$ V and $L = 1\ \mu m$. For Q_1, $k_n' = 100\ \mu A/V^2$, $V_A = 100$ V, and $W = 20\ \mu m$. For Q_2 and Q_3, $k_p' = 50\ \mu A/V^2$ and $|V_A| = 50$ V. For Q_2, $W = 40\ \mu m$. For Q_3, $W = 10\ \mu m$.

(a) If Q_1 is to be biased at 100 μA, find I_{REF}. For simplicity, ignore the effect of V_A.
(b) What are the extreme values of v_O for which Q_1 and Q_2 just remain in saturation?
(c) What is the large-signal voltage gain?
(d) Find the slope of the transfer characteristic at $v_O = V_{DD}/2$.
(e) For operation as a small-signal amplifier around a bias point at $v_O = V_{DD}/2$, find the small-signal voltage gain and output resistance.

****8.48** The MOSFETs in the circuit of Fig. P8.48 are matched, having $k_n'(W/L)_1 = k_p'(W/L)_2 = 1\ mA/V^2$ and $|V_t| = 0.5$ V. The resistance $R = 1\ M\Omega$.

(a) For G and D open, what are the drain currents I_{D1} and I_{D2}?
(b) For $r_o = \infty$, what is the voltage gain of the amplifier from G to D? (*Hint*: Replace the transistors with their small-signal models.)
(c) For finite r_o ($|V_A| = 20$ V), what is the voltage gain from G to D and the input resistance at G?
(d) If G is driven (through a large coupling capacitor) from a source v_{sig} having a resistance of 20 kΩ, find the voltage gain v_d/v_{sig}.
(e) For what range of output signals do Q_1 and Q_2 remain in the saturation region?

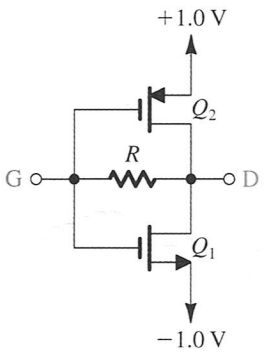

Figure P8.48

8.49 Transistor Q_1 in the circuit of Fig. P8.49 is operating as a CE amplifier with an active load provided by transistor Q_2, which is the output transistor in a current mirror formed by Q_2 and Q_3. (Note that the biasing arrangement for Q_1 is *not* shown.)

(a) Neglecting the finite base currents of Q_2 and Q_3 and assuming that their $V_{BE} \simeq 0.7$ V and that Q_2 has five times the area of Q_3, find the value of I.
(b) If Q_1 and Q_2 are specified to have $|V_A| = 30$ V, find r_{o1} and r_{o2} and hence the total resistance at the collector of Q_1.

(c) Find $r_{\pi 1}$ and g_{m1} assuming that $\beta_1 = 50$.
(d) Find R_{in}, A_v, and R_o.

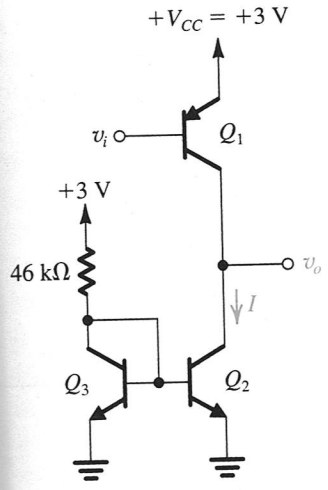

Figure P8.49

D 8.50 It is required to design the CMOS amplifier of Fig. 8.16(a) utilizing a 0.18-μm process for which $k_n' = 387\ \mu A/V^2$, $k_p' = 86\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.5$ V, $V_{DD} = 1.8$ V, $V_{An}' = 5$ V/μm, and $V_{Ap}' = -6$ V/μm. The output voltage must be able to swing to within approximately 0.2 V of the power-supply rails (i.e., from 0.2 V to 1.6 V), and the voltage gain must be at least 10 V/V. Design for a dc bias current of 50 μA, and use devices with the same channel length. If the channel length is an integer multiple of the minimum 0.18 μm, what channel length is needed and what W/L ratios are required? If it is required to raise the gain by a factor of 2, what channel length would be required, and by what factor does the total gate area of the circuit increase?

Section 8.4: The CG and CB Amplifiers

8.51 A CG amplifier operating with $g_m = 2$ mA/V and $r_o = 20$ kΩ is fed with a signal source having $R_s = 1$ kΩ and is loaded in a resistance $R_L = 20$ kΩ. Find R_{in}, R_{out}, and v_o/v_{sig}.

8.52 A CG amplifier operating with $g_m = 2$ mA/V and $r_o = 20$ kΩ is fed with a signal source having a Norton equivalent composed of a current signal i_{sig} and a source resistance $R_s = 20$ kΩ. The amplifier is loaded in a resistance $R_L = 20$ kΩ. Find R_{in} and i_o/i_{sig}, where i_o is the current through the load R_L. If R_L increases by a factor of 10, by what percentage does the current gain change? Can you see the effectiveness of the CG as a current buffer?

D 8.53 It is required to design the current source in Fig. P8.53 to deliver a current of 0.2 mA with an output resistance of 500 kΩ. The transistor has $V_A = 20$ V and $V_t = 0.5$ V. Design for $V_{OV} = 0.2$ V and specify R_s and V_{BIAS}.

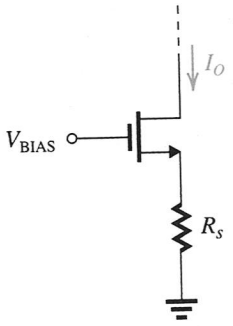

Figure P8.53

D 8.54 Figure P8.54 shows a current source realized using a current mirror with two matched transistors Q_1 and Q_2. Two equal resistances R_s are inserted in the source leads to increase the output resistance of the current source. If Q_2 is operating at $g_m = 1$ mA/V and has $V_A = 10$ V, and if the maximum allowed dc voltage drop across R_s is 0.3 V, what is the maximum available output resistance of the current source? Assume that the voltage at the common-gate node is approximately constant.

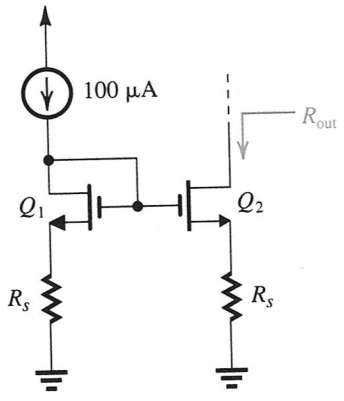

Figure P8.54

8.55 In the common-gate amplifier circuit of Fig. P8.55, Q_2 and Q_3 are matched. $k_n'(W/L)_n = k_p'(W/L)_p = 4\ mA/V^2$, and all transistors have $|V_t| = 0.8$ V and $|V_A| = 20$ V.

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

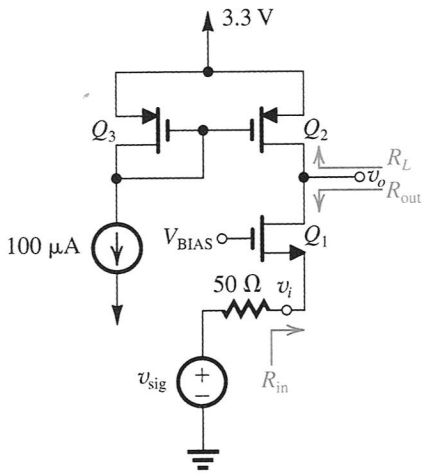

Figure P8.55

The signal v_{sig} is a small sinusoidal signal with no dc component.

(a) Neglecting the effect of V_A, find the dc drain current of Q_1 and the required value of V_{BIAS}.
(b) Find the values of g_{m1} and r_o for all transistors.
(c) Find the value of R_{in}.
(d) Find the value of R_{out}.
(e) Calculate the voltage gains v_o/v_i and v_o/v_{sig}.
(f) How large can v_{sig} be (peak-to-peak) while maintaining saturation-mode operation for Q_1 and Q_2?

8.56 For the CB amplifier, use Eq. (8.63) to explore the variation of the input resistance R_{in} with the load resistance R_L. Specifically, find R_{in} as a multiple of r_e for $R_L/r_o = 0$, 1, 10, 100, 1000, and ∞. Let $\beta = 100$. Present your results in tabular form.

8.57 What value of load resistance R_L causes the input resistance of the CB amplifier to be approximately double the value of r_e?

8.58 Show that for the CB amplifier,

$$\frac{R_{out}}{r_o} \simeq 1 + \frac{\beta(R_e/r_e)}{\beta + 1 + (R_e/r_e)}$$

Generate a table for R_{out} as a multiple of r_o versus R_e as a multiple of r_e with entries for $R_e = 0$, r_e, $2r_e$, $10r_e$, $(\beta/2)r_e$, βr_e, and $1000r_e$. Let $\beta = 100$.

8.59 As mentioned in the text, the CB amplifier functions as a current buffer. That is, when fed with a current signal, it passes it to the collector and supplies the output collector current at a high output resistance. Figure P8.59 shows a CB amplifier fed with a signal current i_{sig} having a source resistance $R_{sig} = 10\,k\Omega$. The BJT is specified to have $\beta = 100$ and $V_A = 50$ V. (Note that the bias arrangement is not shown.) The output at the collector is represented by its Norton equivalent circuit. Find the value of the current gain k and the output resistance R_{out}. Note that k is the short-circuit current gain and should be evaluated using the T model of the transistor with the collector short-circuited to ground.

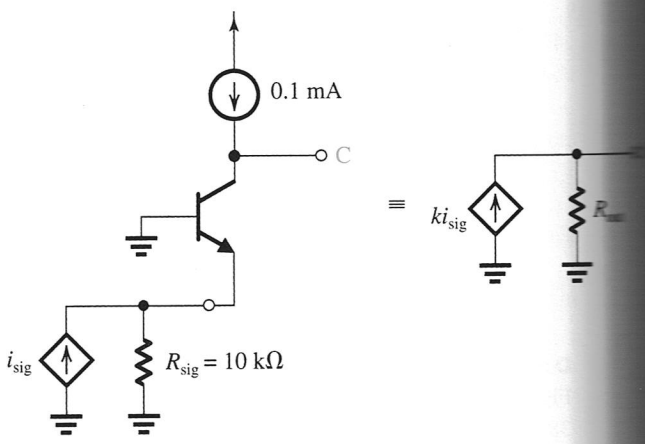

Figure P8.59

8.60 For the constant-current source circuit shown in Fig. P8.60, find the collector current I and the output resistance. The BJT is specified to have $\beta = 100$, $V_{BE} = 0.7$ V, and $V_A = 100$ V. If the collector voltage undergoes a change of 10 V while the BJT remains in the active mode, what is the corresponding change in collector current?

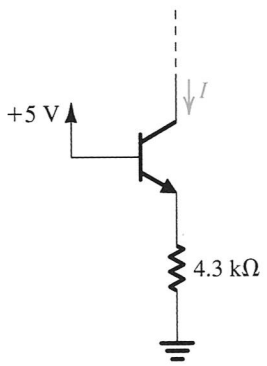

Figure P8.60

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

8.61 Find the value of the resistance R_e, which, when connected in the emitter lead of a CE BJT amplifier, raises the output resistance by a factor of (a) 5, (b) 10, and (c) 50. What is the maximum possible factor by which the output resistance can be raised, and at what value of R_e is it achieved? Assume the BJT has $\beta = 100$ and is biased at $I_C = 0.5$ mA.

Section 8.5: The Cascode Amplifier

D 8.62 In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 50. If the transistor is operated at $V_{OV} = 0.2$ V, what must its V_A be? If the process technology specifies V_A' as 5 V/μm, what channel length must the transistor have?

D 8.63 For a cascode current source such as that in Fig. 8.32, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by $IR_o = 2|V_A|^2/|V_{OV}|$. Now consider the case of transistors that have $|V_A| = 4$ V and are operated at $|V_{OV}|$ of 0.2 V. Also, let $\mu_p C_{ox} = 100$ μA/V^2. Find the W/L ratios required and the output resistance realized for the two cases: (a) $I = 0.1$ mA and (b) $I = 0.5$ mA. Assume that V_{SD} for the two devices is the minimum required (i.e., $|V_{OV}|$).

D *8.64 For a cascode current source, such as that in Fig. 8.32, show that if the two transistors are identical, the current I supplied by the current source and the output resistance R_o are related by

$$IR_o = \frac{2|V_A'|^2}{|V_{OV}|}L^2$$

Now consider the case of a 0.18-μm technology for which $|V_A'| = 5$ V/μm and let the transistors be operated at $|V_{OV}| = 0.2$ V. Find the figure-of-merit IR_o for the three cases of L equal to the minimum channel length, twice the minimum, and three times the minimum. Complete the entries of the table at the bottom of the page. Give W/L and the area $2WL$ in terms of n, where n is the value of W/L for the case $I = 0.01$ mA. In the table, A_v denotes the gain obtained in a cascode amplifier such as that in Fig. 8.33 that utilizes our current source as load and which has the same values of g_m and R_o as the current-source transistors.

(a) For each current value, what is price paid for the increase in R_o and A_v obtained as L is increased?
(b) For each value of L, what advantage is obtained as I is increased, and what is the price paid? (*Hint:* We will see in Chapter 10 that the amplifier bandwidth increases with g_m.)
(c) Contrast the performance obtained from the circuit with the largest area with that obtained from the circuit with the smallest area.

D 8.65 Design the cascode amplifier of Fig. 8.30(a) to obtain $g_{m1} = 2$ mA/V and $R_o = 200$ kΩ. Use a 0.18-μm technology for which $V_{tn} = 0.5$ V, $V_A' = 5$ V/μm, and $k_n' = 400$ μA/V^2. Determine L, W/L, V_{G2}, and I. Use identical transistors operated at $V_{OV} = 0.25$ V, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?

8.66 The cascode amplifier of Fig. 8.33 is operated at a current of 0.2 mA with all devices operating at $|V_{OV}| = 0.20$ V.

	$L = L_{min} = 0.18$ μm $IR_o =$ V				$L = 2L_{min} = 0.36$ μm $IR_o =$ V				$L = 3L_{min} = 0.54$ μm $IR_o =$ V			
	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm^2)	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm^2)	g_m (mA/V)	R_o (kΩ)	A_v (V/V)	$2WL$ (μm^2)
$I = 0.01$ mA $W/L = n$												
$I = 0.1$ mA $W/L =$												
$I = 1.0$ mA $W/L =$												

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

All devices have $|V_A| = 4$ V. Find g_{m1}, the output resistance of the amplifier, R_{on}, the output resistance of the current source, R_{op}, the overall output resistance, R_o, and the voltage gain, A_v.

D 8.67 Design the CMOS cascode amplifier in Fig. 8.33 for the following specifications: $g_{m1} = 1$ mA/V and $A_v = -280$ V/V. Assume that for the available fabrication process, $|V_A'| = 5$ V/μm for both NMOS and PMOS devices and that $\mu_n C_{ox} = 4\,\mu_p C_{ox} = 400$ μA/V^2. Use the same channel length L for all devices and operate all four devices at $|V_{OV}| = 0.25$ V. Determine the required channel length L, the bias current I, and the W/L ratio for each of four transistors. Assume that suitable bias voltages have been chosen, and neglect the Early effect in determining the W/L ratios.

D 8.68 Design the circuit of Fig. 8.32 to provide an output current of 100 μA. Use $V_{DD} = 3.3$ V, and assume the PMOS transistors to have $\mu_p C_{ox} = 60$ μA/V^2, $V_{tp} = -0.8$ V, and $|V_A| = 5$ V. The current source is to have the widest possible signal swing at its output. Design for $V_{OV} = 0.2$ V, and specify the values of the transistor W/L ratios and of V_{G3} and V_{G4}. What is the highest allowable voltage at the output? What is the value of R_o?

8.69 The cascode transistor can be thought of as providing a "shield" for the input transistor from the voltage variations at the output. To quantify this "shielding" property of the cascode, consider the situation in Fig. P8.69. Here we have grounded the input terminal (i.e., reduced v_i to zero), applied a small change v_x to the output node, and denoted the voltage change that results at the drain of Q_1 by v_y. By what factor is v_y smaller than v_x?

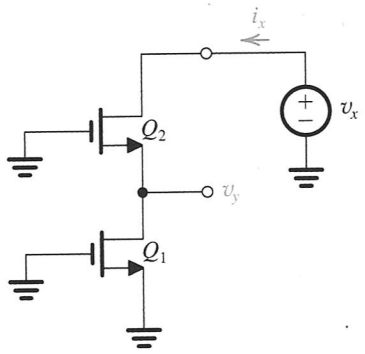

Figure P8.69

***8.70** In this problem we investigate whether, as an alternative to cascoding, we can simply increase the channel length L of the CS MOSFET. Specifically, we wish to compare the two circuits shown in Fig. P8.70(b) and (c). The circuit in Fig. P8.70(b) is a CS amplifier in which the channel length has been quadrupled relative to that of the original CS amplifier in Fig. P8.70(a) while the drain bias current has been kept constant.

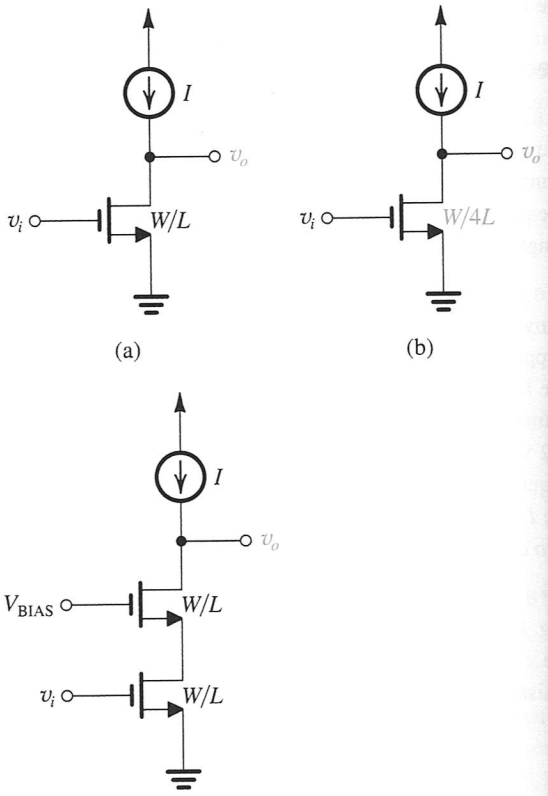

Figure P8.70

(a) Show that for this circuit V_{OV} is double that of the original circuit, g_m is half that of the original circuit, and $\frac{v_o}{v_i}$ is double that of the original circuit.

(b) Compare these values to those of the cascode circuit in Fig. P8.70(c), which is operating at the same bias current and has the same minimum voltage requirement at the drain as in the circuit of Fig. P8.70(b).

8.71 Consider the cascode amplifier of Fig. 8.33 with the dc component at the input $V_I = 0.6$ V, $V_{G2} = 0.9$ V, $V_{G3} = 0.4$ V, $V_{G4} = 0.7$ V, and $V_{DD} = 1.3$ V. If all devices are matched, that is, $k_{n1} = k_{n2} = k_{p3} = k_{p4}$, and have equal $|V_t|$ of 0.4 V, what is the overdrive voltage at which the four transistors are operating? What is the allowable voltage range at the output?