# ECE 523/421 - Analog Electronics:
# University of New Mexico

**Problem 8.42**

**Figure P8.42 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{an} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q1 and Q2, find an expression for the overall voltage gain in terms of gm and ro of Q1 and Q2. If Q1 and Q2 are to be operated at equal overdrive voltages, |VOV|, find the required value of |VOV| if |VA| = 5 V and the gain required is 400 V/V.**

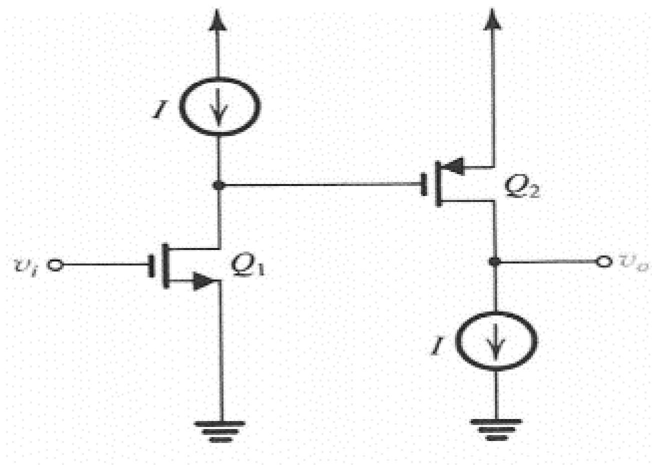



Figure P8.42

Using the π model of the two transistors.

$$v_{gs2} = -g_{m1} v_i (r_{o1} \,||\, r_{o1})$$
$$v_{gs2} = -g_{m1} v_i \left(\frac{r_{o1}}{2}\right)$$

We do the same for the second transistor

$$v_o = -g_{m2} v_{gs2} (r_{o2} \,||\, r_{o2})$$
$$v_o = -g_{m2} v_{gs2} \left(\frac{r_{o2}}{2}\right)$$

Since the ro and gm is equal for both transistors, and solving

$$v_o = -g_{m2} \left(-g_{m1} v_i \left(\frac{r_{o1}}{2}\right)\right)\left(\frac{r_{o2}}{2}\right)$$
$$G_v = \frac{v_o}{v_i} = {g_m}^2 \left(\frac{{r_o}^2}{4}\right)$$

For calculating $V_{ov}$

$$g_m = \frac{2I_D}{V_{OV}}$$

$$r_o = \frac{V_A}{I_D}$$

$$G_v = \frac{1}{4}\left(\frac{2I_D}{V_{OV}}\right)^2 \left(\frac{V_A}{I_D}\right)^2$$

$$G_v = \left(\frac{V_A}{V_{OV}}\right)^2$$

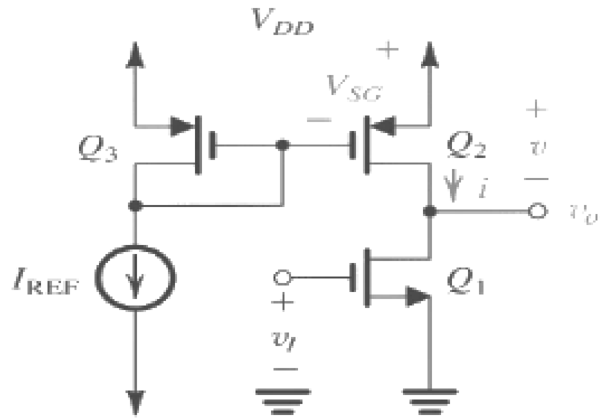
Using |VA| = 5 V and gain = 400 V/V.

$$V_{OV} = 0.25$$

**Problem 8.47**

**Consider the circuit shown in Fig. 8.16(a), using a 3.3-V supply and transistors for which $|V_t|$ = 0.8 V and L = 1 μm. For Q1, kn =100 μA/V2, VA =100 V, and W =20 μm. For Q2 and Q3, kp = 50 μA/V2 and |VA| = 50 V. For Q2, W = 40 μm. For Q3, W = 10 μm.**

- **(a) If Q1 is to be biased at 100 μA, find $I_{REF}$. For simplicity, ignore the effect of VA.**
- **(b) What are the extreme values of $v_O$ for which Q1 and Q2 just remain in saturation?**
- **(c) What is the large-signal voltage gain?**
- **(d) Find the slope of the transfer characteristic at $v_O$ =VDD/2.**
- **(e) For operation as a small-signal amplifier around a bias point at $v_O$ = VDD/2, find the small-signal voltage gain and output resistance.**




(a)

Calculating the reference current

$$I_{D2} = I_{D1} = 100\ \mu A$$

$$\frac{I_{D3}}{I_{D2}} = \left(\frac{W}{L}\right)_3 \Big/ \left(\frac{W}{L}\right)_2 = \frac{W_3}{W_2} = \frac{10}{40}$$

$$I_{D3} = \frac{1}{4} I_{D2}$$

$$I_{REF} = I_{D3} = 25\ \mu A$$

Calculating the output resistance

$$R_{out} = r_{o1} || r_{o2}$$

$$r_{o1} = \frac{V_{A1}}{I_D} = \frac{100}{0.1m} = 1M\Omega$$

$$r_{o2} = \frac{V_{A2}}{I_D} = \frac{50}{0.1m} = 500k\Omega$$

$$R_{out} = 333.3\ k\Omega$$

Calculating the small signal voltage gain

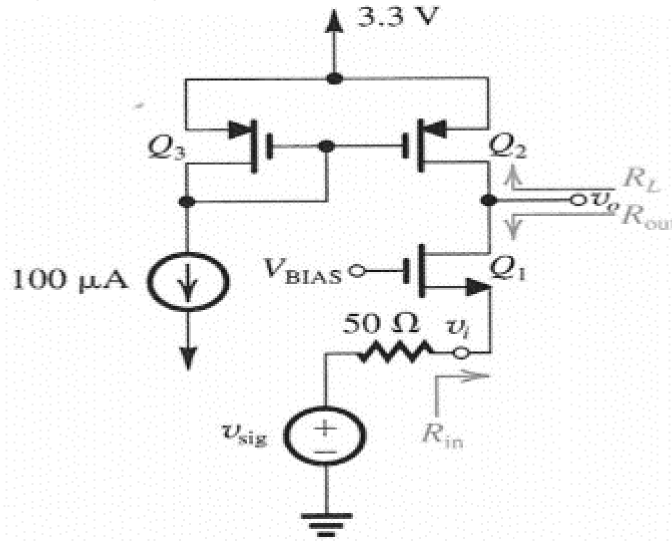
$$g_m = \sqrt{2k_n I_{D1}}$$
$$g_m = \sqrt{2(100\mu)(20/1)(100\mu)}$$
$$g_m = 0.632 \, {}^{mA}\!/_{V}$$

$$A_v = -g_{m1}(r_{o1}||r_{o2})$$
$$A_v = -210.6$$

**Problem 8.55**

**In the common-gate amplifier circuit of Fig. P8.55, Q2 and Q3 are matched. kn(W/L)n = kp(W/L)p = 4 mA/V2, and all transistors have |Vt| = 0.8V and |VA| = 20 V. The signal vsig is a small sinusoidal signal with no dc component.**

a) **Neglecting the effect of VA, find the dc drain current of Q1 and the required value of VBIAS.**
b) **Find the values of gm1 and ro for all transistors.**
c) **Find the value of Rin.**
d) **Find the value of Rout.**
e) **Calculate the voltage gains vo/vi and vo/vsig.**
f) **How large can vsig be (peak-to-peak) while maintaining saturation-mode operation for Q1 and Q2?**




a) The drain currents of Q2 is equal to Q3, so the drain current of Q1 is equal to drain current of transistor 3.

$$I_{D1} = 100\ \mu A$$

Using the expression of $I_{D1}$ and substituting the values we can obtain $v_{GS1}$

$$I_{D1} = \frac{1}{2} k_n (v_{GS1} - V_t)^2$$
$$100\ \mu = \frac{1}{2} 4m\ (v_{GS1} - 0.8)^2$$
$$v_{GS1} = 1.024\ V$$

For calculating $V_{BIAS}$

$$V_{BIAS} = I_{D1}\ R + \ v_{GS1}$$
$$V_{BIAS} = 100\ \mu A\ 50\Omega + \ 1.024V$$
$$V_{BIAS} = 1.029V$$

b) For calculating gm

$$g_m = \sqrt{2k_n I_{D1}}$$
$$g_m = \sqrt{2(4m)(100\mu)}$$
$$g_m = 0.89\, {}^{mA}\!/_{V}$$

For calculating ro

$$r_o = \frac{V_A}{I_D}$$
$$r_o = \frac{20}{100\ \mu A}$$
$$r_o = 200\ K\Omega$$

c) For calculating $R_{IN}$

$$R_{in} = \frac{r_{o1} + r_{o2}}{1 + r_{o1} g_{m1}}$$
$$R_{in} = \frac{200k + 200k}{1 + 200k(0.89m)}$$
$$R_{in} = 2.247\ k\Omega$$

d) For calculating $R_{OUT}$

$$R_{out} = r_{o1} + 50(1 + r_{o1} g_{m1})$$
$$R_{out} = 200k + 50(1 + 200k(0.89m))$$
$$R_{out} = 209\ k\Omega$$

e) For calculating the gains

$$v_o = v_i \left( \frac{(1 + r_{o1} g_{m1}) r_{o2}}{r_{o1} + r_{o2}} \right)$$
$$\frac{v_o}{v_i} = \left( \frac{(1 + 200k(0.89m))200k}{200k + 200k} \right)$$
$$\frac{v_o}{v_i} = 89.5$$
$$v_i = v_{sig} \left( \frac{R_{in}}{R_{in} + 50} \right)$$
$$v_o = v_{sig} \left( \frac{R_{in}}{R_{in} + 50} \right) \left( \frac{(1 + r_{o1} g_{m1}) r_{o2}}{r_{o1} + r_{o2}} \right)$$
$$\frac{v_o}{v_{sig}} = \left( \frac{2.247\ k}{2.247\ k + 50} \right) \left( \frac{(1 + 200k(0.89m))200k}{200k + 200k} \right)$$
$$G_V = 87.5$$

**Problem 8.62**
**In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 50. If the transistor is operated at VOV = 0.2 V, what must its VA be? If the process technology specifies $V_A$ as 5 V/μm, what channel length must the transistor have?**

As we saw in class, the factor that the problem state is

$$K = g_{m2} r_{o2}$$

$$g_m = \frac{2I_D}{V_{OV}}$$

$$r_o = \frac{V_A}{I_D}$$

$$K = \frac{2I_D}{V_{OV}} \frac{V_A}{I_D}$$

$$K = \frac{2V_A}{V_{OV}}$$

From here

$$V_A = 5V$$

For calculating the channel length

$$V_A = V_A{}' L$$

$$L = \frac{5V}{5\ {}^{V}/_{\mu m}}$$

$$L = 1\mu m$$

**Problem 8.65**

**Design the cascode amplifier of Fig. 8.30(a) to obtain gm1 = 2 mA/V and Ro = 200 kΩ. Use a 0.18-μm technology for which Vtn = 0.5 V, $V_A$ = 5 V/μm, and $k_n$= 400 μA/V2. Determine L, W/L, VG2, and I. Use identical transistors operated at VOV = 0.25 V, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?**

For calculating the current

$$g_m = \frac{2I_D}{V_{OV}}$$
$$I_D = \frac{g_m V_{OV}}{2}$$
$$I_D = \frac{2m\ 0.25}{2}$$
$$I_D = 0.25\ mA$$

For calculating the length

$$R_o = g_{m1} r_{o1} r_{o2}$$
$$r_o = \frac{V_A{}' L}{I_D}$$
$$R_o = g_{m1} \frac{V_A{}' L}{I_D} \frac{V_A{}' L}{I_D}$$
$$200\ k\Omega = 2m \frac{\left(5\ {}^{V}\!/_{\mu m}\right)^2 L^2}{0.25m^2}$$
$$L = 0.5\ \mu m$$

For calculating W/L

$$I_{D1} = \frac{1}{2} k_n{}' \frac{W}{L} (v_{GS1} - V_t)^2$$
$$0.25m = \frac{1}{2} 400\mu \frac{W}{L} (0.25)^2$$
$$\frac{W}{L} = 20$$

For maximum negative signal swing

$$V_{DS} = V_{OV} = 0.25V$$
$$V_{G2} = V_{DS} + V_{GS}$$
$$V_{G2} = V_{DS} + V_{OV} + V_{tn}$$
$$V_{G2} = 0.25 + 0.25 + 0.5$$
$$V_{G2} = 1V$$

For minimum output voltage

$$V_{out} = V_{DS} + V_{DS}$$
$$V_{out} = 0.25 + 0.25$$
$$V_{out} = 0.5V$$

**Problem 8.69**

**The cascode transistor can be thought of as providing a “shield” for the input transistor from the voltage variations at the output. To quantify this “shielding” property of the cascode, consider the situation in Fig. P8.69. Here we have grounded the input terminal (i.e., reduced vi to zero), applied a small change vx to the output node, and denoted the voltage change that results at the drain of Q1 by vy. By what factor is vy smaller than vx?**

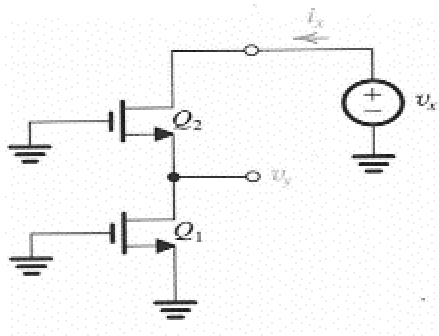



Figure P8.69

From the circuit we can see $v_{gs1} = 0$

$$v_i = v_{gs1} = 0$$
$$v_y = -v_{gs2}$$

Using the small signal model with the dependent source of Q1 in open circuit and using KCL in the $V_y$ node

$$\frac{v_y}{r_{o1}} - g_{m2}v_{gs2} + \frac{v_y - v_x}{r_{o2}} = 0$$
$$\frac{v_y}{r_{o1}} - g_{m2}v_y + \frac{v_y}{r_{o2}} = \frac{v_x}{r_{o2}}$$

Calculating $\frac{v_y}{v_x}$ from the formula

$$\frac{v_y}{v_x} = \frac{1}{g_{m2}r_{o2}}$$