*9.24 A design error has resulted in a gross mismatch in the circuit of Fig. P9.24. Specifically, Q_2 has twice the W/L ratio of Q_1. If v_{id} is a small sine-wave signal, find:

(a) I_{D1} and I_{D2}.
(b) V_{OV} for each of Q_1 and Q_2.
(c) The differential gain A_d in terms of R_D, I, and V_{OV}.

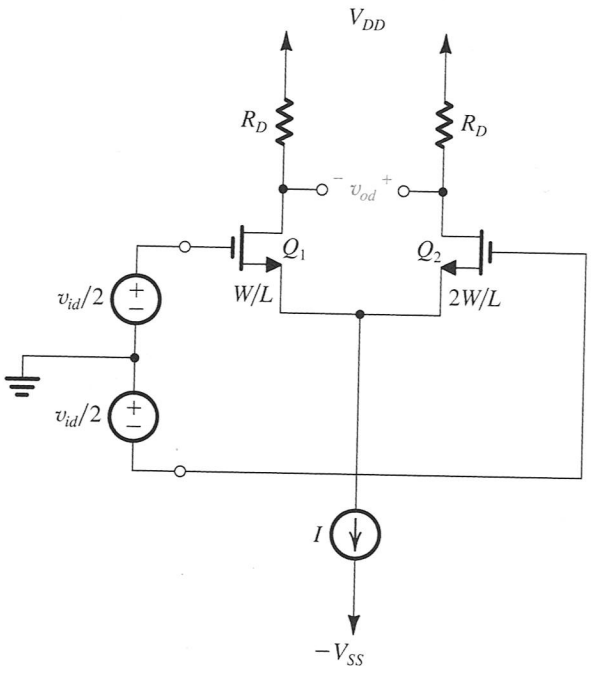

Figure P9.24

D 9.25 For the cascode differential amplifier of Fig. 9.13(a), show that if all transistors have the same channel length and are operated at the same $|V_{OV}|$ and assuming that $V'_{An} = |V'_{Ap}| = |V'_A|$, the differential gain A_d is given by

$$A_d = 2(|V_A|/|V_{OV}|)^2$$

Now design the amplifier to obtain a differential gain of 500 V/V. Use $|V_{OV}| = 0.2$ V. If $|V'_A| = 5$ V/μm, specify the required channel length L. If g_m is to be as high as possible but the power dissipation in the amplifier (in equilibrium) is to be limited to 0.5 mW, what bias current I would you use? Let $V_{DD} = V_{SS} = 0.9$ V.

Section 9.2: The BJT Differential Pair

9.26 For the differential amplifier of Fig. 9.15(a) let $I = 0.4$ mA, $V_{CC} = V_{EE} = 2.5$ V, $V_{CM} = -1$ V, $R_C = 5$ kΩ, and $\beta = 100$. Assume that the BJTs have $v_{BE} = 0.7$ V at $i_C = 1$ mA. Find the voltage at the emitters and at the outputs.

9.27 An *npn* differential amplifier with $I = 0.4$ mA, $V_{CC} = V_{EE} = 2.5$ V, and $R_C = 5$ kΩ utilizes BJTs with $\beta = 100$ and $v_{BE} = 0.7$ V at $i_C = 1$ mA. If $v_{B2} = 0$, find V_E, V_{C1}, and V_{C2} obtained with $v_{B1} = +0.5$ V, and with $v_{B1} = -0.5$ V. Assume that the current source requires a minimum of 0.3 V for proper operation.

9.28 An *npn* differential amplifier with $I = 0.4$ mA, $V_{CC} = V_{EE} = 2.5$ V, and $R_C = 5$ kΩ utilizes BJTs with $\beta = 100$ and $v_{BE} = 0.7$ V at $i_C = 1$ mA. Assuming that the bias current is obtained by a simple current source and that all transistors require a minimum v_{CE} of 0.3 V for operation in the active mode, find the input common-mode range.

9.29 Repeat Exercise 9.7 for an input of –0.3 V.

9.30 An *npn* differential pair employs transistors for which $v_{BE} = 690$ mV at $i_C = 1$ mA, and $\beta = 50$. The transistors leave the active mode at $v_{CE} \leq 0.3$ V. The collector resistors $R_C = 82$ kΩ, and the power supplies are ±1.2 V. The bias current $I = 20$ μA and is supplied with a simple current source.

(a) For $v_{B1} = v_{B2} = V_{CM} = 0$ V, find V_E, V_{C1}, and V_{C2}.
(b) Find the input common-mode range.
(c) If $v_{B2} = 0$, find the value of v_{B1} that increases the current in Q_1 by 10%.

9.31 Consider the BJT differential amplifier when fed with a common-mode voltage V_{CM} as shown in Fig. 9.15(a). As is often the case, the supply voltage V_{CC} may not be pure dc but might include a ripple component v_r of small amplitude and a frequency of 120 Hz (see Section 4.5). Thus the supply voltage becomes $V_{CC} + v_r$. Find the ripple component of the collector voltages, v_{C1} and v_{C2}, as well as of the difference output voltage $v_{od} \equiv v_{C2} - v_{C1}$. Comment on the differential amplifier response to this undesirable power-supply ripple.

D 9.32 Consider the differential amplifier of Fig. 9.14 and let the BJT β be very large:

(a) What is the largest input common-mode signal that can be applied while the BJTs remain comfortably in the active region with $v_{CB} = 0$?
(b) If the available power supply V_{CC} is 2.0 V, what value of IR_C should you choose in order to allow a common-mode input signal of ±1.0 V?
(c) For the value of IR_C found in (b), select values for I and R_C. Use the largest possible value for I subject to the

D 9.60 A MOS differential amplifier utilizing a simple current source to provide the bias current I is found to have a CMRR of 60 dB. If it is required to raise the CMRR to 100 dB by adding a cascode transistor to the current source, what must the intrinsic gain A_0 of the cascode transistor be? If the cascode transistor is operated at $V_{OV} = 0.2$ V, what must its V_A be? If for the specific technology utilized $V_A' = 5$ V/μm, specify the channel length L of the cascode transistor.

9.61 The differential amplifier circuit of Fig. P9.61 utilizes a resistor connected to the negative power supply to establish the bias current I.

(a) For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$.
(b) For $v_{B1} = v_{B2} = v_{icm}$, where v_{icm} has a zero average, find the magnitude of the common-mode gain, $|v_o/v_{icm}|$.
(c) Calculate the CMRR.
(d) If $v_{B1} = 0.1 \sin 2\pi \times 60t + 0.005 \sin 2\pi \times 1000t$, volts, and $v_{B2} = 0.1 \sin 2\pi \times 60t - 0.005 \sin 2\pi \times 1000t$, volts, find v_o.

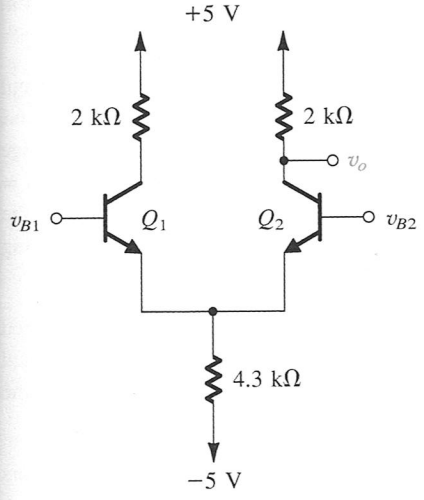

Figure P9.61

9.62 For the differential amplifier shown in Fig. P9.62, identify and sketch the differential half-circuit and the common-mode half-circuit. Find the differential gain, the differential input resistance, the common-mode gain assuming the resistances R_C have 1% tolerance, and the common-mode input resistance. For these transistors, $\beta = 100$ and $V_A = 100$ V.

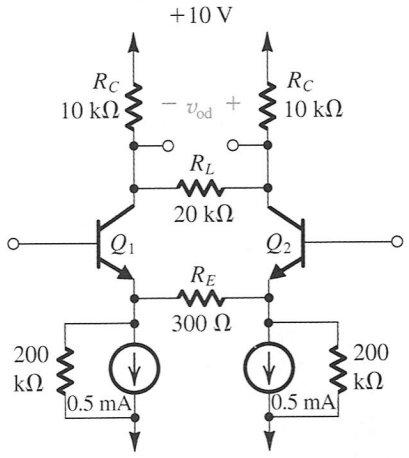

Figure P9.62

9.63 Consider the basic differential circuit in which the transistors have $\beta = 100$ and $V_A = 100$ V, with $I = 0.2$ mA, $R_{EE} = 500$ kΩ, and $R_C = 25$ kΩ. The collector resistances are matched to within 1%. Find:

(a) the differential gain
(b) the differential input resistance
(c) the common-mode gain
(d) the common-mode rejection ratio
(e) the common-mode input resistance

9.64 In a bipolar differential-amplifier circuit, the bias current generator consists of a simple common-emitter transistor operating at 200 μA. For this transistor, and those used in the differential pair, $V_A = 20$ V and $\beta = 50$. What common-mode input resistance would result? Assume $R_C \ll r_o$.

9.65 A bipolar differential amplifier with $I = 0.5$ mA utilizes transistors for which $V_A = 50$ V and $\beta = 100$. The collector resistances $R_C = 5$ kΩ and are matched to within 10%. Find:

(a) the differential gain
(b) the common-mode gain and the CMRR if the bias current I is generated using a simple current mirror
(c) the common-mode gain and the CMRR if the bias current I is generated using a Wilson mirror. (Refer to Eq. 8.95 for R_o of the Wilson mirror.)

D 9.66 It is required to design a differential amplifier to provide the largest possible signal to a pair of 10-kΩ load

9.92 A current-mirror-loaded NMOS differential amplifier operates with a bias current I of 200 μA. The NMOS transistors are operated at $V_{OV} = 0.2$ V and the PMOS devices at $|V_{OV}| = 0.3$ V. The Early voltages are 20 V for the NMOS and 12 V for the PMOS transistors. Find G_m, R_o, and A_d. For what value of load resistance is the gain reduced by a factor of 2?

9.93 This problem investigates the effect of transistor mismatches on the input offset voltage of the current-mirror-loaded MOS differential amplifier of Fig. 9.32(a). For this purpose, ground both input terminals and short-circuit the output node to ground.

(a) If the amplifying transistors Q_1 and Q_2 exhibit a W/L mismatch of $\Delta(W/L)_A$, find the resulting short-circuit output current and hence show that the corresponding V_{OS} is given by

$$V_{OS1} = (V_{OV}/2)\frac{\Delta(W/L)_A}{(W/L)_A}$$

where V_{OV} is the overdrive voltage at which Q_1 and Q_2 are operating.

(b) Repeat for a mismatch $\Delta(W/L)_M$ in the W/L ratios of the mirror transistor Q_3 and Q_4 to show that the corresponding V_{OS} is given by

$$V_{OS2} = (V_{OV}/2)\frac{\Delta(W/L)_M}{(W/L)_M}$$

where V_{OV} is the overdrive voltage at which Q_1 and Q_2 are operating.

(c) For a circuit in which all transistors are operated at $|V_{OV}| = 0.2$ V and all W/L ratios are accurate to within ±1% of nominal, find the worst-case total offset voltage V_{OS}.

9.94 The differential amplifier in Fig. 9.36(a) is operated with $I = 500$ μA, with devices for which $V_A = 10$ V and $\beta = 100$. What differential input resistance, output resistance, short-circuit transconductance, and open-circuit voltage gain would you expect? What will the voltage gain be if the input resistance of the subsequent stage is equal to R_{id} of this stage?

9.95 A bipolar differential amplifier having a simple *pnp* current-mirror load is found to have an input offset voltage of 2 mV. If the offset is attributable entirely to the finite β of the *pnp* transistors, what must β_P be?

9.96 For the current-mirror-loaded bipolar differential pair, replacing the simple current-mirror load by the base-current-compensated mirror of Fig. 8.11, find the expected systematic input offset voltage. Evaluate V_{OS} for $\beta_P = 50$.

9.97 For the current-mirror-loaded bipolar differential pair, replacing the simple current-mirror load by the Wilson mirror of Fig. 8.40(a), find the expected systematic input offset voltage. Evaluate V_{OS} for $\beta_P = 50$.

9.98 Figure P9.98 shows a differential cascode amplifier with an active load formed by a Wilson current mirror. Utilizing the expressions derived in Chapter 8 for the output resistance of a bipolar cascode and the output resistance of the Wilson mirror, and assuming all transistors to be identical, show that the differential voltage gain A_d is given approximately by

$$A_d = \frac{1}{3}\beta g_m r_o$$

Evaluate A_d for the case of $\beta = 100$ and $V_A = 20$ V.

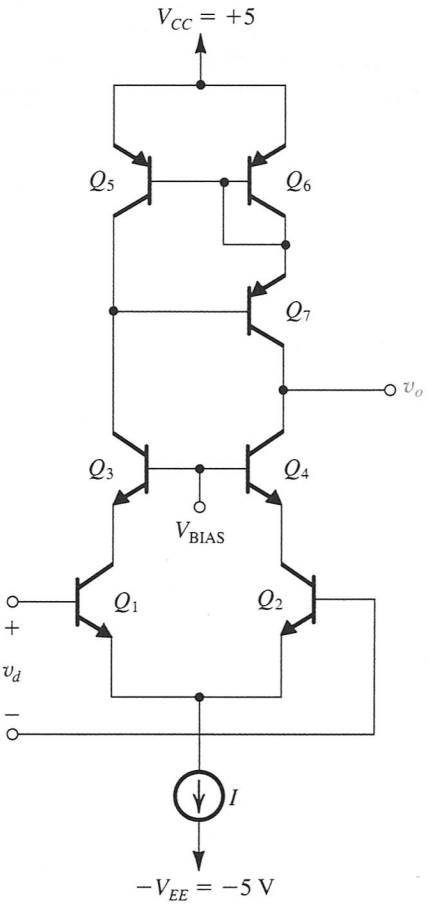

Figure P9.98

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

Table P9.113

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5

common-mode range, and the output voltage range. Neglect the effect of V_A on the bias currents.

D 9.114 The two-stage CMOS op amp in Fig. P9.114 is fabricated in a 0.18-μm technology having $k_n' = 4k_p' = 400\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.4$ V.

(a) With A and B grounded, perform a dc design that will result in each of Q_1, Q_2, Q_3, and Q_4 conducting a drain current of 100 μA and each of Q_6 and Q_7 a current of 200 μA. Design so that all transistors operate at 0.2-V overdrive voltages. Specify the W/L ratio required for each MOSFET. Present your results in tabular form. What is the dc voltage at the output (ideally)?
(b) Find the input common-mode range.
(c) Find the allowable range of the output voltage.
(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 6 V.

D *9.115 In a particular design of the CMOS op amp of Fig. 9.40 the designer wishes to investigate the effects of increasing the W/L ratio of both Q_1 and Q_2 by a factor of 4. Assuming that all other parameters are kept unchanged, refer to Example 9.6 to help you answer the following questions:

(a) Find the resulting change in $|V_{OV}|$ and in g_m of Q_1 and Q_2.
(b) What change results in the voltage gain of the input stage? In the overall voltage gain?
(c) What is the effect on the input offset voltages? (You might wish to refer to Section 9.4).

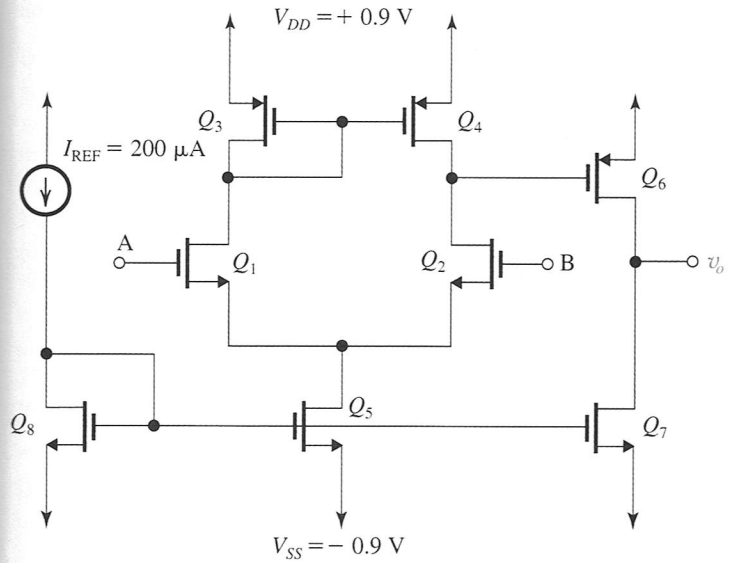

Figure P9.114

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

9.116 Consider the amplifier of Fig. 9.40, whose parameters are specified in Example 9.6. If a manufacturing error results in the W/L ratio of Q_7 being 48/0.8, find the current that Q_7 will now conduct. Thus find the systematic offset voltage that will appear at the output. (Use the results of Example 9.6.) Assuming that the open-loop gain will remain approximately unchanged from the value found in Example 9.6, find the corresponding value of input offset voltage, V_{OS}.

9.117 Consider the input stage of the CMOS op amp in Fig. 9.40 with both inputs grounded. Assume that the two sides of the input stage are perfectly matched except that the threshold voltages of Q_3 and Q_4 have a mismatch ΔV_t. Show that a current $g_{m3}\Delta V_t$ appears at the output of the first stage. What is the corresponding input offset voltage?

9.118 The two-stage op amp in Figure P9.114 is fabricated in a 65-nm technology having $k_n' = 5.4 \times k_p' = 540\ \mu\text{A/V}^2$ and $V_{tn} = -V_{tp} = 0.35$ V. The amplifier is operated with $V_{DD} = +1.2$ V and $V_{SS} = 0$ V.

(a) With A and B at a dc voltage of $V_{DD}/2$, perform a dc design that will result in each of Q_1, Q_2, Q_3, and Q_4 conducting a drain current of 200 μA and each of Q_6 and Q_7 conducting a current of 400 μA. Design so that all transistors operate at 0.15-V overdrive voltages. Specify the W/L ratio required for each MOSFET. Present all results in a table.

(b) Find the input common-mode range.

(c) Find the allowable range of the output voltage.

(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 1.8 V.

***9.119** Figure P9.119 shows a bipolar op-amp circuit that resembles the CMOS op amp of Fig. 9.40. Here, the input differential pair Q_1–Q_2 is loaded in a current mirror formed by Q_3 and Q_4. The second stage is formed by the current-source-loaded common-emitter transistor Q_5. Unlike the CMOS circuit, here there is an output stage formed by the emitter follower Q_6. The function of capacitor C_C will be explained later, in Chapter 11. All transistors have $\beta = 100$, $|V_{BE}| = 0.7$ V, and $r_o = \infty$.

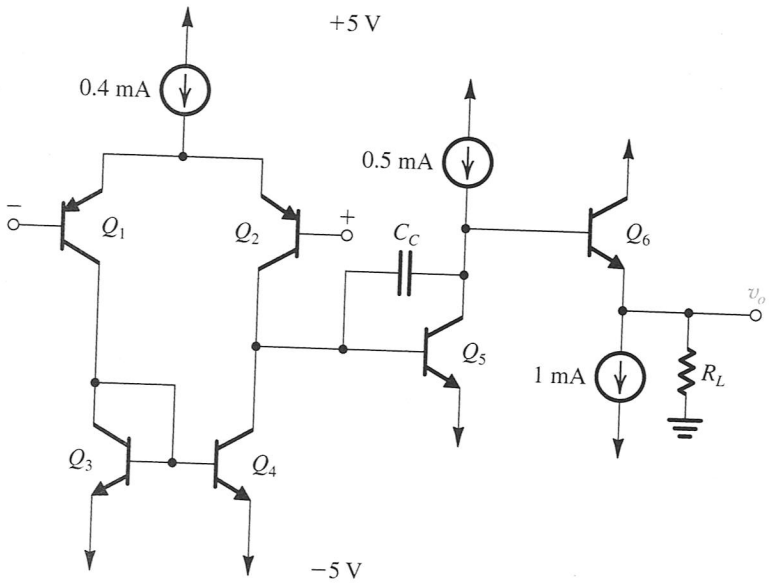

Figure P9.119

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(a) For inputs grounded and output held at 0 V (by negative feedback, not shown) find the emitter currents of all transistors.
(b) Calculate the gain of the amplifier with $R_L = 1$ kΩ.

9.120 A BJT differential amplifier, biased to have $r_e = 50\ \Omega$ and utilizing two 50-Ω emitter resistors and 5-kΩ loads, drives a second differential stage biased to have $r_e = 25\ \Omega$. All BJTs have $\beta = 100$. What is the voltage gain of the first stage? Also find the input resistance of the first stage, and the current gain from the input of the first stage to the collectors of the second stage.

9.121 In the multistage amplifier of Fig. 9.41, emitter resistors are to be introduced—100 Ω in the emitter lead of each of the first-stage transistors and 25 Ω for each of the second-stage transistors. What is the effect on input resistance, the voltage gain of the first stage, and the overall voltage gain? Use the bias values found in Example 9.7.

D 9.122 Consider the circuit of Fig. 9.41 and its output resistance. Which resistor has the most effect on the output resistance? What should this resistor be changed to if the output resistance is to be reduced by a factor of 2? What will the amplifier gain become after this change? What other change can you make to restore the amplifier gain to approximately its prior value?

D 9.123 (a) If, in the multistage amplifier of Fig. 9.41, the resistor R_5 is replaced by a constant-current source $\simeq 1$ mA, such that the bias situation is essentially unaffected, what does the overall voltage gain of the amplifier become? Assume that the output resistance of the current source is very high. Use the results of Example 9.8.
(b) With the modification suggested in (a), what is the effect of the change on output resistance? What is the overall gain of the amplifier when loaded by 100 Ω to ground? The original amplifier (before modification) has an output resistance of 152 Ω and a voltage gain of 8513 V/V. What is its gain when loaded by 100 Ω? Comment. Use $\beta = 100$.

***9.124** Figure P9.124 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.

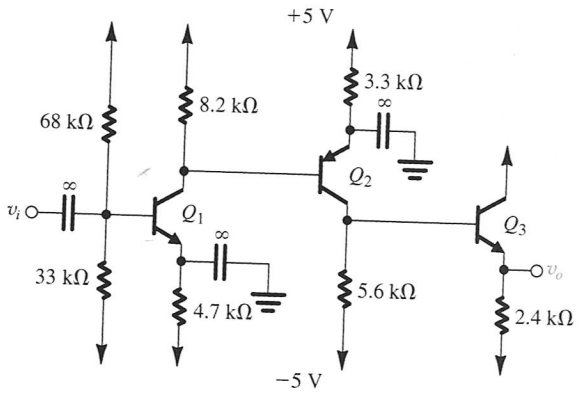

Figure P9.124

(a) Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume $|V_{BE}| = 0.7$ V, $\beta = 100$, and neglect the Early effect.
(b) Find the input resistance and the output resistance.
(c) Use the current-gain method to evaluate the voltage gain v_o/v_i.

9.125 For the current mirror in Fig. P9.125, replace the transistors with their hybrid-π models and show that:

$$R_i = \frac{1}{g_{m1}} \| r_{o1}$$

$$A_{is} \simeq A_{is}\Big|_{\text{ideal}} \left(1 - \frac{1}{g_{m1} r_{o1}}\right)$$

$$A_{is}\Big|_{\text{ideal}} = g_{m2}/g_{m1}$$

$$R_o = r_{o2}$$

where A_{is} denotes the short-circuit current gain.

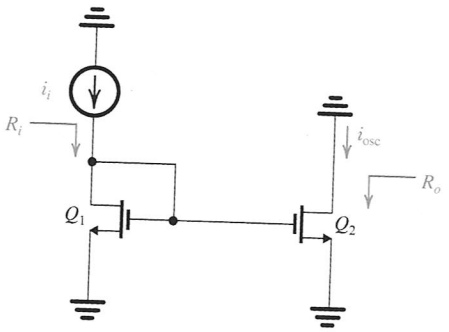

Figure P9.125

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem